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## Links & resources

Answers to many questions (e.g. structure and content of the configuration files, etc.) are covered in [this presentation](#) by Sven Dornbusch.

The latest DBBC3 software, firmware and documentation can be obtained from the [HatLab website](#) (login required).

A python toolkit for DBBC3 control and monitoring can be obtained from [GitHub](#).

## DDC Mode

### Configuring the BBCs (DDC\_U mode)

```
open c:/DBBC_CONF/config_ddc_u.txt
```

```
1 3024.0 64
2 3152.0 64
3 3280.0 64
4 3408.0 64
5 0.0 64
6 0.0 64
7 0.0 64
8 0.0 64
9 . . . . .
```

column 1: BBC number

column 2: Frequency in MHz. Setting a frequency to 0.0 will disable the BBC

column 3: Bandwidth in MHz

BBC	Board	eth device	
1-8	A	eth0	
9-16	B	eth0	
17-24	C	eth0	
25-32	D	eth0	
...	...	...	
65-72	A	eth1	
73-80	B	eth1	
...	...	...	

**Notes:**

- If defining less than 8 BBCs per block the vsi-bitmask must be set in order to not output any data streams for the disabled BBC. The vsi\_bitmask command must be set prior to the vdif\_frame command:

```
vsi_bitmask 0x0000FFFF 0x0000FFFF 0x0000FFFF 0x0000FFFF
vdif_frame ...
```

The above example sets the mask for 4 BBCs per block

- If defining bandwidths < 128 MHz the clock divisor must be set with the vsi\_samplerate directive *before* setting the vdif\_frame command:

```
vsi_samplerate 128000000 2
```

The above line will set the sampling clock for 64 MHz bands.

**Setting the vsi-bitmask**

By default all 32 output datastreams corresponding to the 16 BBCs (USB and LSB) are enabled. If running the DDC mode with less than 16 BBCs per board the unused datastreams should be disabled.

This is done by placing the vsi\_bitmask directive in the fila10 configuration file of the board (e.g. ddc\_U\_core3H\_1.fila10g).

**Note: The directive must be placed prior to the vdif\_frame command**

```
vsi_bitmask 0x0000FFFF 0x0000FFFF 0x0000FFFF 0x0000FFFF
vdif_frame ...
```

Bitmask logic:

	DWORD 1	DWORD 2	DWORD 3	DWORD 4
bitmask (hex)	0x0000FFFF	0x0000FFFF	0x0000FFFF	0x0000FFFF
BBC#	16.....9	87654321	16.....9	87654321

Note: DWORD 1 and 3 must be identical; DWORD 2 and 4 must be identical.

The above example would disable the output streams from BBCs 13-16 and 5-8

Each half-byte contains the bit-mask for the sign and magnitude bits of the upper and lower side band produced by the corresponding BBC.

F = 1111 (sign and magnitude enabled for upper and lower sideband)

C = 1100 (Check: sign and mag enabled for lower sideband)

3 = 0011 (Check: sign and mag enabled for upper sideband)

## OCT\_D Mode

### Setting up config-files for different filter bandwidth

The filters can be loaded with the tap-command, for example:

```
tap=1,1,0-250_64taps.flr
```

will load the 0-250MHz filter into the first filter of the first board.

Parameter 1 is the board number (1-8)

Parameter 2 is the filter number (1 or 2)

Parameter 3 is the filename of the filter to be loaded.

The filters can be loaded once the control software is started. You can load different filters with the same bandwidth without the need to restart or reset anything.

The default filters after the start of the control software are 2000-4000 MHz in filter 1 (eth0 output) and 0-2000 MHz in filter 2 (eth2 output)

When you want to test a filter with a different bandwidth you need to adjust the config file for the Core3Hs you are using:

the vsi\_bitmask command followed by a reset command needs to be inserted at the correct position in the corresponding fila10g-config files (like oct\_D\_core3H\_1.fila10g)

for 2000 MHz: no vsi\_bitmask command should be inserted, or remove the vsi\_bitmask and reset commands if present

for 1000 MHz: insert the vsi\_bitmask and reset command at line 3 and 4 after the core3\_init command like this:

```
reboot
core3_init
vsi_bitmask 0x33333333 0x33333333 0x33333333 0x33333333 0x33333333
0x33333333 0x33333333 0x33333333
reset
....
```

for 500 MHz:

```
reboot
core3_init
vsi_bitmask 0x03030303 0x03030303 0x03030303 0x03030303 0x03030303
0x03030303 0x03030303 0x03030303
```

```
reset  
....
```

for 250 MHz:

```
reboot  
core3_init  
vsi_bitmask 0x00030003 0x00030003 0x00030003 0x00030003 0x00030003  
0x00030003 0x00030003 0x00030003  
reset  
....
```

So to use a 250 MHz filter for example you need to:

1. Insert the vsi\_bitmask and reset commands into the config-files
2. Start or Restart the control software to load the correct config.  
If the OCT\_D firmware is already loaded, there is no need to reload the firmware, reloading the config is enough.
3. Load the 250MHZ-filters with the tap-command.