Description

Issue observed at PV. Samplers randomly get out of sync (indicated by dsc_corr and checkphase commands). A similar (or identical) issue has been seen with the Ishioka system in the MPIfR lab as well as with the Bonn Lab system.

Findings

- Happens with all DDC modes: DDC_L, DDC_V and DDC_U with calibration loop enabled
- Does not happen on OCT_D and DSC modes
- Apparently does not happen on DDC modes when calibration loop is disabled
- Sometimes can be triggered by touching the "sys clk" port on the DBBC3 backside

Possibly solution:

Gino was suggesting that the issue might be caused by an unterminated "sys clk out" port of the DBBC3. This was confirmed by Michael. Terminating the port should reduce the likelyhood of the samplers getting out of sync.

Tests:

Port was terminated by Salvador on the PV system on 24.3.2020 (15:00).

Test procedure:

1. Reload DDC_V 124 (no multicast)
2. execute samplerResync.py until sampler synchronization is achieved.
3. execute monitorStability.py for a longer period

Results

run date / time	out of sync	when	boards	Comments
24.3. 19:31	yes	20:50	3	sysclk port terminated