General

1st LO = 92100 MHz

Total LO (DBBC2) = 85500 MHz

Total LO (DBBC3) = 84100 MHz (UI band)

DBBC2

Firmware

- Installed new firmware ddc v107 beta3
- Finished DBBC3 calibration

Tone injection

- noise + tone injected into pins 4 of board A and B
- verified if power levels (attenuation 23)
- set vsi_clk=128
- set dbbcform=astro

tone (MHz)	IF A	IFB	
528	OK	OK	
592	OK	OK	
656	**Missing**	OK	
720	OK	OK	
784	**Missing**	OK	
848	OK	OK	
912	**Missing**	OK	
976	OK	OK	

Bandpass plot shows that LSB of BBC2, BBC3, BBC4 are corrupted

Cleaned connectors of VSI1 cable connectin DDBC2 to Fila10G. No change. As a test have re-configured Fila10G to use vsi2 instead of vsi1 which has not changed the result. This implies that it is not a transmission problem over the VSI cables.

Update: Due to a power failure on March 3rd the VLBI equipment was brought down (DBBC2, Fila10G). After restarting all equipment the bandpass now looks good and lines are verified in all subbands.

DBBC3

Firmware installation

- installed DDC_V_123

IF-Setup

IF1 (E0VLI, LCP) => CoreBoardA => recorder2 eth3 => Module MPI%8005 (slot 1)

IF3 (E0HLI, RCP) => CoreBoardB => recorder2 eth35 => Module MPI%8008 (slot 2)

System verification

- run setupDBBC3_DDC_V.py

```
(env) [oper@cc-pico utilities]$ ./setupDBBC3_DDC_V.py -n 4 192.168.0.60
--ignore-errors -i A B
Selecting commandset version: DBBC3Commandset_DDC_V_123
===Trying to connect to 192.168.0.60:4000
===Connected
===Checking 1PPS synchronisation
[WARN] The following boards report pps_delay=0: ['C', 'D']
[RESOLUTION] Check if these boards have been disabled in the DBBC3 config
file
=== Checking time synchronisation of core board A
[OK] Reported time: 2019-04-04 11:31:07
===Checking synthesizer lock state of board A
[OK] Locked
===Checking GCoMo synthesizer frequency of board A
[OK] Freq=9048 MHz
=== Checking IF power level on core board A
[OK] count = 31895
 ===Checking sampler gains for board A
[OK] sampler powers = [70874617, 71217086, 71445220, 70643756]
===Checking sampler offsets for board A sampler 0
[OK] Asymmetry = 0.000604%
===Checking sampler offsets for board A sampler 1
[OK] Asymmetry = 0.006149%
===Checking sampler offsets for board A sampler 2
[OK] Asymmetry = 0.020379%
===Checking sampler offsets for board A sampler 3
[OK] Asymmetry = 0.014416%
=== Checking time synchronisation of core board B
[OK] Reported time: 2019-04-04 11:31:18
===Checking synthesizer lock state of board B
[OK] Locked
===Checking GCoMo synthesizer frequency of board B
[OK] Freq=9048 MHz
=== Checking IF power level on core board B
[OK] count = 31750
 ===Checking sampler gains for board B
[OK] sampler powers = [82511346, 82256136, 85668418, 81651315]
===Checking sampler offsets for board B sampler 0
[OK] Asymmetry = 0.007875%
===Checking sampler offsets for board B sampler 1
```

```
[OK] Asymmetry = 0.003713%
===Checking sampler offsets for board B sampler 2
[OK] Asymmetry = 0.012987%
===Checking sampler offsets for board B sampler 3
[OK] Asymmetry = 0.010675%
=== Done
```

Tone injection

Tone was injected into the beam at 86.242GHz

Line appeared in both polarizations in the baseband at 3190 MHz.

Recording

The recorded bistreams are in the following order:

BBC01_USB / BBC01_LSB / BBC02_USB / BBC02_LSB / ....

LCP	RCP