

DBBC Setup and Operation

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IVS TOW, MIT-Haystack Observatory, May 2015

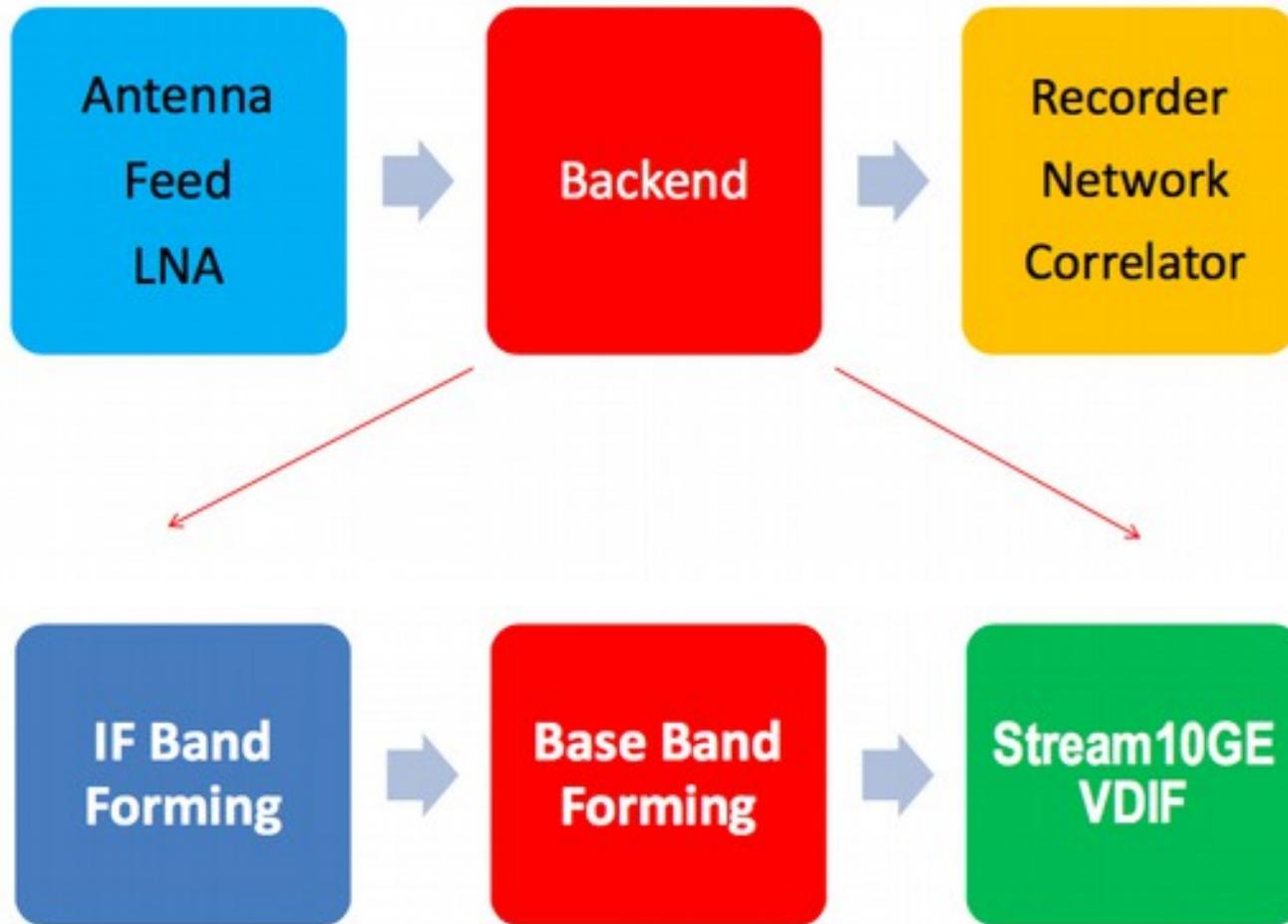


Content

- DBBC hardware characteristics
 - What is it good for
 - A tour around the DBBC
 - Component description
- Installation of a DBBC
- DBBC software
 - Poly-phase Filter Bank (PFB)
 - Digital Down Conversion (DDC)
- Basic testing
- Field System integration
- VLBI operation



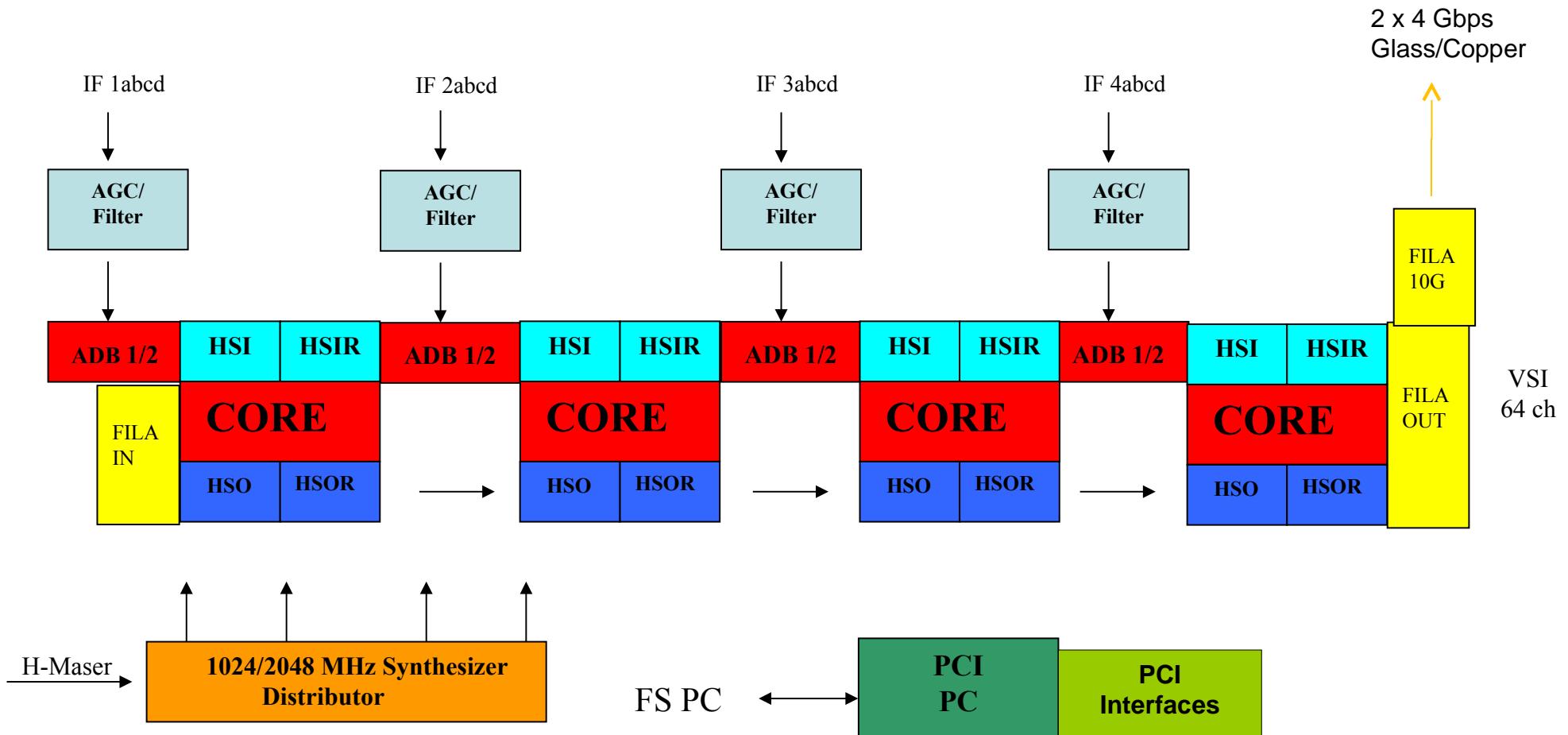
The VLBI backend





The DBBC Architecture

IF_n (MHz)
 1~512, 512~1024, 1024~1536, 1536~2048
 or
 1~1024, 1024~2048 MHz





DBBC Outside (front view)

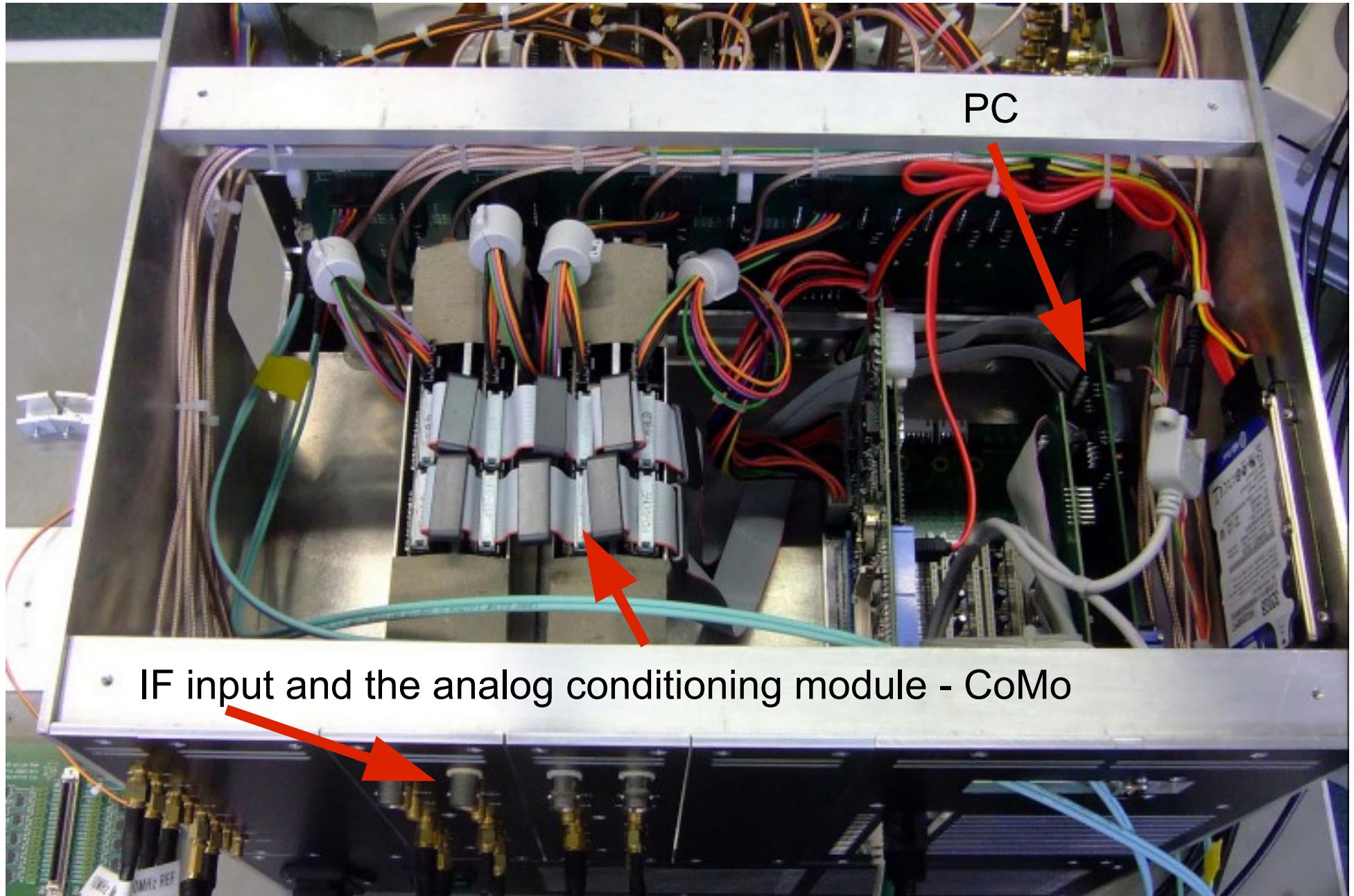




DBBC Outside (rear view)

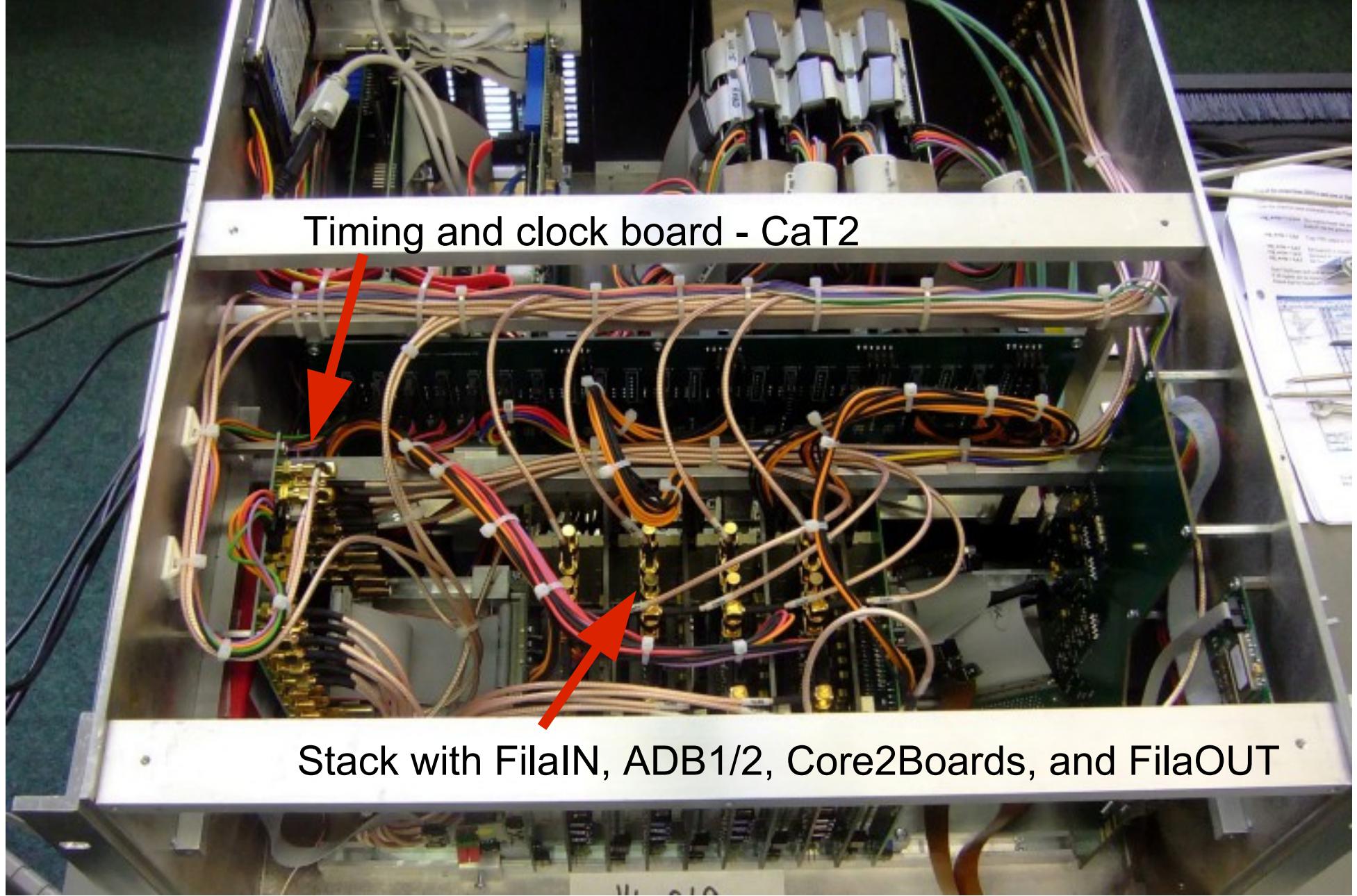


DBBC Inside

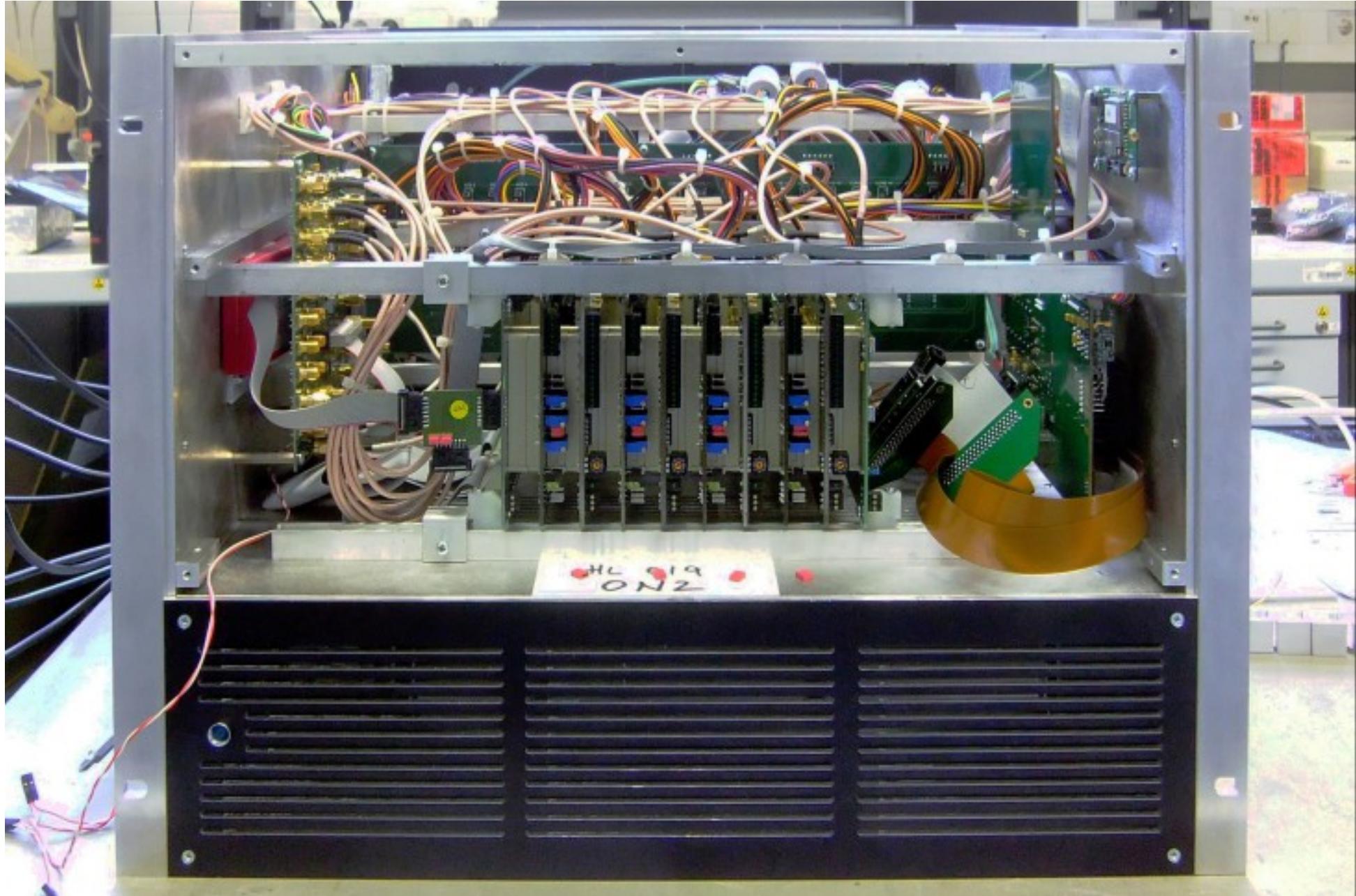




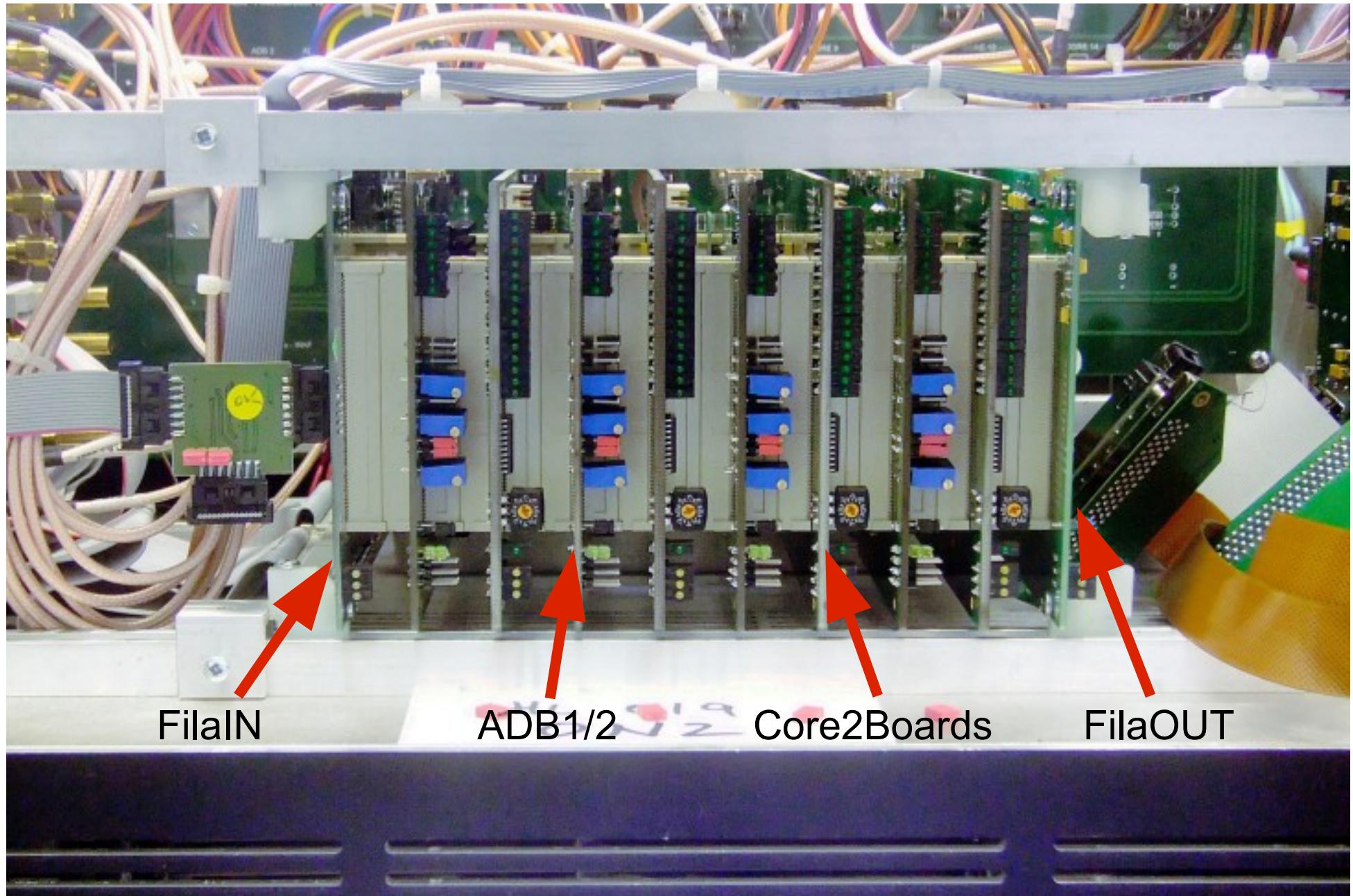
DBBC Inside



DBBC Inside



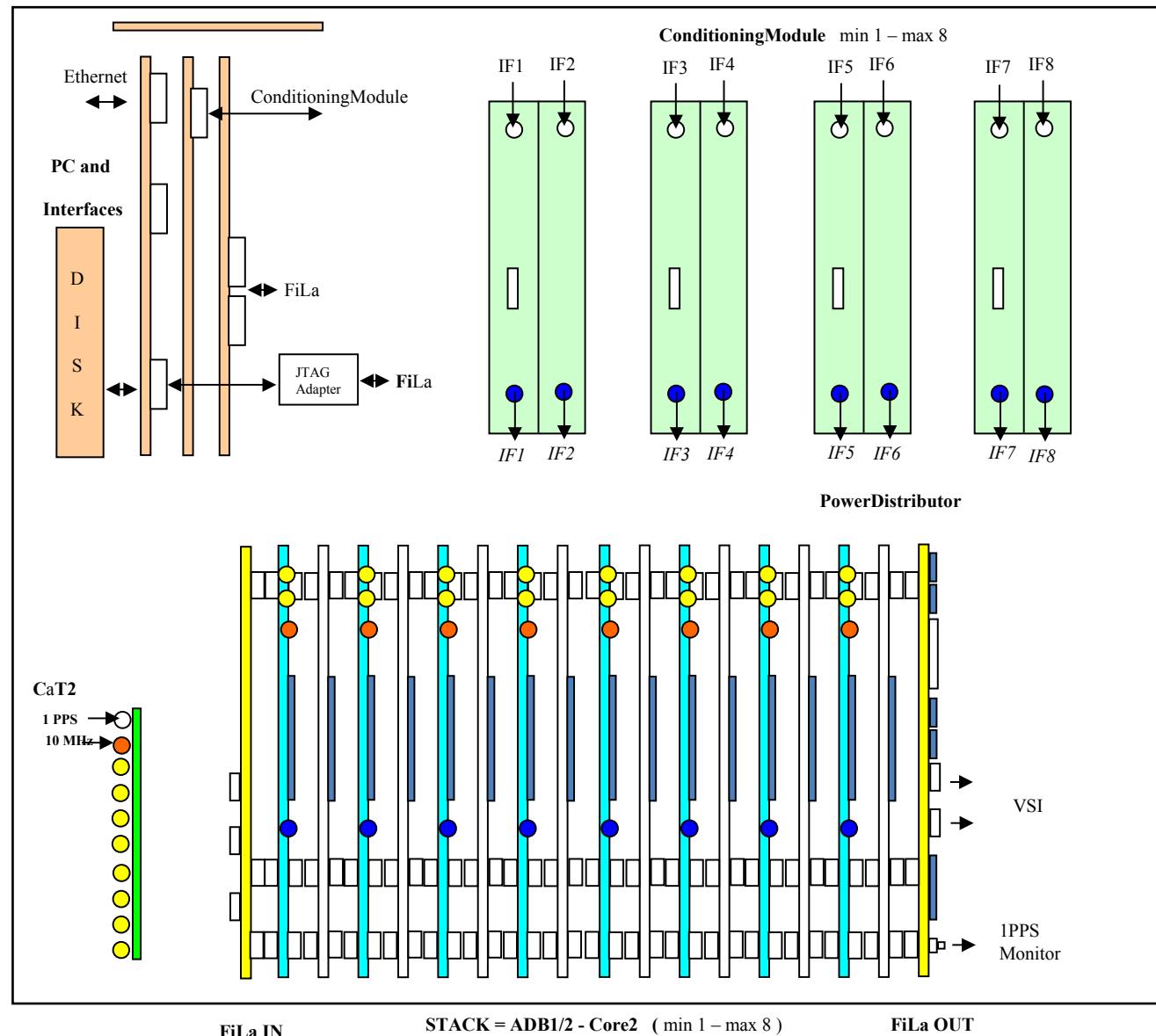
DBBC Inside





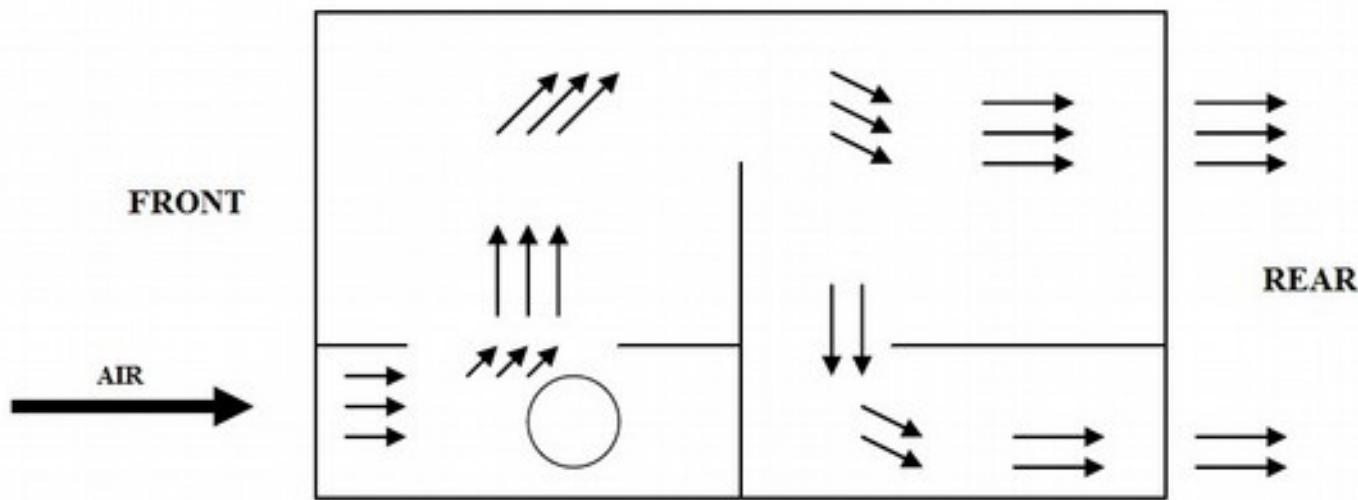
The DBBC Architecture

DBBC2 / DCCB2010 Schematic Top View





The DBBC Architecture



The air cooling flow from a side view



General Features

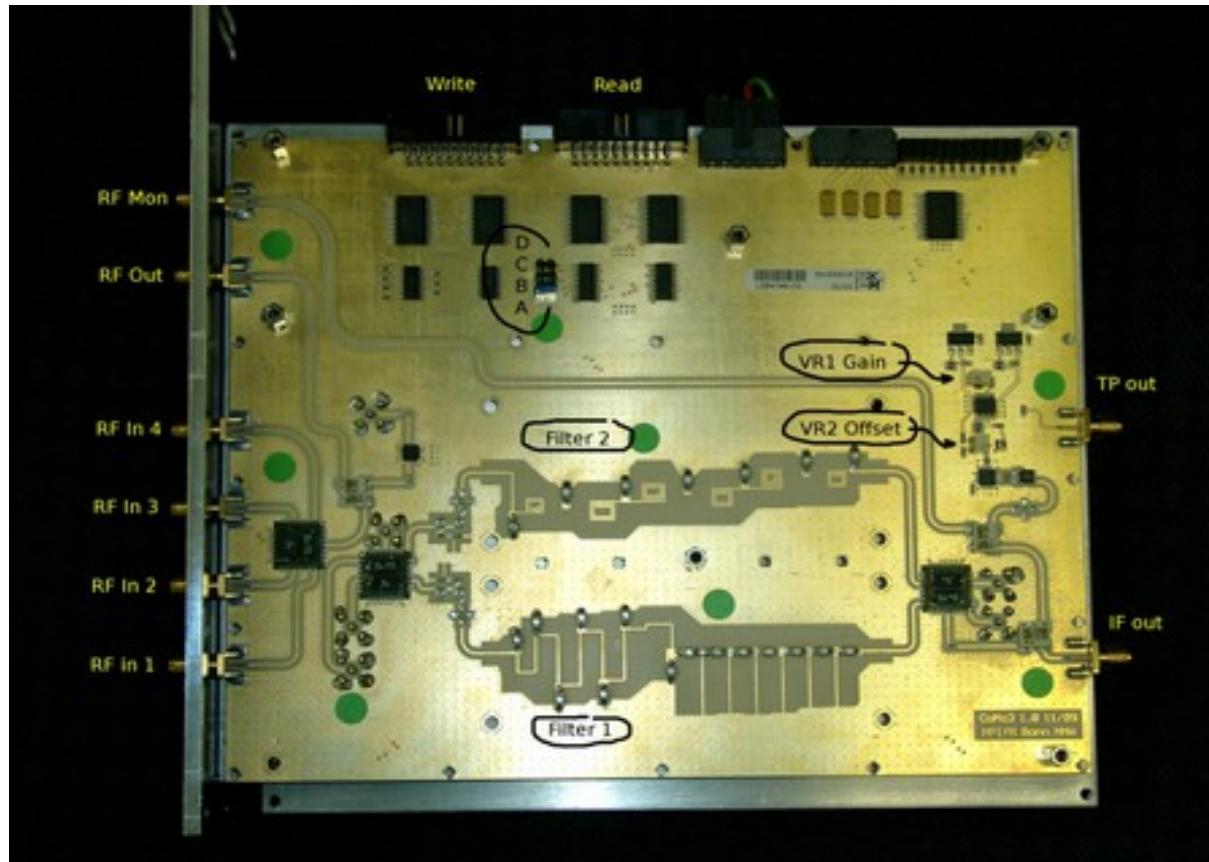
- 4/8 RF/IF Input out of 16 (4x4) in a range up to 2.2 (3.5) GHz
- 1024/2048 MHz sampling clock frequency
- More personalities for different observing modes
- Input 4/8 polarizations / bands
- Output 4/8 groups of 32 data channel
- Output as VSI interfaces or as 10G Ethernet streams
- Control under Field System or other client console



Component description

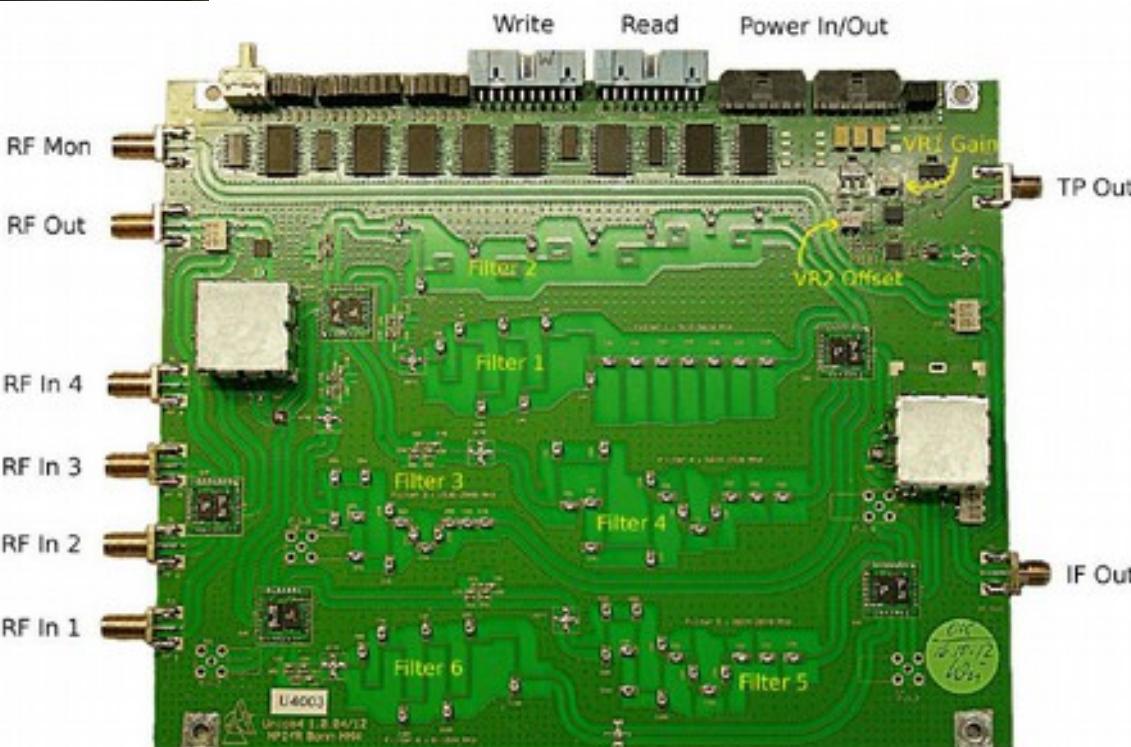
1. Analog Conditioning Module – CoMo
2. Analog-Digital Converter (ADB1 / ADB2)
3. Data Processing (Core2)
4. Connection and Service
(FiLaIN/OUT – FiLa10G FILA10G-4)
5. Timing and Clock (CaT2 – Clock and Timing)
6. Computer Control (PCSet)

1. Conditioning Module (Unica3)



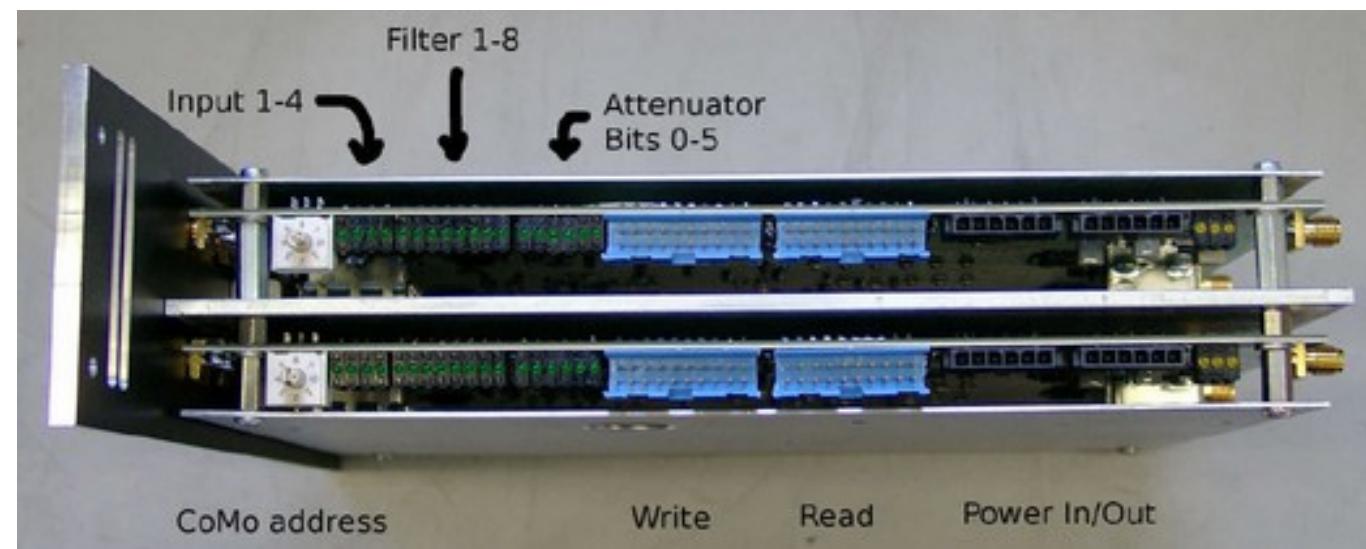
- 4 selectable RF inputs
- 4 selectable Nyquist filters
- 31.5 dB programmable attenuation
- Total power full band
- Manual or automatic gain control

1. Conditioning Module (Unica4)



- Now with:
8 selectable Nyquist filters

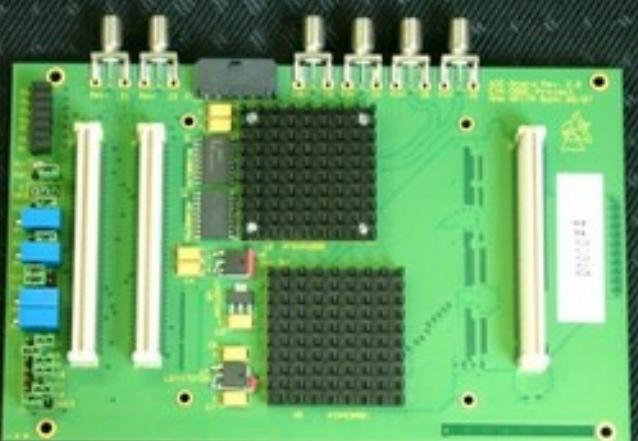
- 2 Unica boards build 1 CoMo



2. Analog to digital converter ADB1/2



- Analog input: 0 - 2.2 GHz
- Max Sampling clock 1.5 GHz
- Max Instantaneous bandwidth 750 MHz (real) / 1.5 GHz (complex)
- Output data 2 x 8-bit @1/4 Sclk DDR



- Analog input: 0 – 3.5 GHz
- Max sampling clock 2.2 GHz
- Max instantaneous bandwidth 1.1 GHz (real) / 2.2 GHz (complex)
- Output data 2 x 8-bit @1/4 Sclk DDR
4 x 8-bit @1/8 Sclk DDR
- Piggy pack module support for 10-bit output and connection to Fila10G

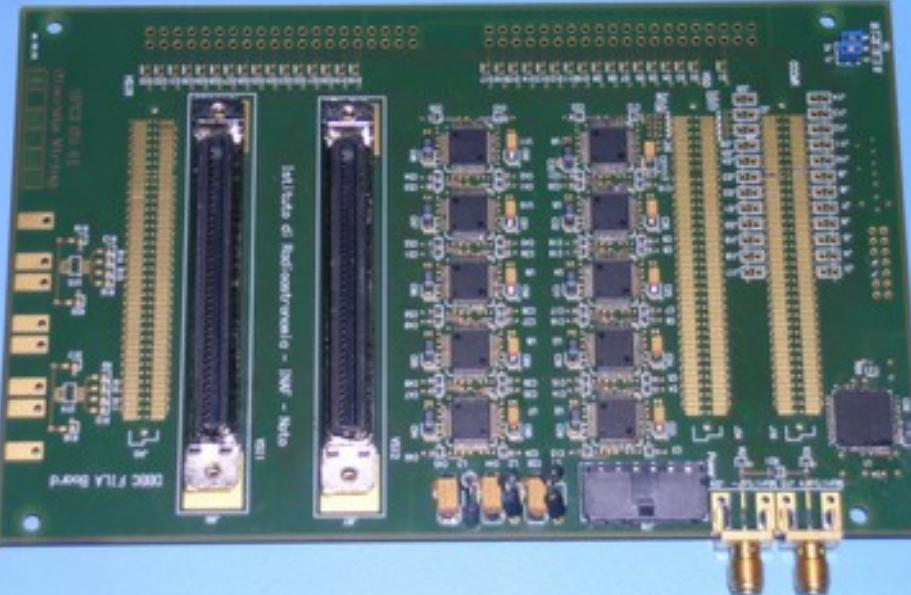


3. Basic processing unit - Core2



- Input rate:
(4 IF x 2 bus x 8-bit x SClk/4 DDR) b/s
(2 IF x 4 bus x 8-bit x SClk/8 DDR) b/s
....
- Typical output rate:
(64 ch x 32-64-128) Mb/s
- Programmable architecture
 - Digital down conversion (DDC)
1 Core2 = 4 BBCs
 - Poly-phase Filter Bank (PFB)
1 Core2 = 16 Poly-phase f lters
- 1 VSI 32 channel output

4. Connection and service - FiLaBoard

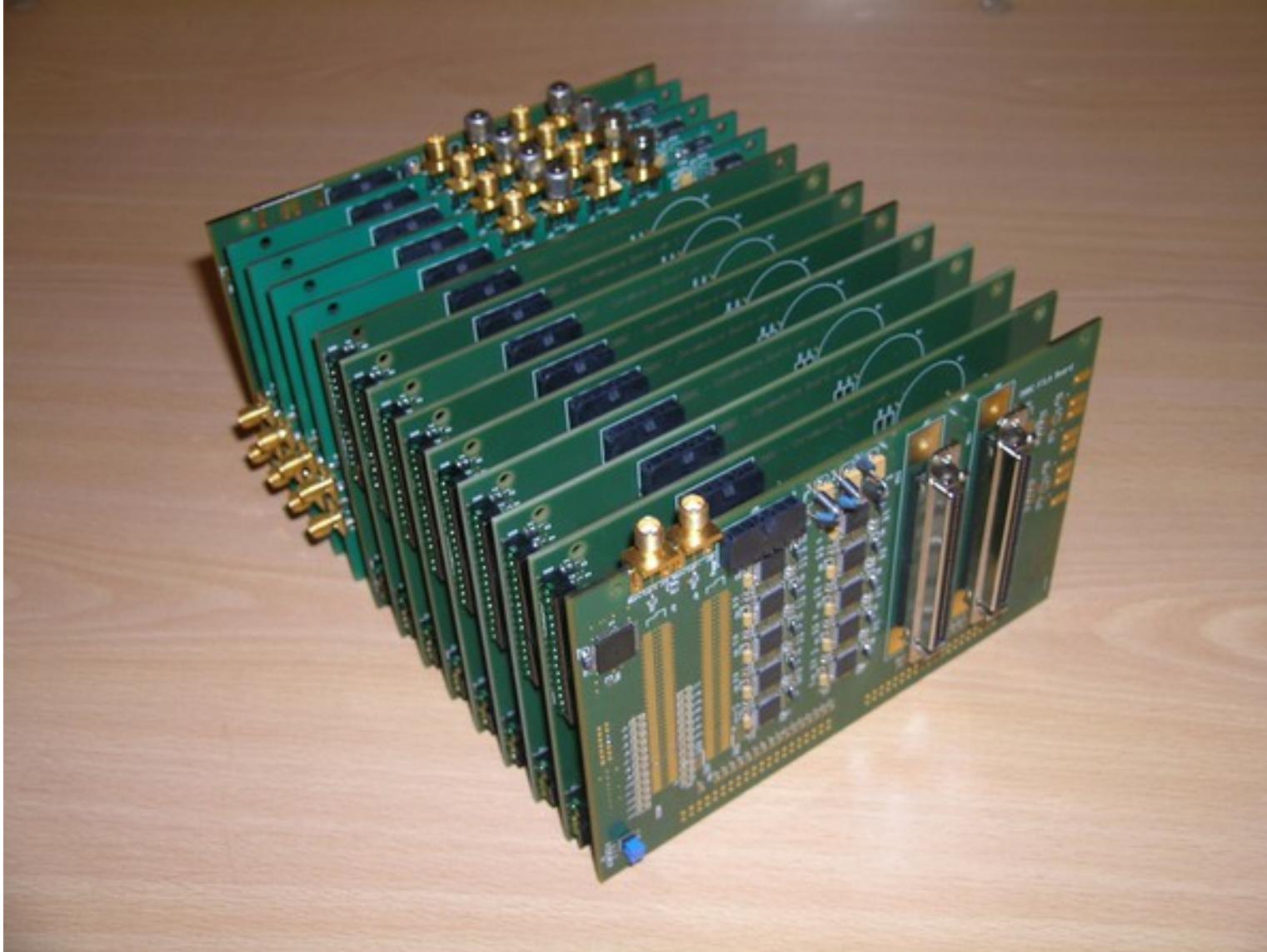


First and Last board in the stack

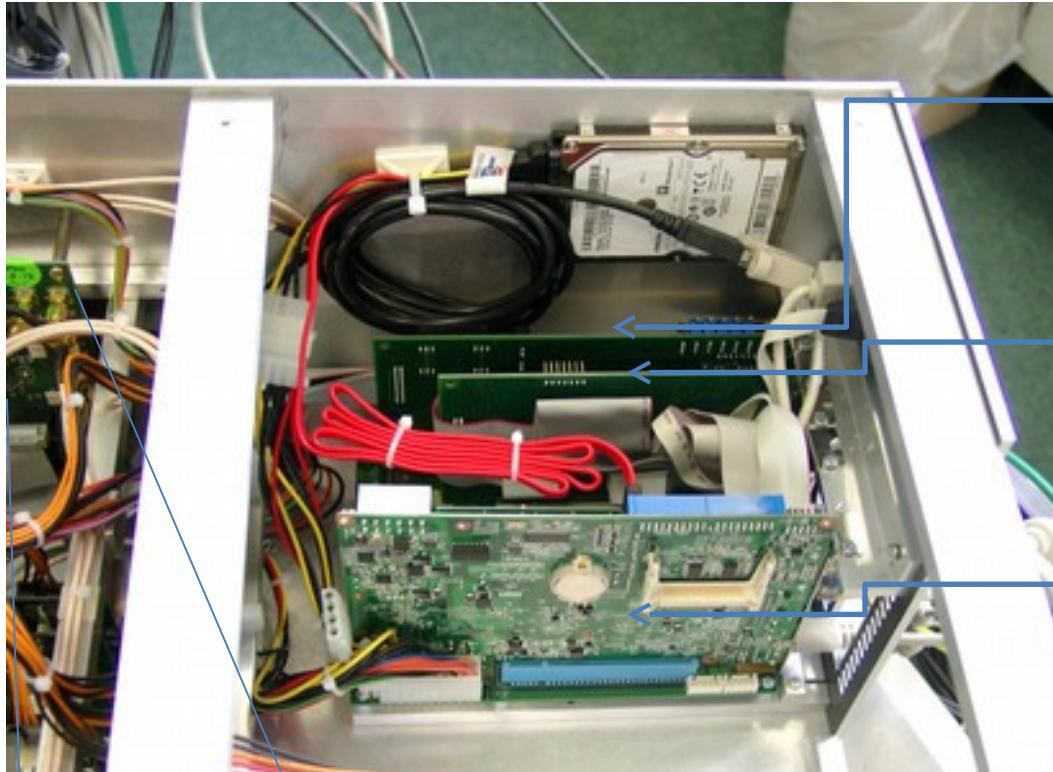
- First: IN
 - Communication interface
 - JTAG programming channel
 - 1pps in
- Last: OUT
 - 2 VSI interfaces
 - 1pps monitor out
 - 80 Hz continues calibration out



Complete Module Stack



6. PC Set – Control computer



ADLink PCI9111HR:
Communication with Conditioning Modules
for IF total power measure, automatic gain
control, registers control, etc.

ADLink PCI7200:
Communication with 32-bit bus for Core2
register setting, total power measurement,
state statistics, etc.

Adventech PCI-7030:
Half Size PCI Motherboard (Intel Atom)
on PCI backplane

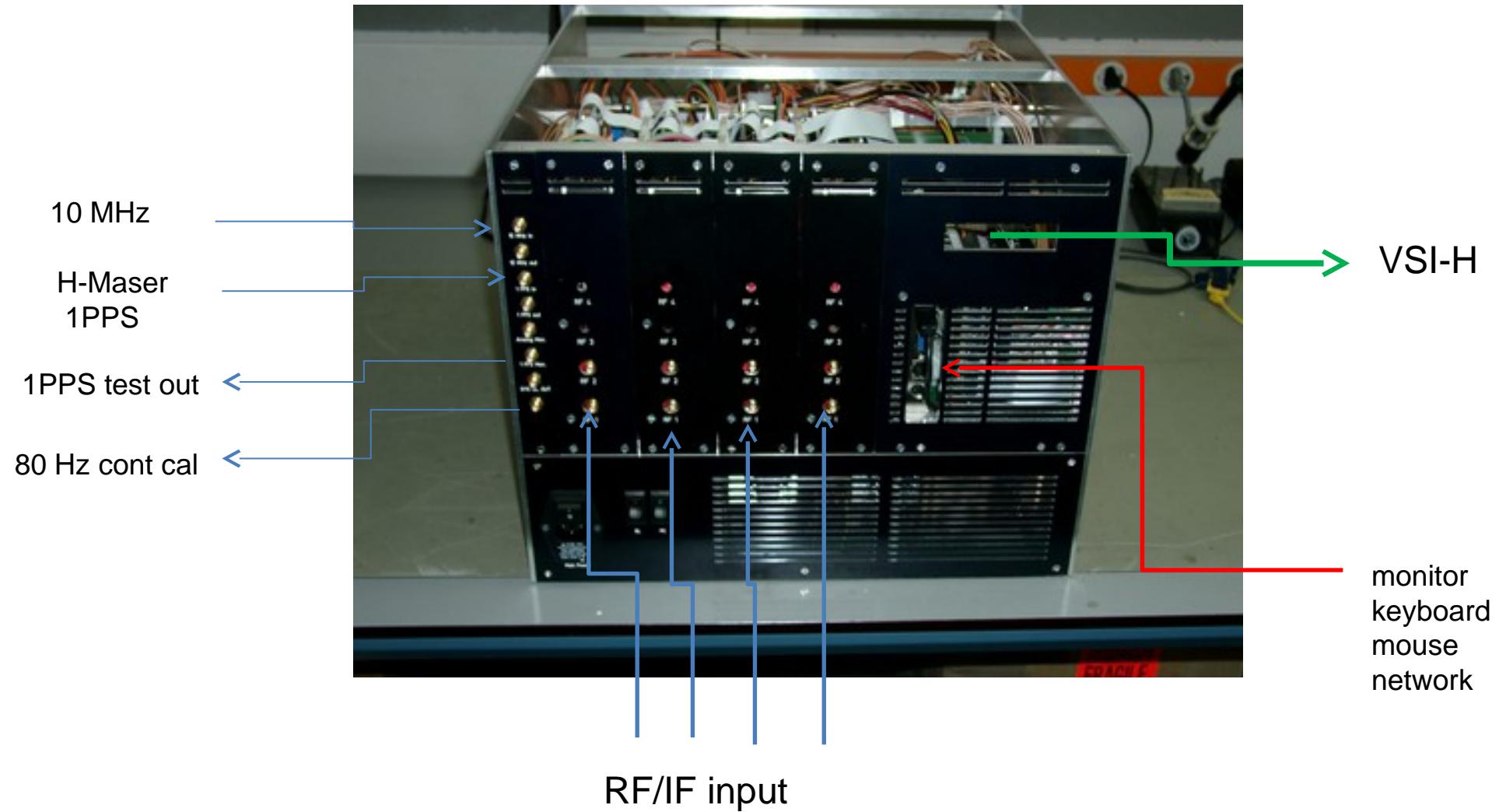


Xilinx programmer:
FPGA device configuration
through USB – JTAG interface



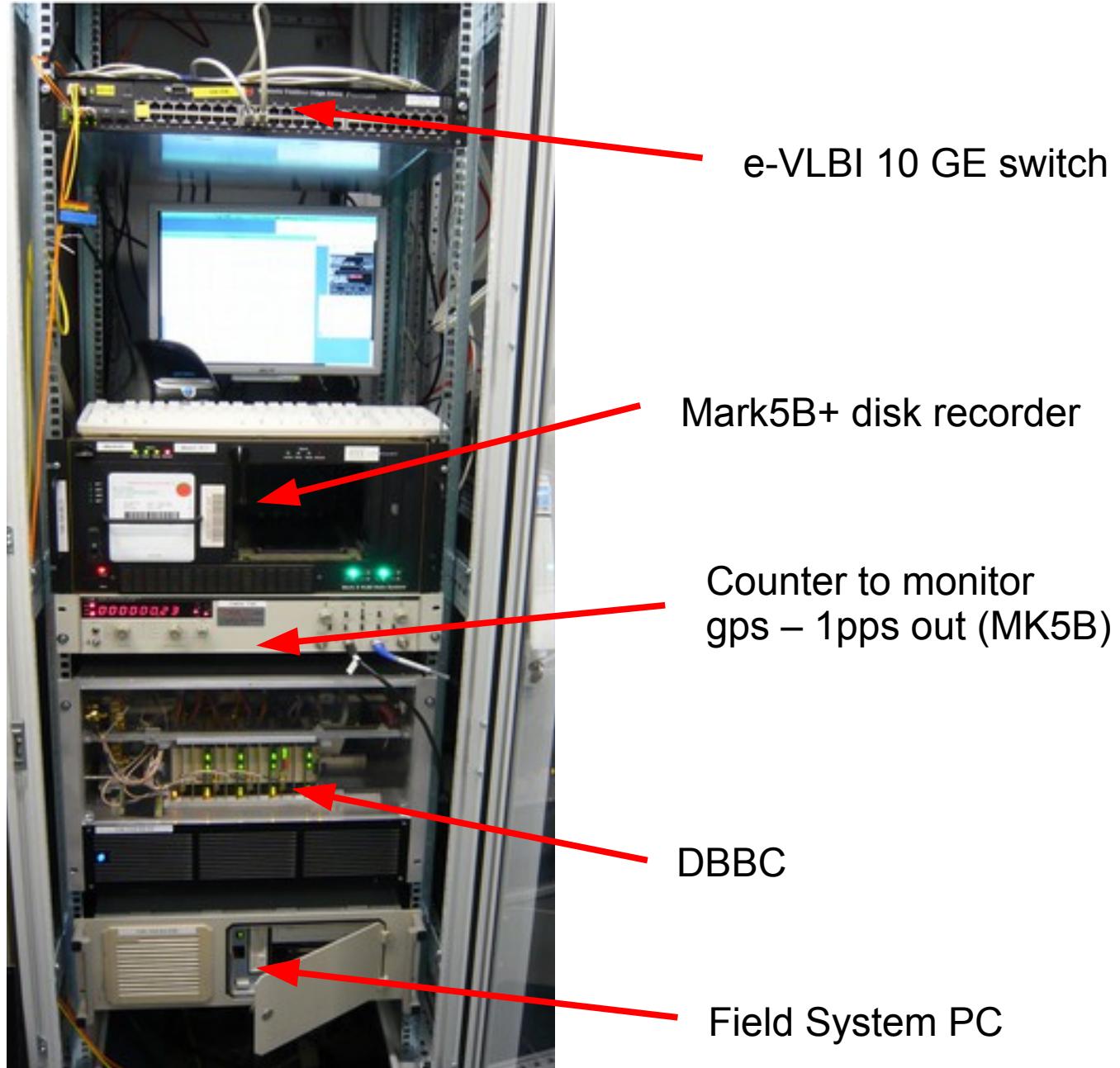
Installation of a DBBC

How to connect the DBBC

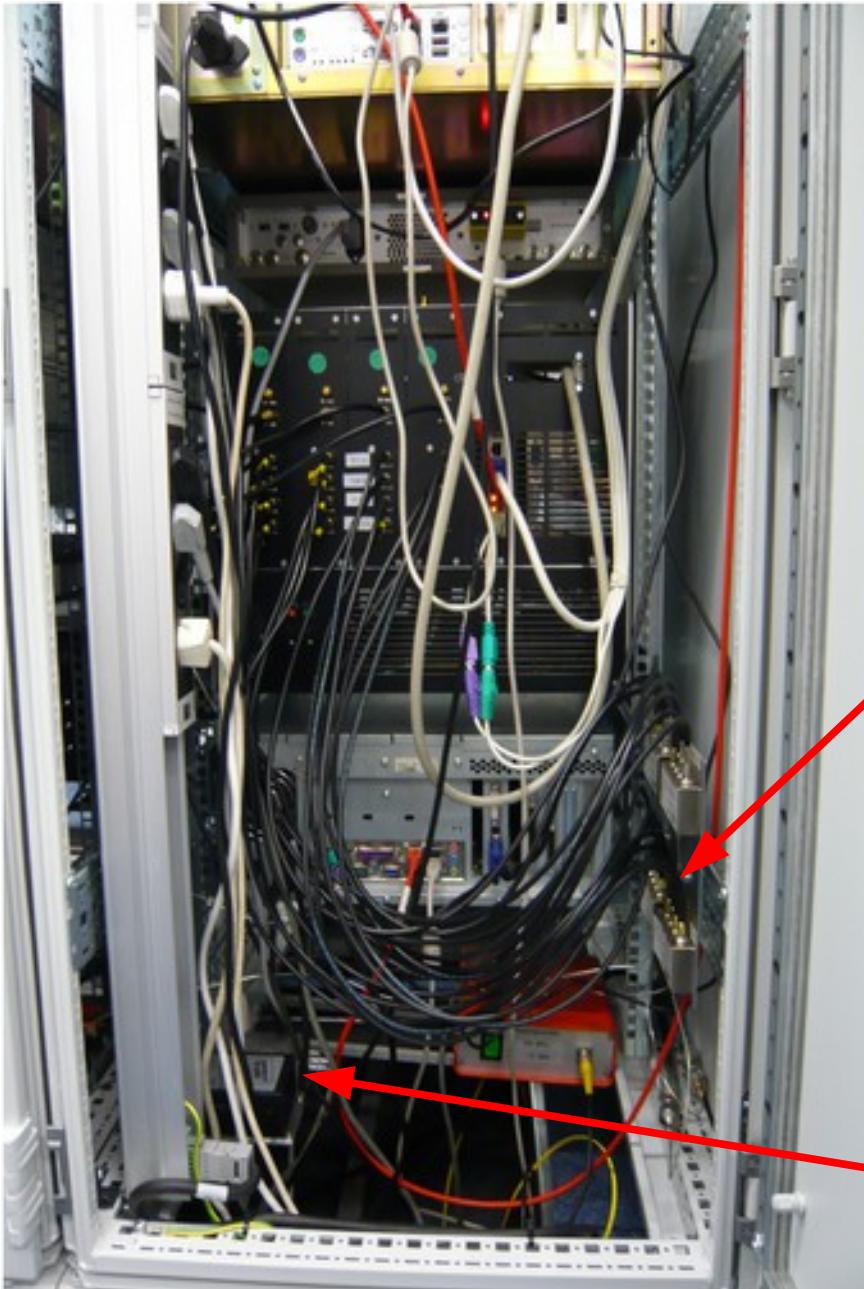




Installation of a DBBC



Installation of a DBBC



4x4 IF-Splitter to provide all possible IFs at the DBBC Inputs:

- IF1: a. 500-1000 IF RCP
- b. 0-500 IF RCP
- c. 500-1000 IF LCP
- d. 0-500 IF LCP

- IF2: a. 500-1000 IF RCP
- b. 0-500 IF RCP
- c. 500-1000 IF LCP
- d. 0-500 IF LCP

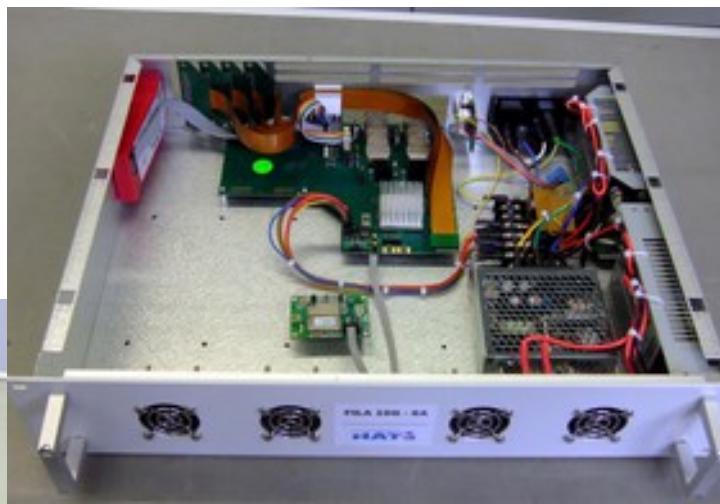
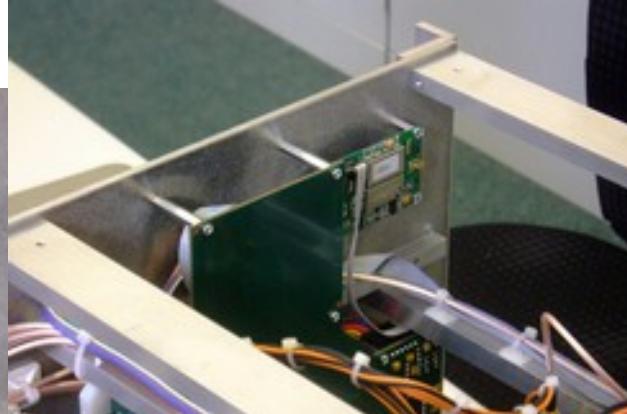
- IF3: a. 500-1000 IF RCP
- b. 0-500 IF RCP
- c. 500-1000 IF LCP
- d. 0-500 IF LCP

- IF4: a. 500-1000 IF RCP
- b. 0-500 IF RCP
- c. 500-1000 IF LCP
- d. 0-500 IF LCP

blank – sync generation from 80 Hz



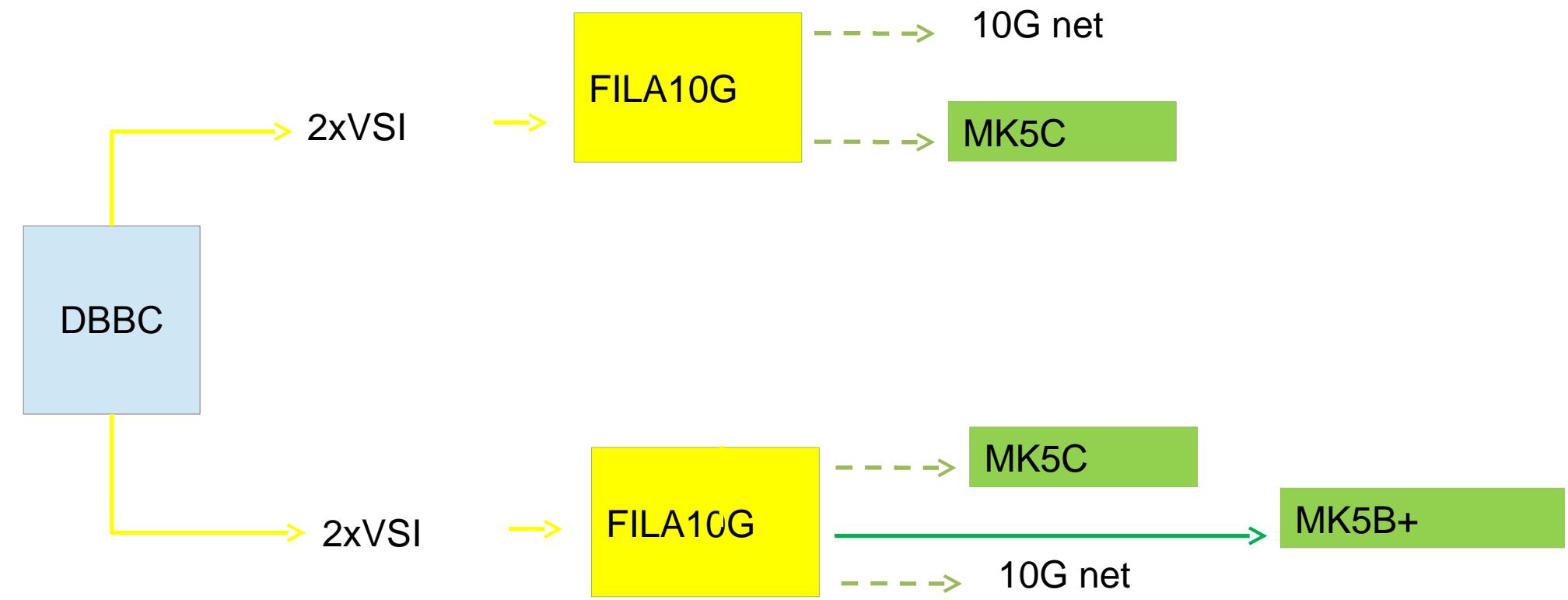
FiLa10G (SA)



- Two independent 10G Ethernet UDP port
- Physical interface optical XFP
- 10G port fully bidirectional
- Installed inside the DBBC box or as stand-alone
- Data rate: 1 – 2 – 4 Gbps each 10G port
- Format mode: RAW, MK5B or VDIF



Connection examples





FiLa10G Software

- FILA10G Files:

- c:\DBBC\bin\timesyncFILA10G.exe (MK5B time set)
- c:\DBBC\bin\vdif_timesyncFILA10G.exe (VDIF time set)
- c:\DBBC\bin\sendstr.exe (serial communication)
- c:\DBBC_conf\FilesDBBC\fila10g_v3.3.1.bit
- c:\DBBC\doc\DBBC2 FILA10G Command set v3.3.1.pdf

Note: a program to sync with a NTP server is required
(eg. NetTimeSetup-314.exe) or new FiLa10G modules
have a GPS module build in that can be used to get the
GPS time.



Setting up the FiLa10G

- Upload of the firmware is
 - automatically made by the DDC/PFB control software (internal FiLa10G)
 - done with an additional Xilinx JTAG programmer using a script for IMAPCT (external FiLa10G-SA)
- Communication is through serial port or Ethernet in the stand-alone version
- Commands available (see document)
- VDIF packet size setting (see document)
- Script files can be used for block of commands (see batch)



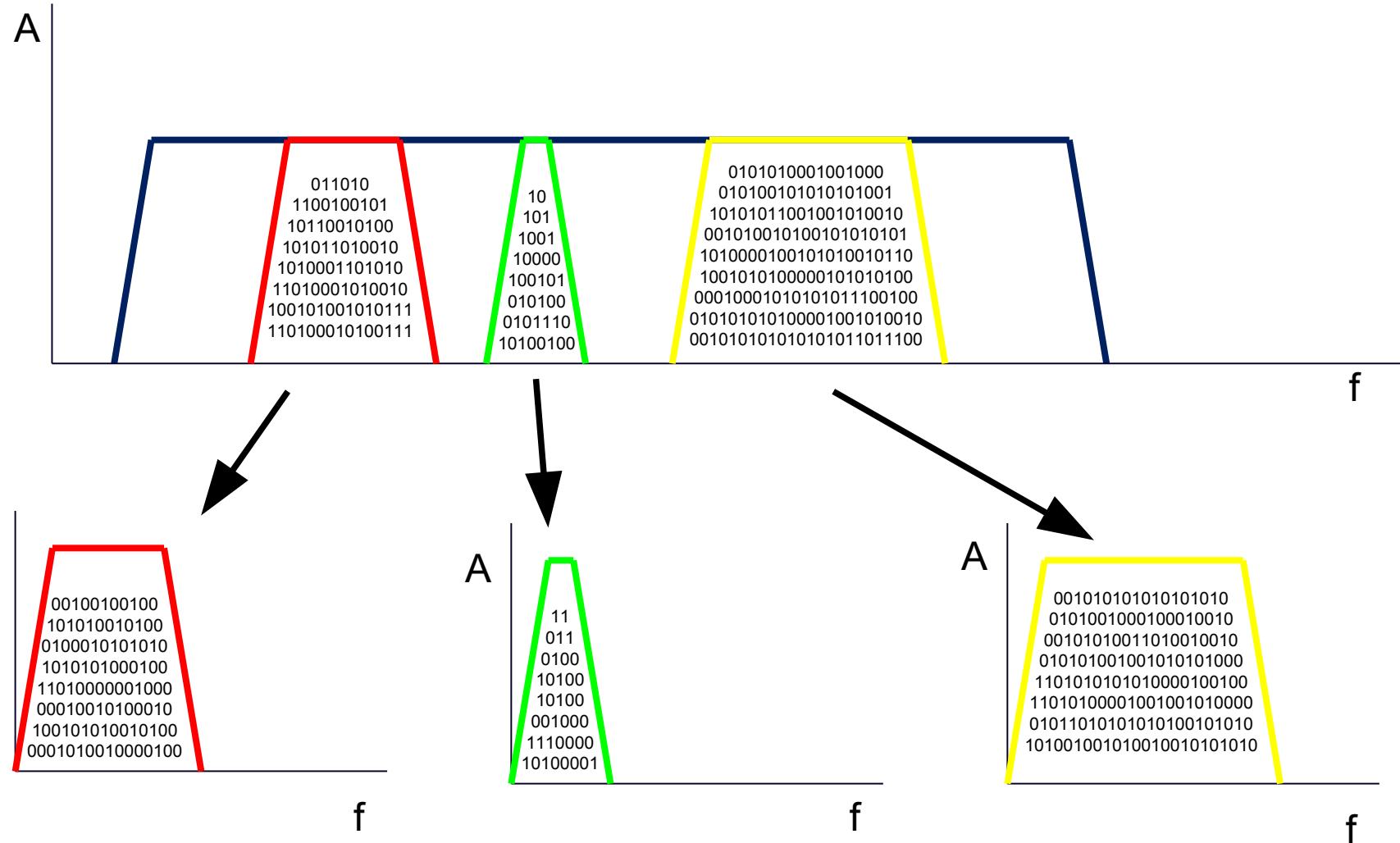
Observing modes

- DDC: tunable, channel bandwidth between 1 MHz and 16 MHz, U&L, Continuous cal with 80 Hz synchronization, modes: geo, astro, astro2, w-astro, lba, test
DDC-E: like DDC but bandwidth up to 32 MHz (astro3)
- PFB: fixed tuning, channel bandwidth 32/64 MHz, all U or L depending on the Nyquist zone
- DSC: full $4 \times 512/1024$ MHz, max 8×1024 MHz band direct sampling conversion, all U or L depending on the Nyquist zone
- SPECTRA: 4Kch/IF spectrometer, max 32K channels



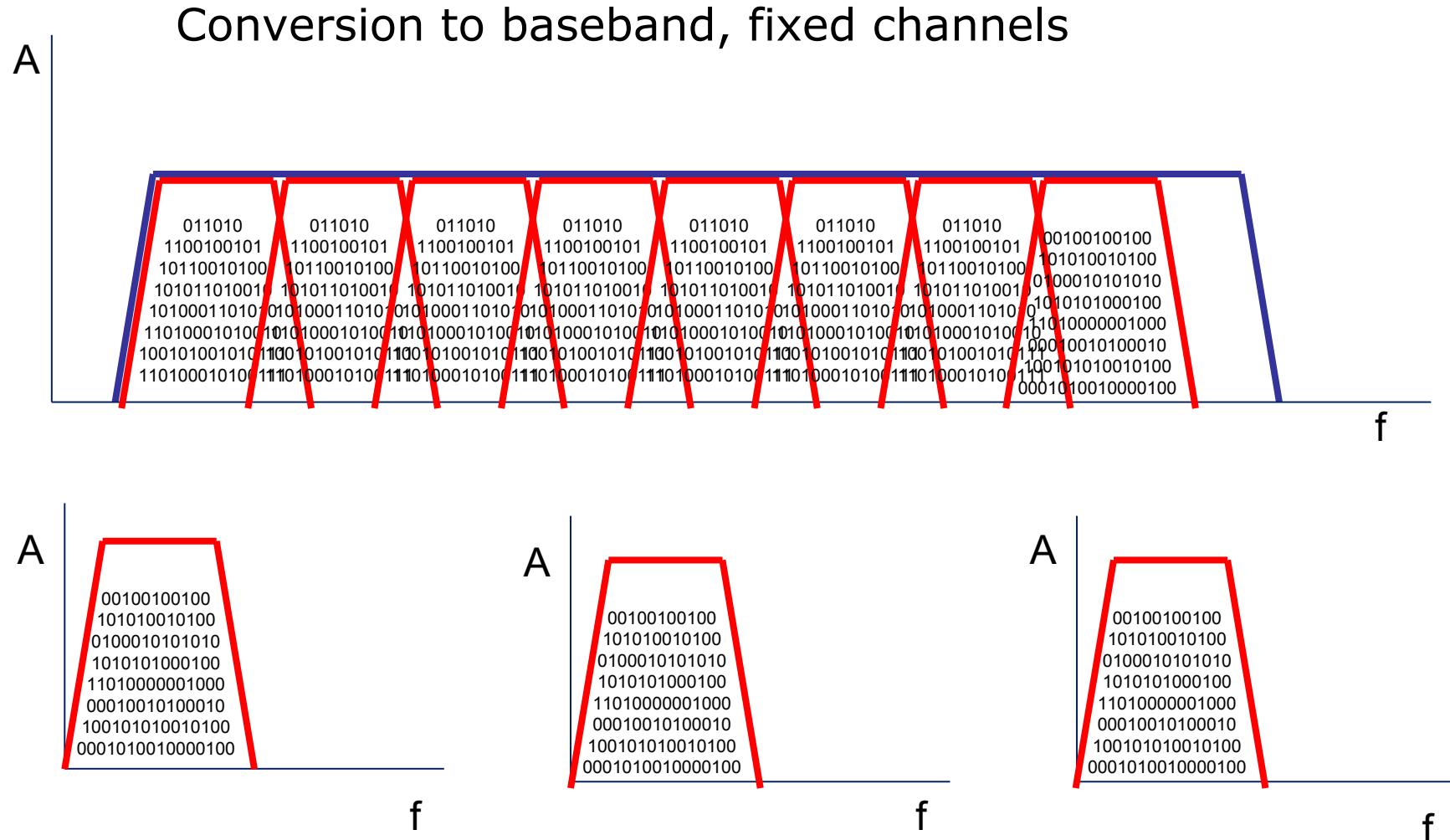
DDC – digital down conversion

Conversion to baseband, tunable channels of variable bandwidth



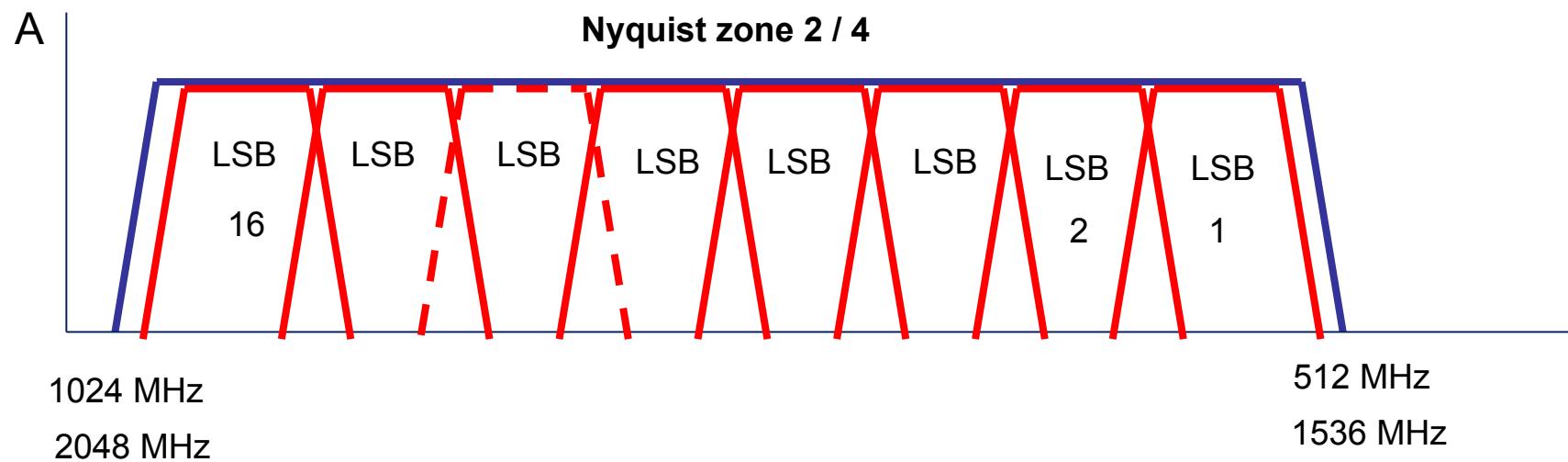
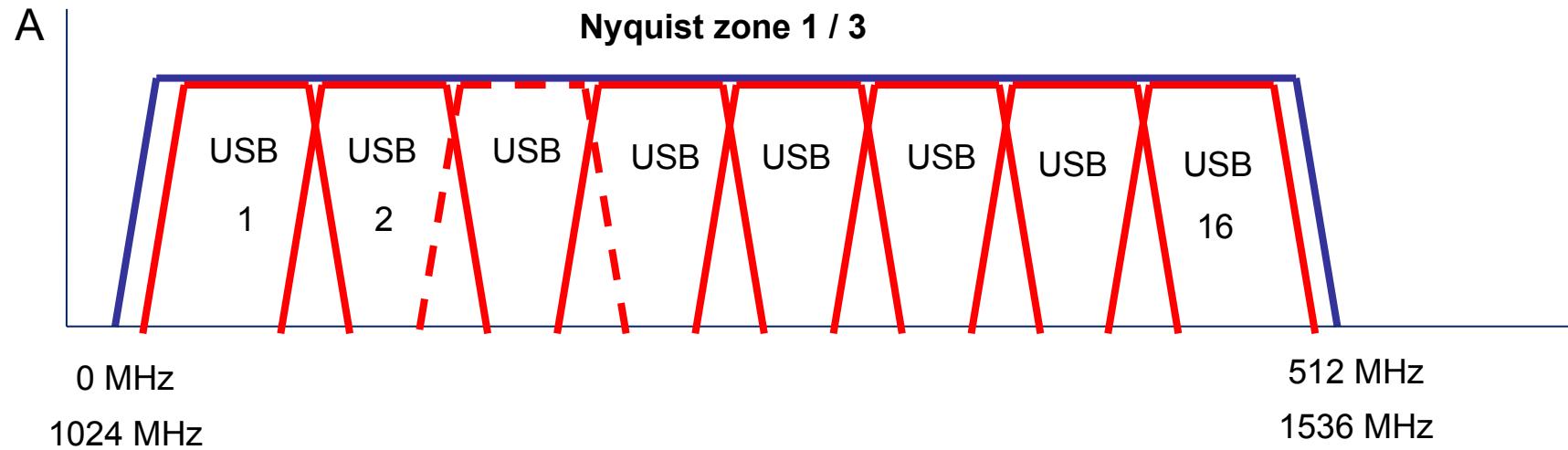


PFB – poly-phase filter bank





PFB – poly-phase filter bank





Software

How the observing mode is selected

- Using a dedicated firmware
- Using a dedicated control software
- Using a dedicated configuration text file

Software (Windows XP)

Files Structure:

C:\DBBC\bin

→ control software

C:\DBBC\doc

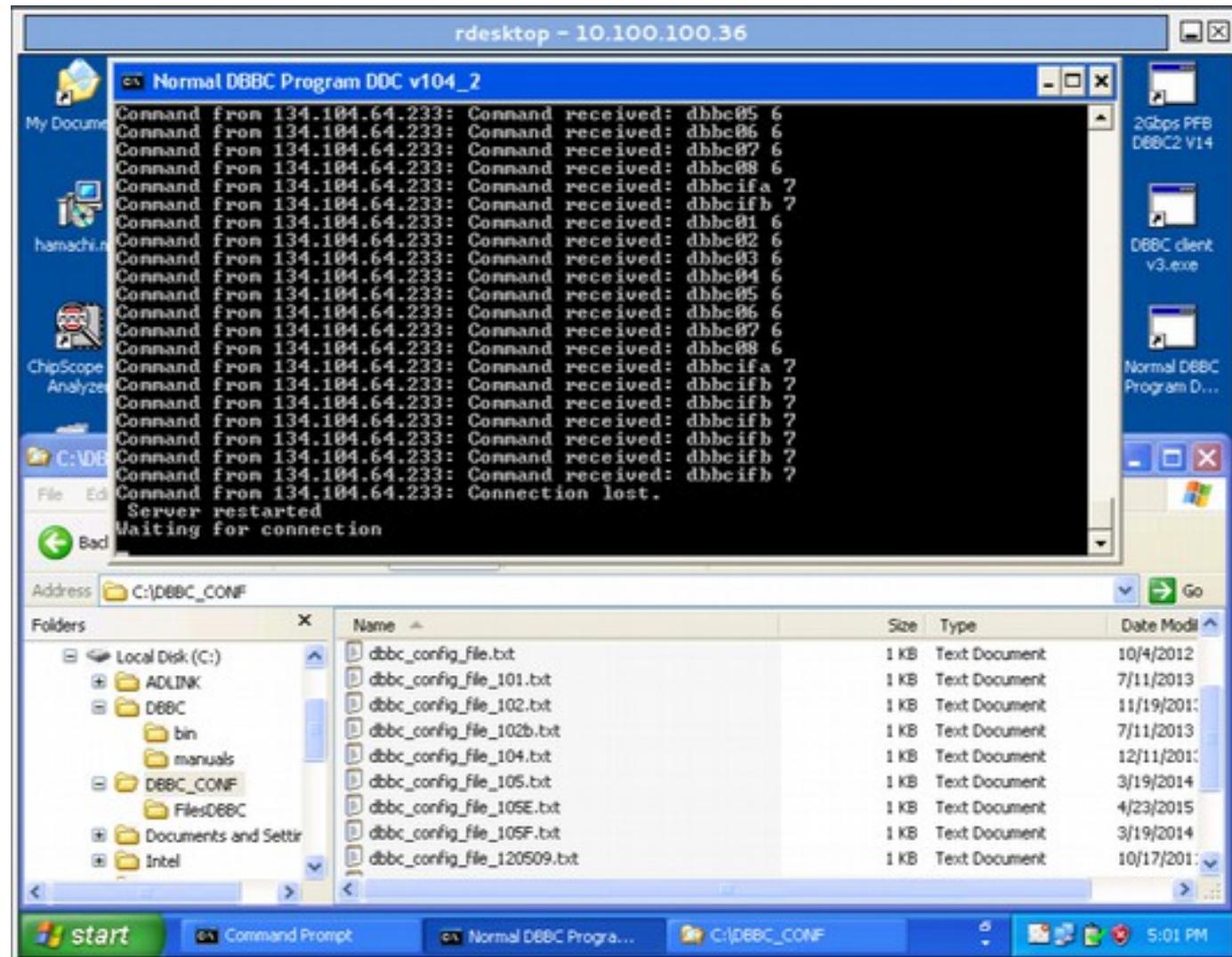
→ manuals

C:\DBBC_CONF\

→ configuration text files

C:\DBBC_CONF\FilesDBBC

→ firmware





Main Menu

- Home
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Menu utente

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Home > Support

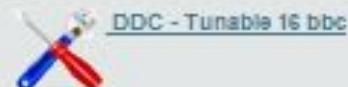
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Overview

Page: 1 of 1

Number of Categories: 6

[DDC - Tunable 16 BBC](#)

Files: 4

[BASE - General](#)

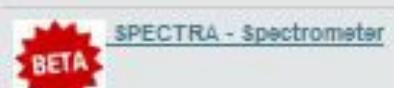
Files: 4

[FILA10G - 10G Ethernet](#)

Files: 2

[PFB - Polyphase 16 bands](#)

Files: 3

[SPECTRA - Spectrometer](#)

Files: 1

[Technical Notes](#)

Files: 10

search...



Software

- General:

BASE Package

c:\DBBC\bin\DBBC client v3.exe (general client)

c:\DBBC\bin\clock1024.exe (CAT2 1024)

c:\DBBC\bin\clock2048.exe (CAT2 2048)

c:\DBBC\bin\ad9858.exe (CAT1)

c:\DBBC\bin\power.exe (on-off hardware)

c:\DBBC\bin\agc_if.exe (CoMo Unica3 test)

c:\DBBC\bin\agc_if_unica4.exe (CoMo Unica4 test)



Software

- DDC:

c:\DBBC\bin\DBBC2 Control DDC v104.exe (server)
c:\DBBC_conf\dbbc_config_file_104.txt
c:\DBBC_conf\FilesDBBC\dbbc2_ddc_v104.bit
c:\DBBC\doc\DBBC2 DDC command set v104.pdf

- PFB:

c:\DBBC\bin\DBBC2 Control PFB v15.exe (server)
c:\DBBC_conf\dbbc_poly_config_file_15.txt
c:\DBBC_conf\FilesDBBC\dbbc2_pfb_v15.bit
c:\DBBC\doc\DBBC2 PFB command set v15.pdf



DDC configuration file

c:\DBBC_conf\dbbc_config_file_104.txt

Example:

```

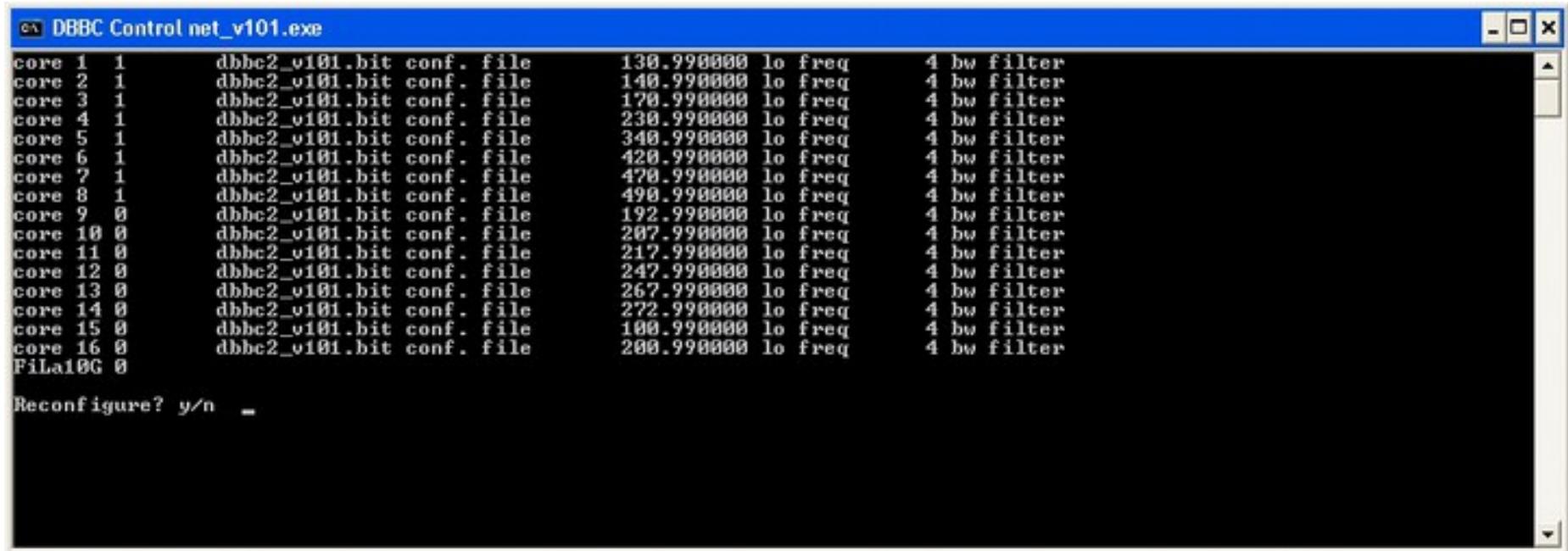
1 dbbc2_ddc_v104.bit 597.00 8 ←the first number is indication of ADB1|2, in this case ADB1 is on
1 dbbc2_ddc_v104.bit 682.00 8 IFA and ADB2 on IFB, ADB1 in IFC, no Core2 for IFD
1 dbbc2_ddc_v104.bit 853.00 8 If no Core2 is inserted in the first and second column put 0.
1 dbbc2_ddc_v104.bit 938.00 8 The second parameter is the firmware file name to be used.
2 dbbc2_ddc_v104.bit 597.00 8 The third and fourth parameters are frequency and bandwidth respectively.
2 dbbc2_ddc_v104.bit 682.00 8
2 dbbc2_ddc_v104.bit 853.00 8
2 dbbc2_ddc_v104.bit 938.00 8
1 dbbc2_ddc_v104.bit 597.00 8
1 dbbc2_ddc_v104.bit 682.00 8
1 dbbc2_ddc_v104.bit 853.00 8
1 dbbc2_ddc_v104.bit 938.00 8
0 dbbc2_ddc_v104.bit 597.00 8 Each Core2 board supports 4 bbcs so if not present 0 has to be inserted in
0 dbbc2_ddc_v104.bit 682.00 8 four lines
0 dbbc2_ddc_v104.bit 853.00 8
0 dbbc2_ddc_v104.bit 938.00 8
1 fla10g_v2_1.bit ← if a FILA10G is installed set 1st version 1 (with ACE), 2nd version (without ACE) 2, otherwise 0
1 38000 ← no unica=0 unica3=1, unica4=2, initial CoMos target values for IFA
1 38000 ← no unica=0 unica3=1, unica4=2, initial CoMos target values for IFB
1 38000 ← no unica=0 unica3=1, unica4=2, initial CoMos target values for IFC
1 38000 ← no unica=0 unica3=1, unica4=2, initial CoMos target values for IFD
0 38000 ← no unica=0 unica3=1, unica4=2, initial CoMos target values for IFE
0 38000 ← no unica=0 unica3=1, unica4=2, initial CoMos target values for IFF
0 38000 ← no unica=0 unica3=1, unica4=2, initial CoMos target values for IFG
0 38000 ← no unica=0 unica3=1, unica4=2, initial CoMos target values for IFH
107 112 0 0 ← phase calibration values
CAT2 1024 ← CAT1|2 and sampling frequency

```



Starting the software

DDC: running DBBC2 Control DDC v104.exe



```
DBBC Control net_v101.exe

core 1 1      dbbc2_v101.bit conf. file    130.990000 lo freq   4 bw filter
core 2 1      dbbc2_v101.bit conf. file    140.990000 lo freq   4 bw filter
core 3 1      dbbc2_v101.bit conf. file    170.990000 lo freq   4 bw filter
core 4 1      dbbc2_v101.bit conf. file    230.990000 lo freq   4 bw filter
core 5 1      dbbc2_v101.bit conf. file    340.990000 lo freq   4 bw filter
core 6 1      dbbc2_v101.bit conf. file    420.990000 lo freq   4 bw filter
core 7 1      dbbc2_v101.bit conf. file    470.990000 lo freq   4 bw filter
core 8 1      dbbc2_v101.bit conf. file    490.990000 lo freq   4 bw filter
core 9 0      dbbc2_v101.bit conf. file    192.990000 lo freq   4 bw filter
core 10 0     dbbc2_v101.bit conf. file    207.990000 lo freq   4 bw filter
core 11 0     dbbc2_v101.bit conf. file    217.990000 lo freq   4 bw filter
core 12 0     dbbc2_v101.bit conf. file    247.990000 lo freq   4 bw filter
core 13 0     dbbc2_v101.bit conf. file    267.990000 lo freq   4 bw filter
core 14 0     dbbc2_v101.bit conf. file    272.990000 lo freq   4 bw filter
core 15 0     dbbc2_v101.bit conf. file    100.990000 lo freq   4 bw filter
core 16 0     dbbc2_v101.bit conf. file    200.990000 lo freq   4 bw filter
FilA10G 0

Reconfigure? y/n -
```

after the Core2 configuration is completed

then run a client ex. **DBBC Client v3.exe or Field System**

**DDC Mode Commands and Form
Table (see documents)**



First tests with the DBBC

- Cabling the DBBC: IF, 1pps, 10 MHz, (80 Hz calibration?)
- Starting the DDC software (server) on the DBBC Windows PC
 - Newest version always available at <http://www.hat-lab.com/hatlab/support> currently v104_2 or v105 for DDC
- Configuration file needs to be edit for your hardware installation.

First functionality can be tested with the DBBC_client or from the FS:

- select different IF inputs for the ADBs and let AGC adjustment work, e.g.

```
> dbbcifa          # for query  
> dbbcifa=2,agc,2 # to set RF input 2, agc on, IF filter 2 (0-500 MHz)
```

read out BBCs set different frequencies, ...

```
> dbbc01          # for query  
> dbbc01=596.00,a,16.00 # to set BBC freq=596 MHz, IFA, BBC  
                           band width = 16 MHz
```



First tests with the DBBC

```
> dbbcifa      # for query  
> dbbcifa=2,agc,2 # to set RF input 2, agc on, IF filter 2 (0-500 MHz)
```

read out BBCs set different frequencies, ...

```
> dbbc01      # for query  
> dbbc01=596.00,a,16.00 # to set BBC freq=596 MHz, IFA, BBC  
band width = 16 MHz
```

```
DBBC client v3.exe  
Enter Command: dbbcifa  
Received from DBBC: dbbcifa/2,0,agc,2,0,38000  
Enter Command: dbbcifa  
Received from DBBC: dbbcifa/2,0,agc,2,0,38000  
Enter Command: dbbcifb  
Received from DBBC: dbbcifb/3,0,agc,1,0,38000  
Enter Command: dbbcifc  
Received from DBBC: dbbcifc/4,0,agc,2,0,38000  
Enter Command: dbbc01  
Received from DBBC: dbbc01/124.490000,a,8,1,agc,255,255,4639,4486,4644,4492  
Enter Command: dbbc02  
Received from DBBC: dbbc02/140.490000,a,8,1,agc,255,255,5140,4758,5117,4745  
Enter Command: dbbcifb=2,agc,2  
Received from DBBC: dbbcifb/2,0,agc,2,0,38000  
Enter Command: dbbcifb  
Received from DBBC: dbbcifb/2,0,agc,2,0,38000  
Enter Command: _
```



Connecting a Mark5B(+)

Connect the DBBC VSI1 port to the Mark5B using VSI cable.

Set Mark5B needs to be synced to the 1pps on the VSI cable.

```
tstDIM > clock_set=32:ext
```

```
tstDIM > 1pps_source=vsi
```

```
tstDIM > dot_set=:force
```

```
tstDIM > dot?           # query several times to see if it stays synced
```

Test the quality of the connection

```
DBBC > dbbcform=test,tvg      # starts TVG on the DBBC
```

```
tstDIM > tvr=0xffffffff      # TVR LED should be green.
```

If it is not green it might help to carefully disconnect and reconnect the VSI cable on both ends, sometimes cleaning the connectors with dry air is required.



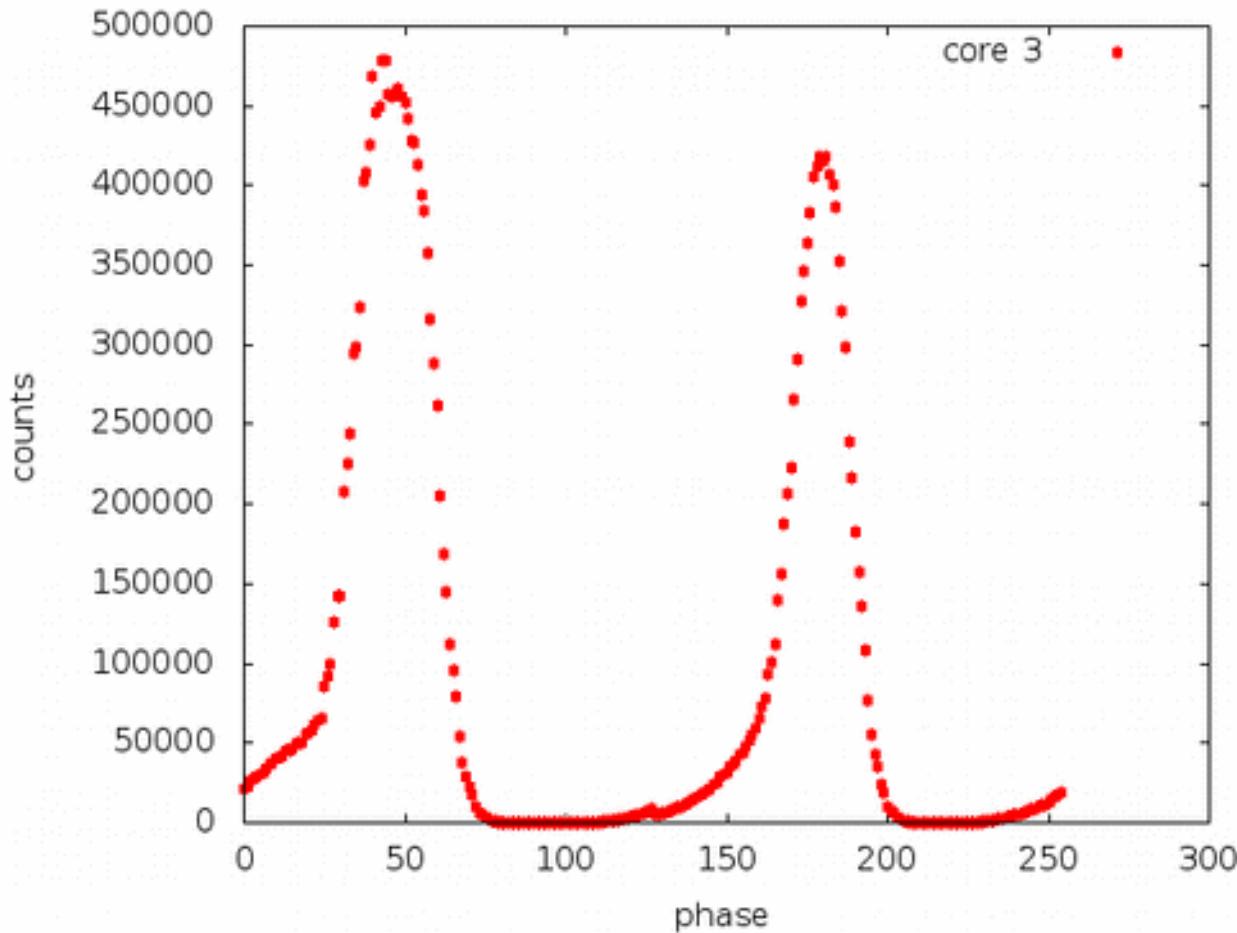
Calibration of the DBBC

Calibration or phase optimization is required at the system installation and has to be repeated after a hardware modification in the stack, transportation, or a new firmware. Periodically as a general check.

- Connect a synthesizer tuned to 764 MHz to all IFs.
- Load the firmware to test.
- Point all dbbcifa,b,c,d to this input
- Run the DBBC command: calibration=all
- ... wait



Calibration of the DBBC



...
252 106 3959 16276 10431
253 135 5588 17455 10729
254 161 5276 18712 11039
255

minM1 00050 ele1 **107** minM2 00050 ele2 **79** minM3 00049 ele3 **92** minM4 00051 ele4 **224**

| | | | | | |
|-----|--------|-----|--------|-------|--|
| ... | | | | | |
| 60 | 270437 | 872 | 261803 | 16988 | |
| 61 | 285347 | 653 | 205494 | 12851 | |
| 62 | 289611 | 395 | 169170 | 10302 | |
| 63 | 301585 | 352 | 144859 | 7090 | |
| 64 | 309365 | 169 | 111552 | 3386 | |
| 65 | 317749 | 102 | 95884 | 2313 | |
| 66 | 322930 | 79 | 79745 | 1817 | |
| 67 | 339064 | 67 | 54644 | 1305 | |
| 68 | 332014 | 57 | 37490 | 881 | |
| 69 | 338031 | 55 | 28940 | 526 | |
| 70 | 324313 | 54 | 22799 | 296 | |
| 71 | 320547 | 52 | 17611 | 223 | |
| 72 | 310049 | 51 | 10504 | 187 | |
| 73 | 276350 | 51 | 6440 | 148 | |
| 74 | 260401 | 51 | 4751 | 106 | |
| 75 | 251864 | 51 | 3334 | 84 | |
| 76 | 204246 | 51 | 2061 | 76 | |
| 77 | 169837 | 51 | 1407 | 60 | |
| 78 | 149612 | 51 | 1155 | 56 | |
| 79 | 97942 | 51 | 361 | 54 | |
| 80 | 74886 | 51 | 228 | 53 | |
| 81 | 55966 | 50 | 130 | 53 | |
| 82 | 46097 | 51 | 113 | 53 | |
| 83 | 28929 | 51 | 80 | 53 | |
| 84 | 21030 | 53 | 69 | 52 | |
| 85 | 7957 | 55 | 59 | 52 | |
| 86 | 5530 | 55 | 51 | 52 | |
| 87 | 2958 | 57 | 51 | 52 | |
| 88 | 2078 | 61 | 50 | 52 | |
| 89 | 1368 | 80 | 50 | 52 | |
| 90 | 734 | 79 | 50 | 52 | |
| 91 | 247 | 117 | 50 | 52 | |
| ... | | | | | |



DDC configuration file

c:\DBBC_conf\dbbc_config_file_104.txt

Example:

```
1 dbbc2_ddc_v104.bit 597.00 8 ←the first number is indication of ADB1|2, in this case ADB1 is on
1 dbbc2_ddc_v104.bit 682.00 8     IFA and ADB2 on IFB, ADB1 in IFC, no Core2 for IFD
1 dbbc2_ddc_v104.bit 853.00 8     If no Core2 is inserted in the first and second column put 0.
1 dbbc2_ddc_v104.bit 938.00 8     The second parameter is the firmware file name to be used.
1 dbbc2_ddc_v104.bit 597.00 8     The third and fourth parameters are frequency and bandwidth respectively.
1 dbbc2_ddc_v104.bit 682.00 8
1 dbbc2_ddc_v104.bit 853.00 8
1 dbbc2_ddc_v104.bit 938.00 8
1 dbbc2_ddc_v104.bit 597.00 8
1 dbbc2_ddc_v104.bit 682.00 8
1 dbbc2_ddc_v104.bit 853.00 8
1 dbbc2_ddc_v104.bit 938.00 8
1 dbbc2_ddc_v104.bit 597.00 8     Each Core2 board supports 4 bpcs so if not present 0 has to be inserted in
1 dbbc2_ddc_v104.bit 682.00 8     four lines
1 dbbc2_ddc_v104.bit 853.00 8
1 dbbc2_ddc_v104.bit 938.00 8
0 fla10g_v2_1.bit ← if a FILA10G is installed set 1st version 1 (with ACE), 2nd version (without ACE 2), otherwise 0
1 38000                         ← no unica=0 unica3=1, unica4=2, initial CoMos target values for IFA
1 38000                         ← no unica=0 unica3=1, unica4=2, initial CoMos target values for IFB
1 38000                         ← no unica=0 unica3=1, unica4=2, initial CoMos target values for IFC
1 38000                         ← no unica=0 unica3=1, unica4=2, initial CoMos target values for IFD
0 38000                         ← no unica=0 unica3=1, unica4=2, initial CoMos target values for IFE
0 38000                         ← no unica=0 unica3=1, unica4=2, initial CoMos target values for IFF
0 38000                         ← no unica=0 unica3=1, unica4=2, initial CoMos target values for IFG
0 38000                         ← no unica=0 unica3=1, unica4=2, initial CoMos target values for IFH
107 79 92 224                  ← phase calibration values
CAT2 1024                       ← CAT1|2 and sampling frequency
```



Test recordings

- Test recordings are good to control the correct sampling (bit statistics), band pass shape, and pcal tones
- The Mark5B comes with a set of programs that allow to check the bit statistics (bstate), do auto- or cross correlations (vlbi2), and extract phase cal (bpcal).
- More power full are the mark5access programs:
m5bstate, m5pcal, m5spec, m5timeseries, ...
Available from the EVN TOG wiki pages
https://deki.mpifr-bonn.mpg.de/Working_Groups/EVN_TOG/DBBC/DBBC_Test_Procedures
- jive5ab allows to stream data directly on a local disk, which avoids to record on diskpacks and use disk2file for small tests.



Test recordings

```
oper@eff-mark5c-1:~$ m5spec
```

m5spec ver. 1.3.1 Walter Brisken, Chris Phillips 20120508

A Mark5 spectrometer. Can use VLBA, Mark3/4, and Mark5B formats using the mark5access library.

Usage : m5spec <infile> <dataformat> <nchan> <nint> <outfile> [<offset>]

<infile> is the name of the input file

<dataformat> should be of the form: <FORMAT>-<Mbps>-<nchan>-<nbit>, e.g.:

VLBA1_2-256-8-2

MKIV1_4-128-2-1

Mark5B-512-16-2

VDIF_1000-64-1-2 (here 1000 is payload size in bytes)

<nchan> is the number of channels to make per IF

<nint> is the number of FFT frames to spectrometize

<outfile> is the name of the output file

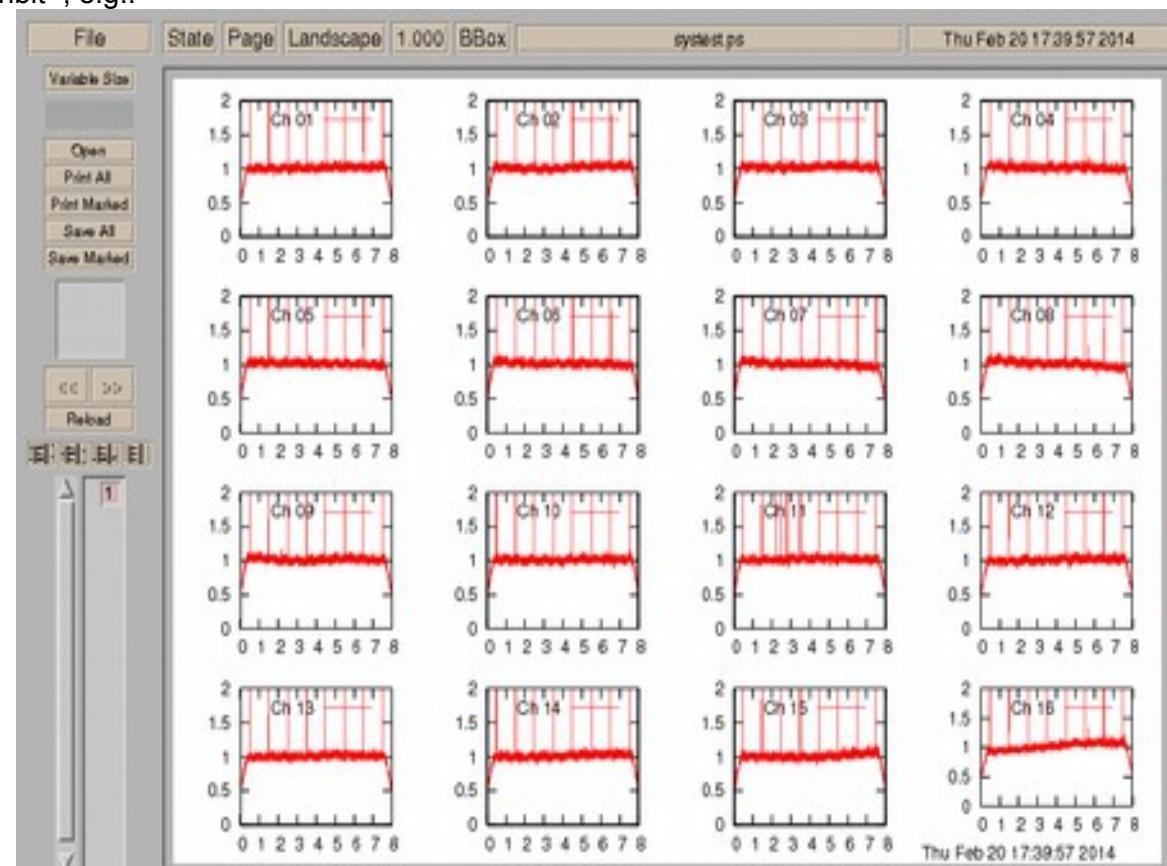
<offset> is number of bytes into file to start decoding

The following options are supported

-dbbc Assume dBBC polarisation order (all Rcp then all Lcp)

-nopol Do not compute cross pol terms

-help This list





Test recordings

> bstate

Usage: bstate <input m5b fname> <# frames>

> bstate n13c1_ef_no0002.m5a 200

| Ch | -- | - | + | ++ | - | - | + | ++ | gfact |
|----|-------|--------|--------|--------|------|------|------|------|-------|
| 0 | 88032 | 157895 | 160426 | 93647 | 17.6 | 32.1 | 31.6 | 18.7 | 1.00 |
| 1 | 93899 | 151616 | 154405 | 100080 | 18.8 | 30.9 | 30.3 | 20.0 | 0.95 |
| 2 | 92338 | 153774 | 156561 | 97327 | 18.5 | 31.3 | 30.8 | 19.5 | 0.97 |
| 3 | 91497 | 154665 | 157139 | 96699 | 18.3 | 31.4 | 30.9 | 19.3 | 0.97 |
| 4 | 84797 | 161299 | 163577 | 90327 | 17.0 | 32.7 | 32.3 | 18.1 | 1.03 |
| 5 | 89860 | 155939 | 158073 | 96128 | 18.0 | 31.6 | 31.2 | 19.2 | 0.98 |
| 6 | 88426 | 157547 | 159995 | 94032 | 17.7 | 32.0 | 31.5 | 18.8 | 1.00 |
| 7 | 85429 | 160711 | 162749 | 91111 | 17.1 | 32.5 | 32.1 | 18.2 | 1.02 |
| 8 | 89485 | 153806 | 157650 | 99059 | 17.9 | 31.5 | 30.8 | 19.8 | 0.97 |
| 9 | 92445 | 150796 | 154915 | 101844 | 18.5 | 31.0 | 30.2 | 20.4 | 0.95 |
| 10 | 89559 | 153929 | 157131 | 99381 | 17.9 | 31.4 | 30.8 | 19.9 | 0.97 |
| 11 | 92958 | 151219 | 155066 | 100757 | 18.6 | 31.0 | 30.2 | 20.2 | 0.95 |
| 12 | 89607 | 153163 | 157750 | 99480 | 17.9 | 31.6 | 30.6 | 19.9 | 0.97 |
| 13 | 84856 | 158081 | 162791 | 94272 | 17.0 | 32.6 | 31.6 | 18.9 | 1.01 |
| 14 | 84164 | 159461 | 163177 | 93198 | 16.8 | 32.6 | 31.9 | 18.6 | 1.02 |
| 15 | 83381 | 159953 | 163898 | 92768 | 16.7 | 32.8 | 32.0 | 18.6 | 1.02 |



Test recordings

- > `vlbi2`

`vlbi file1 file2 -proctime proctime [-rev <0|1>] [-2bit <0|1>] [-tforce <0|1>]`

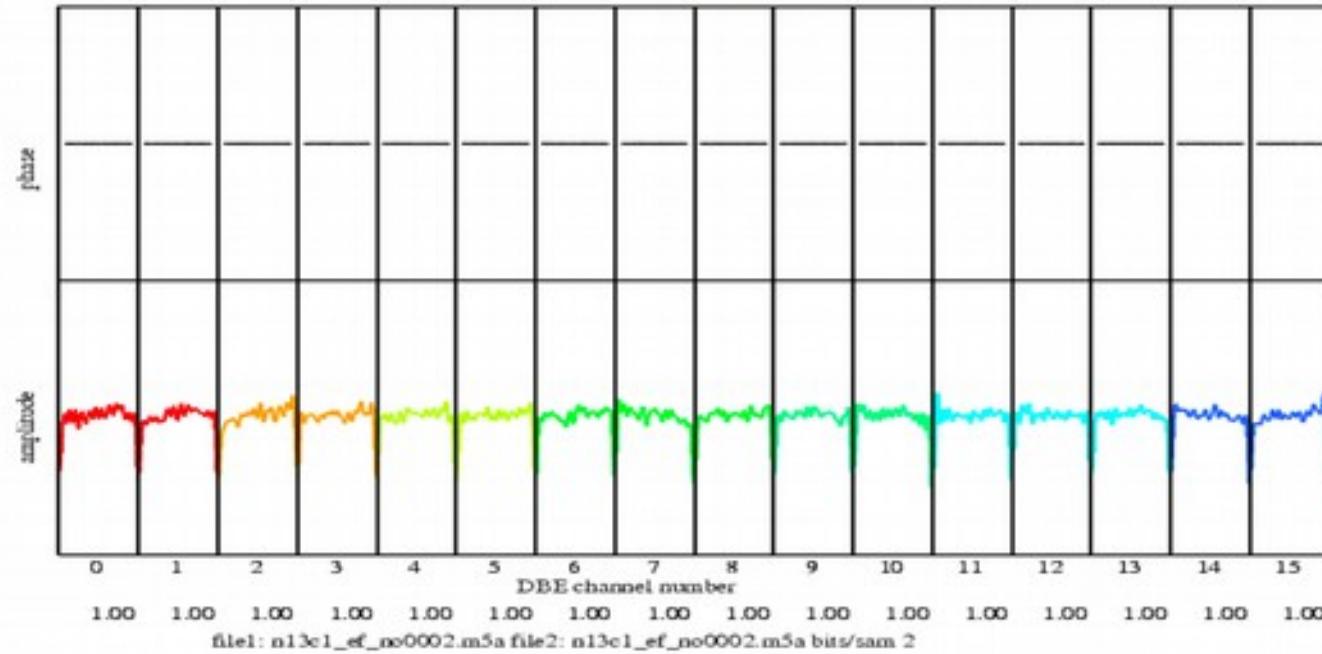
`2bit: 1 to enable 2-bit input`

`rev: 1 to reverse channels in the plot`

`tforce: 1 to force correlation, ignoring timestamps`

`> vlbi2 n13c1_ef_no0002.m5a n13c1_ef_no0002.m5a -2bit 1 # for autocorrelation`

`> gv dd1.pos`





Test recordings

- > *bpcal*

Usage: bpcal <input m5b fname> <tone freq (KHz)> <# frames>
> *bpcal n13c1_ef_no0002.m5a 2490 500*

integration time 0.078 sec

ch amp phase(dg)

| | | |
|----|----|--------|
| 0 | 1 | 153.7 |
| 1 | 0 | -93.5 |
| 2 | 1 | 83.2 |
| 3 | 2 | -20.0 |
| 4 | 1 | -54.9 |
| 5 | 2 | -111.1 |
| 6 | 0 | -179.6 |
| 7 | 1 | -152.4 |
| 8 | 12 | -94.5 |
| 9 | 11 | -82.5 |
| 10 | 11 | -69.3 |
| 11 | 12 | -47.9 |
| 12 | 12 | 24.3 |
| 13 | 12 | -58.8 |
| 14 | 10 | -154.2 |
| 15 | 9 | 134.2 |



Field System integration

- The DBBC is fully integrated into the Field System for DDC mode operation. See `/usr2/fs/misc/dbbc.txt` for all details.
- There are the typical control-files that need to be adapted for a new backend and one special for the DBBC IP address:
 - `dbbad.ctl` hold the DBBC IP address
 - `equip.ctl` for the FS
 - `skedf.ctl` for DRUDG
 - Some more in `point.prc`, `station.prc`, and `.Xresources`
- ➔ Once this is done the FS should be ready to DRUDG and observe DBBC schedules.



Field System integration

```
define proc_library 00000000000x
" EUR135 EFLSBERG Ef
" drudg version 2015Jan29 compiled under FS 9.11.07
"< DBBC  rack >< Mark5B recorder 1>
enddef
define exper_initi 00000000000x
proc_library
sched_initi
logsw_jv
mk5=DTS_id?
mk5=OS_rev?
mk5=SS_rev?
mk5=status?
enddef
define setupsx 00000000000x
pcalon
tpicd=stop
mk5b_mode=ext,0x55555555,,8.000
mk5b_mode
form=geo
form
dbbcsx4
ifdsx
cont_cal=on,4
bbc_gain=all,agc,12000
tpicd=no,200
bank_check
tpicd
enddef

define dbbcsx4 00000000000x
bbc01=100.99,a,4.00
bbc02=110.99,a,4.00
bbc03=140.99,a,4.00
bbc04=200.99,a,4.00
bbc05=310.99,b,4.00
bbc06=390.99,b,4.00
bbc07=440.99,b,4.00
bbc08=460.99,b,4.00
bbc09=112.99,c,4.00
bbc10=127.99,c,4.00
bbc11=137.99,c,4.00
bbc12=167.99,c,4.00
bbc13=187.99,d,4.00
bbc14=192.99,d,4.00
enddef
define ifdsx 00000000000x
ifa=4,agc,2,38000
ifb=4,agc,2,38000
ifc=2,agc,2,38000
ifd=2,agc,2,38000
lo=loa,8110.00,usb,rcp,1
lo=lob,8110.00,usb,rcp,1
lo=loc,2100.00,usb,rcp,1
lo=lod,2100.00,usb,rcp,1
enddef
```

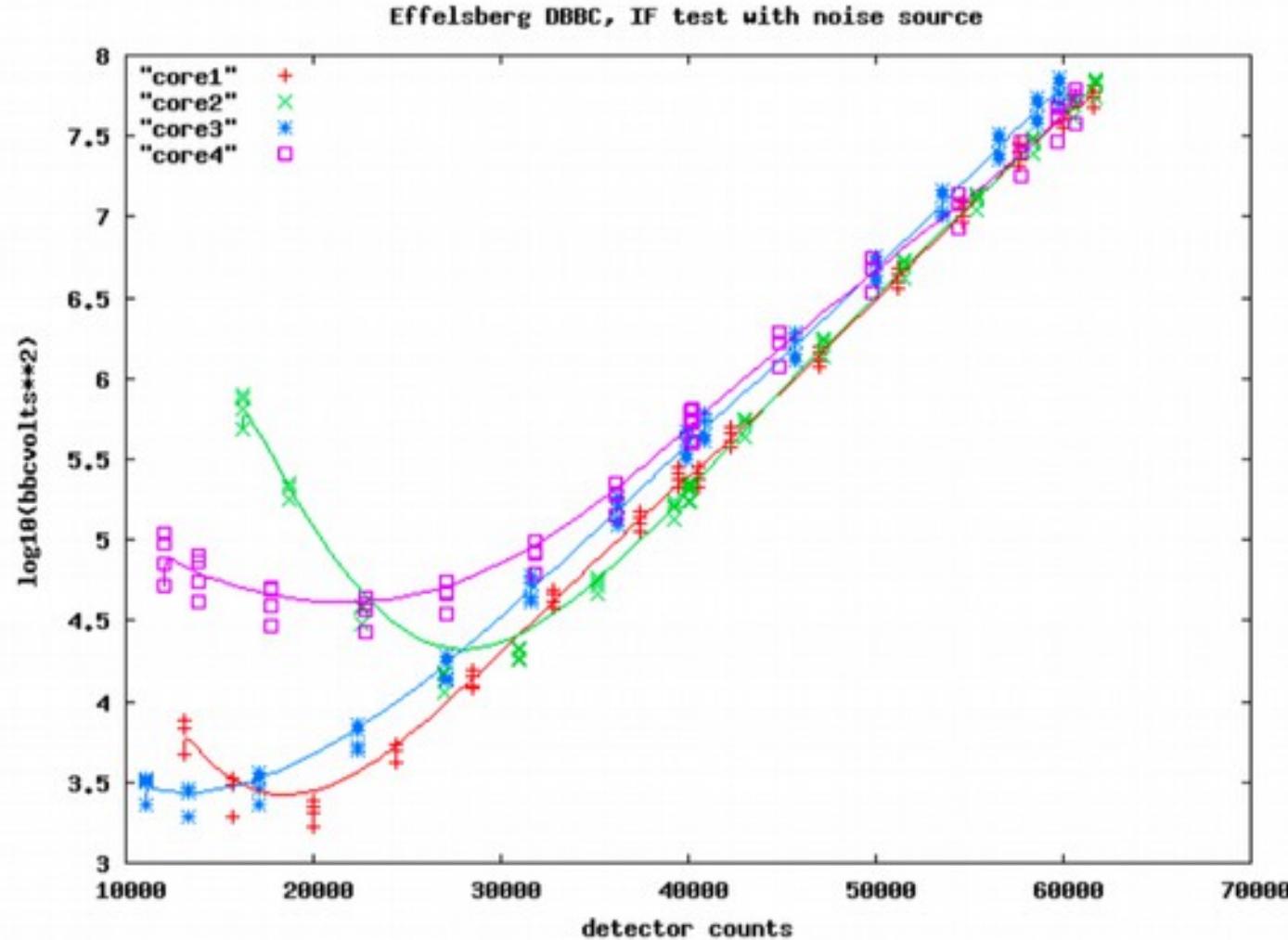


Estimate the best IF level

- IF commands (dbbcifa, or ifa (FS)) allow to specify values for the IF target counts where the AGC should adjusted to.
- With an increasing number of DBBCs the best target IF levels seem to cluster around 35000 to 45000 counts, but it might be worth to test those for your DBBC.
 - Best to use with a true receiver with phase-cal on.
 - Then change the attenuation in steps of 2.5 dB over the whole range, while checking detector counts, bbc counts and doing some short 10 sec recordings at the Mark5B
 - Analyse the recordings using bpcal to measure the Pcal-tone amplitudes.



Estimate the best IF level





Estimate the best IF level

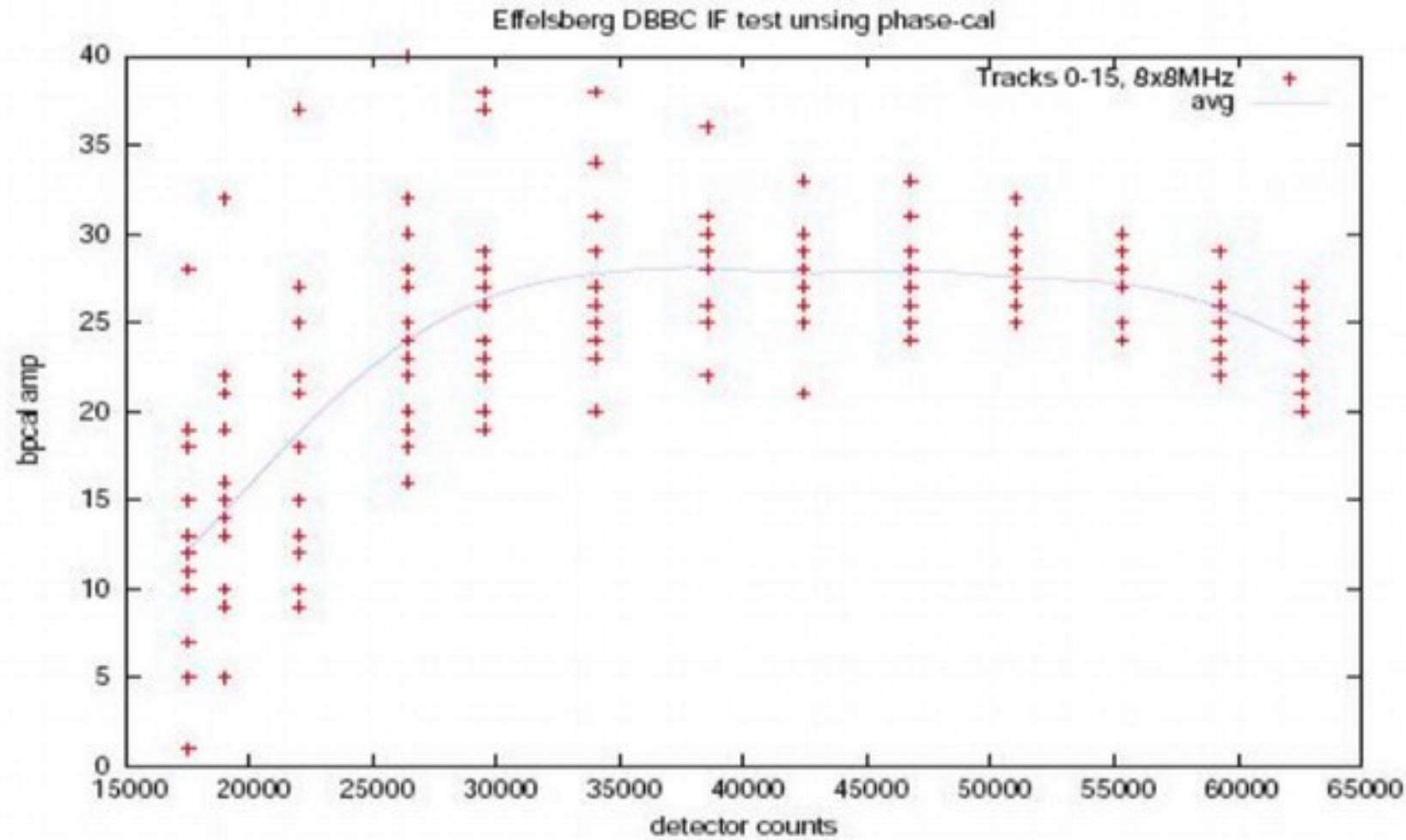
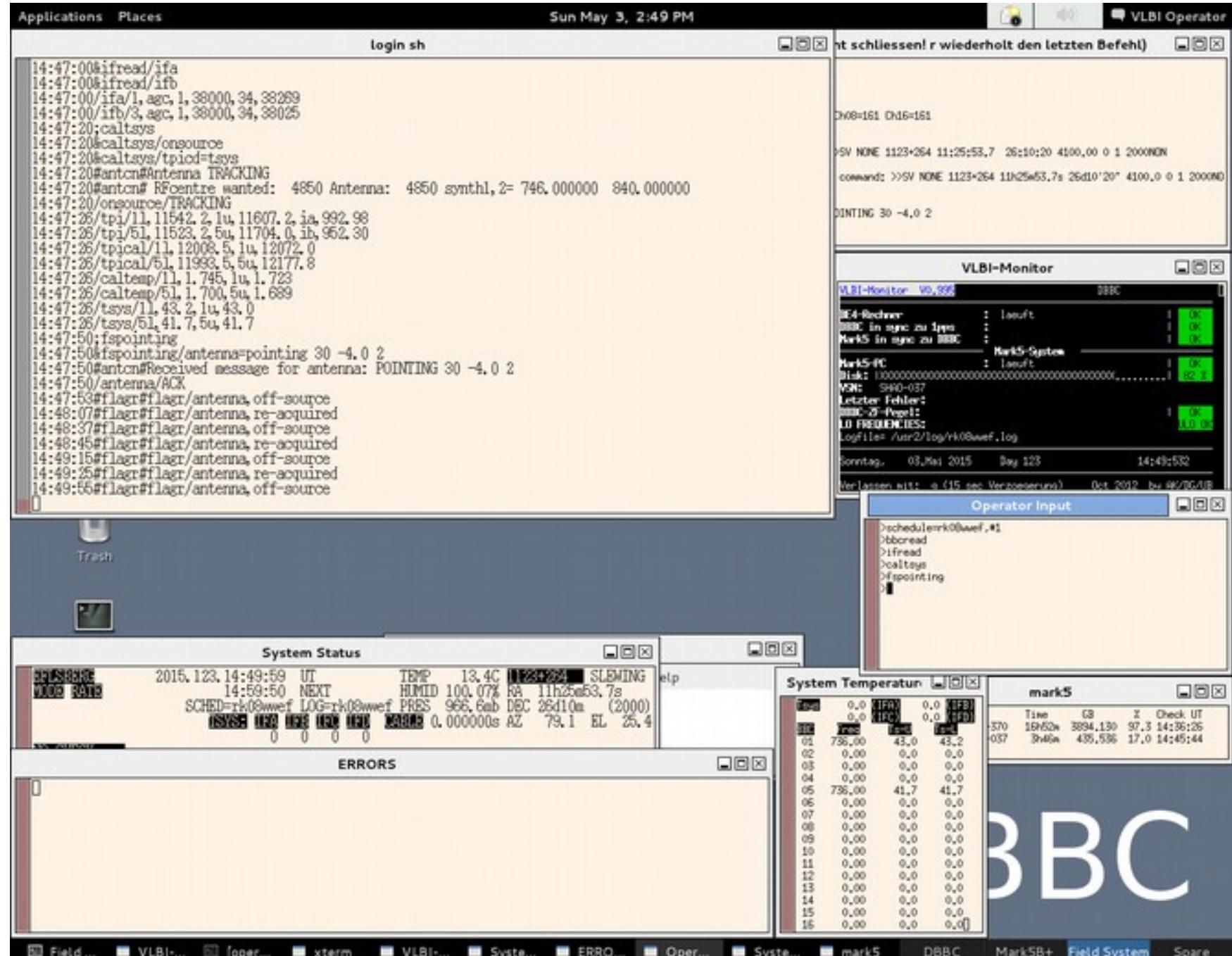


Figure 2: Phase-cal amplitude calculated by bpcal over 0.15 sec against detector counts.

Field System integration



Field System integration



VLBI - KOMPOUND / CHECKLISTE
erstellt am: Dienstag, 28. April 2015 6:48 Uhr

| | | | |
|--|--|------------------------------------|----------------------------------|
| Programm-Name: | rk08ww | Art: | cmac |
| Beginn: | SUN., MAY. 03, 2015 | Tag: | 123 |
| Ende: | SUN., MAY. 03, 2015 | Tag: | 123 |
| Startzeit: | 15:00:00 | UTC | |
| Endzeit: | 16:00:00 | UTC | |
| I. Quelle: | 1123+264 | Azimuth: | 80.8 |
| Elevation: | 26.9 | | |
| 1. Freq | | Kontrolle: | |
| Empfaenger: | 860mm | | <input type="radio"/> |
| Version: | LINKE_500MHz | | <input type="radio"/> |
| Vruefen: | ULQ1 = 746 | MHz: | <input type="radio"/> |
| (Empfaengerraum) | ULQ2 = 840 | MHz: | <input checked="" type="radio"/> |
| ESM1: | 5 | | <input type="radio"/> |
| RX1: | 2 | | <input type="radio"/> |
| SDH: | Sky_freq = 04850+1dB | | <input type="radio"/> |
| Zusätzlich: | XFFTS: Auf 500 MHz oder 2 GHz Filter einstellen MultiFiBa Mode auf 161, Pegel am xfftsGUI okay? | | <input type="radio"/> |
| ULQ-Select Wahlschalter (S 315) nach unten Phasen-Diskriminator (S 172-2) an! | | | |
| Starten der Schedule mit: | schedule = rk08wwrf #1 | (#1= to start at the first line) | <input type="radio"/> |
| Phasecal: on Bei aktiver Schedule kann mit 'phasecal = on/off' die Phasecal geschaltet werden. Zur Kontrolle sollte in den Bandpass des XFFTS gezoomt werden, dort kann man die Toene in einem Abstand von 1 MHz als Kamm sehen. | | | |
| BBC-Pegel: | Abfragen mit bbread | (zeigt auch die BBC-Frequenzen an) | <input type="radio"/> |
| | Einstellung erfolgt automatisch, Pegel counts variable. | | |
| | (benutze Videokonverter: siehe Rueckseite) | | |
| IF-Einstellung: | Abfrage mit ifread | | <input type="radio"/> |
| | Einstellung erfolgt automatisch, Pegel sollte um 38000 liegen | | |
| Toys-messung: | caltsys (Antenne und OBSNP müssen im VLBI Modus sein) | Toys= | <input type="radio"/> |
| | (Toys in benutzten BBC's okay; ST läuft?) | | |
| (Typische Werte bei schwache Quellen: z.B. 18cm-35-40, 6cm-30-35, 5cm-30, 4cm-25-30, 1.3cm-90-100 (weberlangengig)) | | | |
| SCHEDULE lauft?: | keine HALT | In 'System Status' Fenster | <input type="radio"/> |
| Aufnahme auf: | DiskPack (Rueckseite beachten!!!) | Total: | 83.654 GB |
| Korrelator: | **** Moskau **** | | |
| SumLo = | 4100.00 | | |
| Bemerkungen: | | | |
| Nach dem Experiment: | ggf. DiskPack entnommen ggf. Phasecal abgeschaltet ggf. ULQ-Select Wahlschalter (S 315) nach oben! | | <input type="radio"/> |

Wetter: _____

Baender/DiskPacks:

- | | | | |
|-----|-------|-----|-------|
| 01. | _____ | 05. | _____ |
| 02. | _____ | 06. | _____ |
| 03. | _____ | 07. | _____ |
| 04. | _____ | 08. | _____ |

Probleme, Ausfaelle:

Neu:

Die Schedules werden nicht mehr ausgedruckt, koennen aber bei Bedarf im FSPC1 VNC-Fenster mit:
`/home/open>gv /usr2/sched/Lists/rk08wwsnip.ps`
`/home/open>pir /usr2/sched/Lists/rk08wwsnip.ps`
angeschaut bzw. ausgedruckt werden.

DBBC und IF Einstellung:

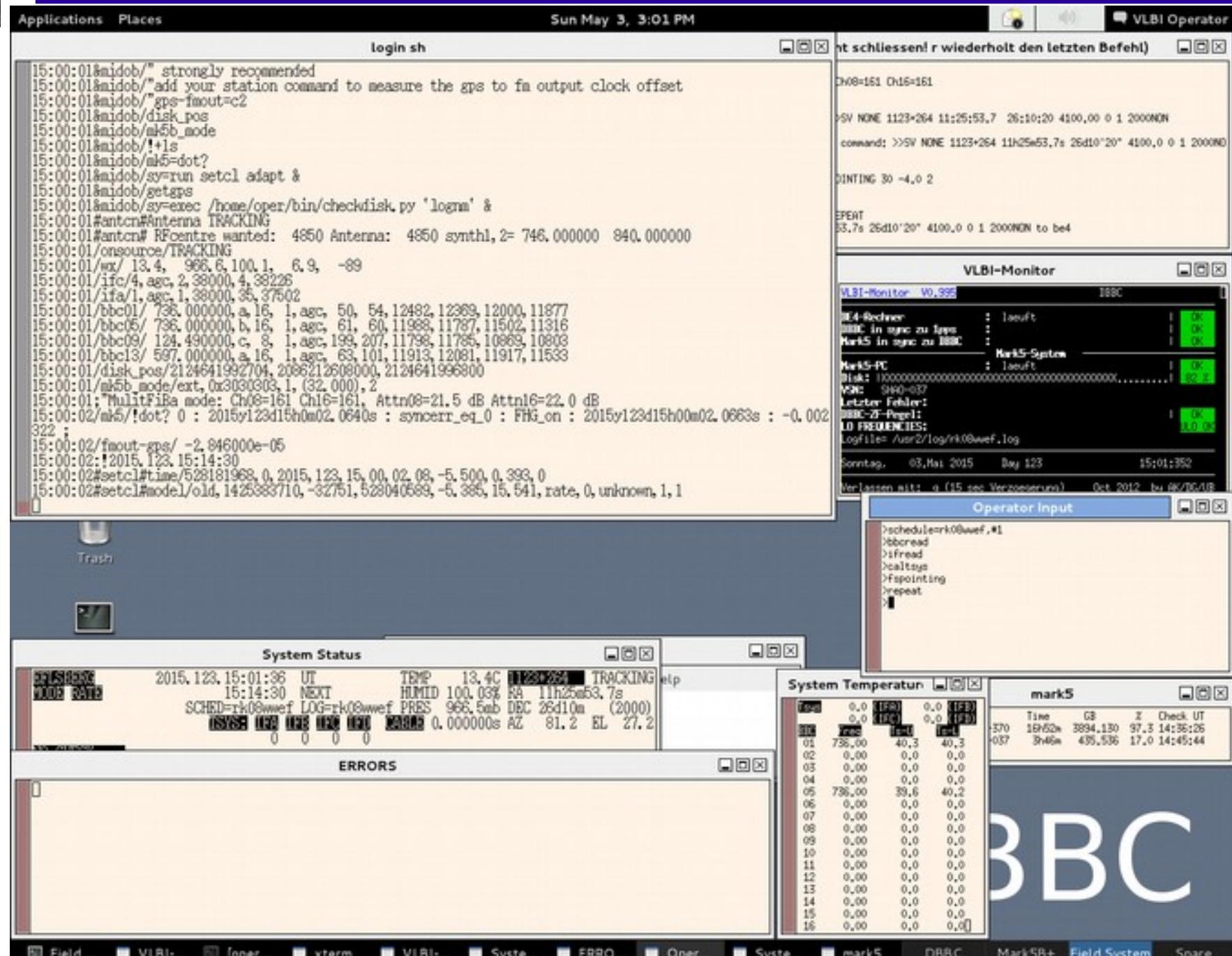
```
rk08wwsnip.ps, 0x03030303, 32, 000
tomastiro
ifan1,agc,1,38000
ifan3,agc,1,38000
```

Einstellung der Videokonverter:

```
procedur dbbc0Id;
bb<<01>>736.00,a,16.00
bb<<03>>736.00,b,16.00
```

Angaben kontrolliert und Programm gestartet von:

Field System integration



Field System integration

ons
01:d
01:a
01#antcn#antenna TRACKING
01#antcn# RFcentre wanted: 4850 Antenna: 4850 synth1,2= 746.000000 840.000000

```

15:15:01/onsource/TRACKING
15:15:01/wx/ 13.5, 966.5, 99.9, 3.5, -89
15:15:01/ifc/4, agc, 2, 38000, 4, 37932
15:15:01/ifa/1, agc, 1, 38000, 33, 38377
15:15:01/bbc01/ 736.000000, a, 16, 1, agc, 49, 53, 11963, 11894, 11467, 11389
15:15:01/bbc05/ 736.000000, b, 16, 1, agc, 62, 61, 12076, 11881, 11586, 11381
15:15:01/bbc09/ 124.490000, c, 8, 1, agc, 202, 211, 11244, 11272, 10319, 10298
15:15:01/bbc13/ 597.000000, a, 16, 1, agc, 63, 103, 11917, 11867, 11927, 11293
15:15:01/disk_pos/2152462417920, 2124641996800, 2124661996800
15:15:01/mk5b_mode/ext, 0x3030303, 1, (32.000), 2
15:15:01;"MultiFiBa mode: Ch08=161 Ch16=161, Attn08=21.5 dB Attn16=22.0 dB
15:15:02/mk5/?dot? 0 : 2015y123d15h15m02.0478s : syncerr_eq_0 : FHG_on : 2015y123d15h15m02.0502s : -0.00
2376:
15:15:02/fmout-gps/ -2.845000e-05
15:15:02:!2015.123.15:29:30
15:15:02#setcl#utime/528271971, 0, 2015, 123, 15, 15, 02, 06, -5, 228, 0.643, 0
15:15:02#setcl#model/old, 1425383710, -32751, 528040589, -5.385, 15.541, rate, 0, unknown, 1, 1
15:15:02;" Disk 00 (1.81e-03, 0.00e+00) is OK!
15:15:02;" Disk 01 (1.75e-03, 0.00e+00) is OK!
15:15:02;" Disk 02 (1.41e-03, 0.00e+00) is OK!
15:15:02;" Disk 03 (2.04e-03, 0.00e+00) is OK!
15:15:02;" Disk 04 (1.83e-03, 0.00e+00) is OK!
15:15:02;" Disk 05 (1.98e-03, 0.00e+00) is OK!
15:15:02;" Disk 06 (2.19e-03, 0.00e+00) is OK!
15:15:02;" Disk 07 (2.00e-03, 0.00e+00) is OK!
```

Trash

System Status

| | | | | | |
|------|-------------------|------|-------|----------|--|
| DATE | 2015.123.15:16:33 | UT | 13.6C | 1123+264 | TRACKING |
| MODE | 15:29:30 | NEXT | HUMID | 99.87% | RA 11h25m53.7s |
| RATE | | | | | SCHED=rk08wwef LOG=rk08wwef PRBS 966.6mb DEC 26d10m (2000) |
| | | | | | ISYS: IFA IFE IFO IFL CABLE 0.00000s AZ 83.9 EL 29.6 |
| | 0 0 0 0 | | | | |

ERRORS

VLBI-Monitor

| VLBI-Monitor V0.995 | | DBBC |
|------------------------|---|-----------------------|
| SE-Rechner: | : lauft | OK |
| DBBC in sync zu Ipp: | : OK | OK |
| Mark5 in sync zu DBBC: | : | OK |
| Mark5-System | | |
| Mark5-PC: | : lauft | OK |
| Diskt: | (XX.....) | B4 T |
| VNC: | SH40-037 | |
| Letzter Fehler: | DBBC-ZF-Pegel1: | OK |
| 10 FREQUENCIES: | 8.0.00 | |
| Logfile: | /usr2/log/rk08wwef.log | |
| Sonntag, | 03.Mai.2015 Bay 123 | 15:16:31 |
| Verlassen mit: | a (15 sec Verzögerung) | Oct. 2012 by AK/BG/UR |

Operator Input

```

>scheduler=rk08wwef,#1
>bbcread
>ifread
>caltsys
>fpointing
>repeat
>
>
```

System Temperatur

| Port | I=0 | I=-1 | I=1 | I=2 |
|------|--------|------|------|-----|
| 01 | 796.00 | 38.3 | 38.4 | |
| 02 | 0.00 | 0.0 | 0.0 | |
| 03 | 0.00 | 0.0 | 0.0 | |
| 04 | 0.00 | 0.0 | 0.0 | |
| 05 | 796.00 | 38.8 | 38.1 | |
| 06 | 0.00 | 0.0 | 0.0 | |
| 07 | 0.00 | 0.0 | 0.0 | |
| 08 | 0.00 | 0.0 | 0.0 | |
| 09 | 0.00 | 0.0 | 0.0 | |
| 10 | 0.00 | 0.0 | 0.0 | |
| 11 | 0.00 | 0.0 | 0.0 | |
| 12 | 0.00 | 0.0 | 0.0 | |
| 13 | 0.00 | 0.0 | 0.0 | |
| 14 | 0.00 | 0.0 | 0.0 | |
| 15 | 0.00 | 0.0 | 0.0 | |
| 16 | 0.00 | 0.0 | 0.0 | |

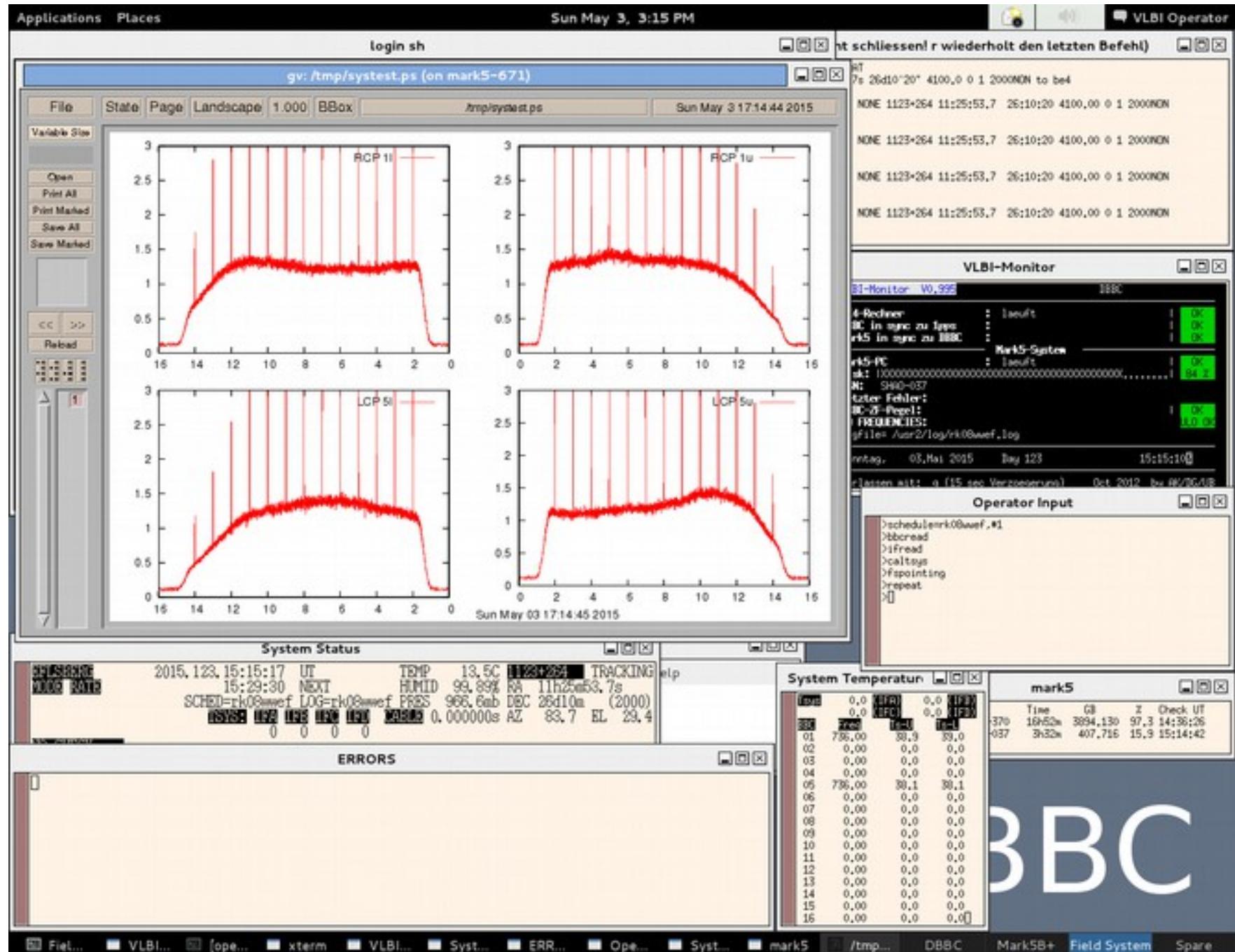
mark5

| Time | G8 | Z | Check UT |
|------|--------|----------|---------------|
| 1370 | 15h52m | 3894.130 | 97.3 14:38:26 |
| 037 | 3h52m | 407.716 | 15.9 15:14:42 |

BBC

Field... VLBI... Open... xterm VLB... Syst... ERRO... Oper... Syst... mark5 DBBC Mark5B+ Field System Spare

Field System integration



Field System integration

stream = File-1/l=systest.mbb
format = Mark5B-1024-1
start mjd/sec = 708 76
frame duration = 78125
framenum = 0
sample rate = 32000000
offset = 0
framebytes = 10016 byte
datasize = 10000 bytes
sample granularity = 1
frame granularity = 1
gframes = 78125
payload offset = 16
read position = 0
data window size = 104

| Ch | — | + |
|----|-------|--------|
| 0 | 78363 | 169483 |
| 1 | 92461 | 155968 |
| 2 | 92018 | 156732 |
| 3 | 91365 | 156659 |
| 4 | 78329 | 170000 |
| 5 | 92118 | 155761 |
| 6 | 91422 | 156754 |
| 7 | 91206 | 156917 |
| 8 | 89432 | 159946 |
| 9 | 91630 | 156454 |
| 10 | 93114 | 154877 |
| 11 | 92675 | 156649 |
| 12 | 92042 | 156667 |
| 13 | 90890 | 157411 |
| 14 | 91835 | 1571 |
| 15 | 92369 | 155732 |

System Status

| 2014.051.21:20:36 UT | TEMP | 7.3C |
|----------------------|----------|------------------|
| 21:20:50 NEXT | HUMID | 95.40% |
| SCHED=mail1lef | RA | 06h32m59.3s |
| LOG=mail1lef | PRES | 967.4mb |
| (SIS) | DEC | 05d49m (2000) |
| 0 0 0 0 | 0.00000s | AZ 206.6 EL 42.4 |

ERRORS

```
* 2014.051.19:49:56.012ERROR qo -301 WARNING: ONSOURCE status is SLEWING!
* 2014.051.20:00:40.022ERROR qo -301 WARNING: ONSOURCE status is SLEWING!
* 2014.051.20:11:25.007ERROR qo -301 WARNING: ONSOURCE status is SLEWING!
* 2014.051.20:22:11.012ERROR qo -301 WARNING: ONSOURCE status is SLEWING!
* 2014.051.20:32:56.012ERROR qo -301 WARNING: ONSOURCE status is SLEWING!
* 2014.051.20:43:41.012ERROR qo -301 WARNING: ONSOURCE status is SLEWING!
* 2014.051.20:54:26.012ERROR qo -301 WARNING: ONSOURCE status is SLEWING!
* 2014.051.21:05:11.012ERROR qo -301 WARNING: ONSOURCE status is SLEWING!
* 2014.051.21:15:56.012ERROR qo -301 WARNING: ONSOURCE status is SLEWING!
```

System Temperatur

| tsup | 0.0 | (IFR) | 0.0 | (IFD) |
|------|--------|-------|------|-------|
| 01 | 100,49 | 19,3 | 26,3 | |
| 02 | 132,49 | 22,6 | 22,4 | |
| 03 | 164,49 | 21,6 | 22,2 | |
| 04 | 196,49 | 22,4 | 24,7 | |
| 05 | 100,49 | 22,1 | 25,1 | |
| 06 | 132,49 | 21,6 | 22,1 | |
| 07 | 164,49 | 21,3 | 21,6 | |
| 08 | 196,49 | 21,8 | 23,4 | |
| 09 | 0,00 | 0,0 | 0,0 | |

VLBI-Server (Wichtig nicht schliessen! r wiederholt den letzten)

BBBC

mark5

start_vncs.cad
rver.cad
rver.cad

Pages