

University of Bordeaux, LAB Internal Memo

Detection and Correction of Radiation Induced Events in Integrated Circuits of the ALMA Correlator High Site

Alain Baudry

baudry@obs.u-bordeaux1.fr

Université de Bordeaux, LAB, 33270 Floirac, France

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History

- Initial document edited on 30/12/2008
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- All sections revised and final SEU measurements included in version of 27 November 2014

Summary

The Cyclic Redundancy Check (CRC) circuit built in the Altera Stratix II FPGAs (90nm technology) of the Tunable Filter Bank (TFB) cards in the ALMA Correlator system and the TFB card design allow us, with the appropriate monitoring software, to estimate the Single Event Upset (SEU) rate observed in these devices at the 5050-m high ALMA site (AOS). SEUs are primarily due to the fast neutrons generated when the Cosmic Rays hit the Earth's atmospheric molecules. We have performed measurements at the AOS for a total test length of 930 hours in the years 2011 and 2012 during which we have monitored the 2048 Altera Stratix II FPGAs assembled on the 128 TFB cards of one Correlator Quadrant. The measured SEU rate, 2.68 events per day and per Quadrant, implies a total rate of 10.7 SEUs per day for the complete 4-Quadrant Correlator system. We tentatively showed that the SEU rate measured at the AOS was not affected by two Solar storms observed during our test period. The observed error rate compares well with the Altera predictions after the acceleration factor due to the site elevation and geographical location is included ; the FIT rate is being dominated by errors in the configuration RAMs. Prior to the final assembly of the last Quadrant of the Correlator at the AOS, measurements were also performed at the Charlottesville integration site (nearly sea level) for all 2048 Altera FPGAs of the TFB cards. The measured rate was found to be 0.08 to 0.07 events per day for test lengths of 100 to 150 days. The SEU rate at the two sites varies roughly in proportion with the site elevation. The results obtained for the TFB card FPGAs show that the SEU rate in these devices is well above the estimated SEU rate in the FPGAs and the correlator chips (with 250nm technology) assembled on the correlator cards. Therefore, measuring the SEU rate in the TFB cards provides a good estimate of the Cosmic Rays impact on the entire Correlator system.

Mitigation of SEU induced errors primarily consists in downloading the FPGA personalities ; the present work suggests that this should be performed several times a day when the full Correlator system is at work. As a CRC error can be identified for each TFB card we also have the possibility to perform 'real time' recovery of the SEU events to improve the astronomical data quality ; this approach still needs software development and prioritization. The ALMA Correlator system can be considered as a 'neutrons detector' and long term recording of SEU events should usefully help to understand the impact of Cosmic Rays at the ALMA site in general.

1. Introduction and main objectives

Effects of Cosmic Rays on electronic devices are enhanced at high elevation terrestrial sites. They are a potential threat for the thousands of Xilinx and Altera Field Programmable Gate Arrays (FPGAs) as well as for all other integrated circuits used in the ALMA Correlator system located at the 5050-m high ALMA site (AOS). The risk arises because of the very large number of digital circuits being used in this system and because of the low but finite probability that the cascade of neutrons generated in the upper terrestrial atmosphere by primary Cosmic Rays alter the personalities downloaded in the FPGAs. The most likely failure in the Correlator system is then a temporary loss of the FPGA personality resulting in a software error and a temporary loss of part of the ALMA science data.

In this memo, we first briefly recall the basic effects expected from the interaction of the primary Cosmic Rays with the Earth's atmosphere and define the non destructive effects of Single Event Upsets (SEUs) on integrated circuits then, we concentrate on our main objectives :

- a) Measure with the built-in redundancy check circuit in the Altera FPGAs of the Tunable Filter Bank (TFB) cards and with the appropriate software the rate of SEUs observed at the ALMA high elevation site (AOS) ;
- b) Compare the SEU rate at the high site with that at sea level for the same number of Altera FPGAs ;
- c) Compare the SEU rate in the Altera FPGAs with the error rate in other FPGAs and the ALMA1 correlator chips ;
- d) Discuss our results and how to mitigate SEU induced errors.

In addition, we suggest to correlate the SEU measurements with other radiation measurements.

Effects of radiation on the ALMA Correlator operation were first discussed in [1] on the basis of the predicted vulnerability of thousands of Xilinx FPGAs used in the system. In the present memo we primarily propose to directly estimate in the Correlator system environment and at two widely different sites the SEU rate thanks to dedicated monitoring routines and the specific built-in circuitry available in the TFB card FPGAs. This is of interest not only as a general diagnosis tool to estimate the occurrence of anomalous events at the AOS but also for better operation of the Correlator system. Our results should help to define a strategy to mitigate the impact of the Cosmic Rays in the ALMA Correlator. SEU induced errors in other sub-systems of the ALMA Observatory using several FPGAs could perhaps be predicted as well, provided that the differences in the FPGA technologies (fabrication process or core voltage) are understood in terms of SEUs.

2. Cosmic Rays and Single Event Upsets in integrated circuits

2.1 Cosmic Rays and Earth's atmosphere

The Cosmic Rays of interest here are not the high energy protons or helium nuclei naturally produced by cosmic sources (distant extragalactic nuclei, supernovae, etc.) or the Sun in the outer space but the secondary particles and radiation produced by the primary Cosmic Rays when they enter the Earth's atmosphere. Protons, the most abundant primary particles, colliding with atmospheric molecules give rise to a cosmic ray 'air shower' of secondary particles whose energy depends on the energy of the primary particles. High and low energy neutrons are kicked out of the nuclei of the atmospheric molecules during this process while gamma rays resulting from the decay of neutral pions are produced simultaneously. The neutron production process is fully random. (Charged pions rapidly decay to muons and other particles which supposedly are not of interest in generating SEUs.)

Both neutron and gamma ray dose rates were measured near the AOS site and at lower elevations with dedicated dosimeters and neutron rem counters (see reference [2] and Sect. 5.2). It was found that the measured particles and radiation doses are more pronounced with altitude for the neutrons than for the gamma rays.

2.2 Single Event Upsets

A Single Event Upset (SEU) is a non destructive effect due to radiation, fast atmospheric neutrons or ionized energetic particles impinging on an electronic device or a semi-conductor

memory. The net result is a change of state or software error. An SEU may toggle one of the flip-flops in a microcircuit resulting in a functional error or induce bit flips in a memory or a register. Once detected, software errors can simply be erased by reloading the content of a memory or the circuit registers. The rôle of radiation and Cosmic Rays has long been recognized to be a potential source of software errors in RAMs (see e.g. [3] and [4]).

SEUs are expected to become more frequent at higher elevations due to the enhanced effects of fast neutrons generated from the interaction of primary Cosmic Rays with the terrestrial atmosphere. These neutrons when they hit a silicon nucleus give rise to various fragments and electrical charges which may upset an electronic device or a volatile memory. SEUs could also be due to the Alpha particles generated by the radioactive decay of natural isotopes present in the device package or in impurities. This source of SEUs should be weak and is well mastered by appropriate packaging of commercial FPGAs ; it is not elevation dependent.

2.3 Other events

At the ALMA site, contrary to space crafts or satellites exposed to energetic primary Cosmic Rays or Solar activity, destructive events such as ‘latchups’ are not expected a priori. However, single event transients could perhaps trigger voltage pulses (or glitches) propagating through the I/O pins of microcircuits. To protect the Correlator system from such problems or malfunctions the system watches for high currents in the most critical places of the Correlator.

3. Measuring SEUs in the Correlator filter cards

3.1 Cyclic Redundancy Check in TFB card FPGAs

The FPGA used in the TFB cards is the Stratix II EP2S30 from Altera (34000 Logic Elements, 90 nanometer logic process). It provides a Cyclic Redundancy Check (CRC) built-in circuit which routinely checks for possible software error in the configuration memory while the device is being used (see [5]). Each FPGA has a dedicated error output line which is enabled at the compilation stage and thus only one external pin has to be monitored for CRC errors. A small programmable logic device (CPLD) assembled on the TFB card is used to monitor all error lines in the matrix of 4x4 Altera Stratix II chips on each card. These 16 lines are ‘OR-ed’ and one output line is sent to another CPLD, CPLD2, which is primarily used to download the FPGA personality. There is only 1 memory error line for all 16 FPGAs on one board. Note that with this design and for observations not requiring all FPGAs (our strategy is to operate those unused FPGAs in low power mode) it is not possible to identify if an SEU occurs in an FPGA being actively used or not.

When a software error occurs (bit 7 of the CPLD2 monitor register is asserted) the green led on the TFB card front panel is switched ‘off’ and the red led is ‘on’. However, the red led can be ‘off’ if the digital filter DLL or the TFB delay chip DLL is unlocked, or if the 3.3V supply is not nominal ; no DLL or 3.3V supply means no filtering functionality.

The time required for each CRC calculation depends on the Altera product and the error detection clock frequency can be specified in the Quartus II software. In our case we use 390 kHz corresponding to the minimum error detection frequency. The CRC calculation time for each Stratix II device assembled on the TFB card is around 2.8 seconds ; we thus get around 30000 samples after one day CRC monitoring.

In addition to the 16 lines OR-ed to monitor SEU events, a seventeenth line is available to check the contents of the RAMs used in the filter design and the DDS mixer block of the TFB filter (an error could occur in the DDS sine table for example). The memory blocks support parity bits to check the memory contents but this possibility is not implemented in our current firmware as it would require to use additional FPGA logic elements. We anticipate that flagging the data on the basis of corrupted memory blocks in the TFB card is not desirable. There is much spare logic available in our design, however, and checking the memory contents is feasible in the future if that would be required.

3.2 Impact of neutrons on Altera products, FIT rate

Accelerated soft error testing and SEU FIT rate measurements or estimates (1 FIT = 1 failure in 10^9 hours) have been made by Altera for their products when they are submitted to both terrestrial neutrons generated by Cosmic Rays and Alpha particles generated by package materials. Although these data are not public, confidential information was passed to us in 2005 [6] at a time where the technology to be adopted for the new, flexible version, of the ALMA digital filter card was still under discussion between the University of Bordeaux group and the Altera engineers. The relative impact of neutrons on the Stratix I (130nm), Stratix II (90nm) and HardCopy I products were compared and it was concluded that the more powerful Stratix II EP2S30 FPGA would not be much more affected above 5000 to 10000 feet than the Stratix I products. (The FIT rate for the HardCopy I version is more than one order of magnitude below the EP2S30 FIT but this version was discarded because it does not offer the possibility to reprogram our filter design and because we had demonstrated that the Stratix II-based filter card could dissipate little power.)

Following our own SEU rate measurements made in 2011 and 2012 in the Correlator system (see Sect. 4) further SEU information was provided to us by Altera for their 90nm products [7]. The various components of the Altera FPGA circuits contribute to the net FIT rate. The configuration RAM (CRAM) errors dominate while errors from Logic Elements or I/O registers are much smaller and the user memory errors are detectable and correctable. For the EP2S30 FPGA the CRAM errors estimated by Altera are 2506 and 737 FITs at sea level for the neutron and Alpha particles contributions, respectively ; these numbers will be used in Sect. 4.1 for comparison with our measurements.

3.3 Conditions and firmware to identify SEU events at the AOS and sea level site

The impact of Cosmic Rays on integrated circuits at the ALMA high site is largely unknown and although Altera FIT predictions exist it is worth checking these predictions and monitoring the actual number of anomalous events occurring in the Correlator system environment. This system consist of 4 Quadrants of digital electronics which were delivered sequentially to the ALMA obseravtory. The correlator team was in a most favourable situation to perform SEU tests in two widely different sites when the third Quadrant was installed at the AOS but unused for science or engineering tasks and the fourth Quadrant was still under test at the NRAO technical building in Charlottesville (nearly at sea level) before delivery to the AOS. Each Quadrant includes a total of 128 TFB cards with a total of 2048 Altera FPGAs. This number is rather high and provided that error monitoring is performed over a long enough period of time a sensible SEU rate can then be estimated and variations of this rate at the two different sites can be observed.

The key elements in such measurements are the CRC circuit and error check logic implemented according to the scheme described in Sect. 3.1 above. Our design thus allows us to remotely monitor errors due to SEU events. The Station Control Card (SCC) must periodically monitor Bit 7 of the CPLD2 monitor register on the TFB card to be informed of eventual CRC errors. Infrequent inquiries, of the order of a few seconds as suggested by the time required for the CRC calculation (see Sect. 3.1), are sufficient to check for errors. This information can be passed to the Correlator Control Computer which periodically monitors various parameters across the Correlator system. Dating the errors is not mandatory but as the CRC errors are random by nature and infrequent the day and month of the errors should be recorded as well as the total duration of the monitoring period.

In practice, for remote semi-manual SEU measurements in the third and fourth Quadrants, the correlator team used a dedicated command issued from the ‘engineering port’ in the Correlator ‘back-end’. This commands allows us to remotely and simultaneously check for possible SEUs in all TFB cards of a Quadrant. In addition, when the SEU error flag was present, a number of other checks were made to exclude other sources of errors and decide if the event could be kept for the SEU statistics. These additional checks included monitoring the power consumption, DLL status (with respect to the reference clock), local bus connection and the TFB current/voltage reading. Finally, we have discarded any monitoring period showing anomalies in the third Quadrant auto-correlation spectra at the AOS

4. SEU statistics in the Correlator system and observed radiation effects

4.1 SEU measurements in the TFB cards

SEU measurements were performed in the third Quadrant at the AOS by checking the SEU error flag according to the procedure outlined above. Data were acquired on a rather regular basis during the period 21 October 2011 to 1 September 2012. Eliminating all suspicious ‘experiments’ we are left with a total of 930 hours (38.8 days) during which an average of 2.68 events per day were observed from the monitoring of 2048 FPGAs in the third Quadrant. This implies about 10.7 SEUs/day across all TFB cards in the full Correlator system.

Our measurements can be compared to the Altera predictions. Restricting the analysis to the CRAM errors and accounting for the FIT rate acceleration factor of 17.46 (due to the ALMA geographical position and elevation) we obtain 2.18 events/day for 2048 EP2S30 devices in the third Quadrant. For the entire system we then get 8.7 events/day which must be seen as a minimum value. Considering that there might be other sources of events not included in this estimate (Solar activity for instance) 8.7 events/day is reasonably close to the actual measurements leading to 10.7 events/day.

Similar procedures for SEU measurements in the fourth Quadrant at Charlottesville were applied and started in March 2011. The test length was longer than at the AOS as required for a 130-m elevation site where less events are expected. The measured rate ([8]) is 0.08 and 0.073 SEU/day for test lengths of 97.7 and 149.85 days, respectively.

It is interesting to note that the ratio of the SEU rates measured at the 5050-m and 130-m sites in one Quadrant, 34 or 37 depending on using 0.08 or 0.073 SEU/day per Quadrant at Charlottesville, is close to the sites elevation ratio of $5050/130 = 39$. Certainly, the neutron flux impacting the integrated circuits increases with elevation and our measurements reflect this trend.

4.2 SEU rate and rôle of Solar activity

Because the number of 10.7 events/day in the complete TFB card sub-system is rather high it is worth investigating whether there might be some relationship with the Solar activity. The ‘normal’ Solar activity is measured in terms of the Sunspot number and is anti-correlated with the neutron counts measured on the Earth because the Sun helps to protect us from the Cosmic Rays. From this view point the period from about 2010 to about 2015 is favourable since the Sunspot number increases according to the undecadal Solar cycle (minimum reached in 2009). However, we have observed events at the AOS in the 2011-2012 period which was perhaps still too close to the Sunspot number minimum. The overall Solar picture is much more complex than the image provided from ‘normal’ activity. Solar wind streams, shocks and enhanced magnetic field activity may help to repel the Cosmic Rays while large eruptions are frequent and may inject fast neutrons and ionized particles thus affecting the average neutron counts at high elevation sites. Two significant Solar events were observed during our SEU measurements. A large Solar eruption was observed around Christmas 2011 and the strongest Solar storm observed since 2005 was recorded in January 2012. Despite our SEU data base is relatively small we have counted the events in different monthly bins but could not find any significant deviation from the average 2.7 SEUs per day and per Quadrant in relation with these Solar events.

4.3 SEU rate in full Correlator system

The average SEU rate expected at the AOS for the 8192 Altera FPGAs of the entire filtering sub-system (512 TFB cards) is relatively high, 10-11 SEUs per day, and must be compared with expectations for the other devices in the Correlator system. As for the TFB FPGAs neutrons and radiations randomly affect the 32768 correlator chips and the thousands of Xilinx chips assembled on the 512 correlation cards of the ALMA Correlator. Because the smallest Xilinx chip already has four times the number of flip-flops in a correlator chip, the SEU risk is much higher in the Xilinx FPGAs than in the correlator ASICs where it can be neglected (see [1]). The 250nm technology used in the ALMA1 correlator chip is also less susceptible to the effects of radiations than the 180nm technology used in the Xilinx FPGAs and, even if one event would affect one lag flip-flop among the numerous flip-flops in the 4096 lags of each ALMA1 chip, the error would be for a single 16 msec integration time of the Correlator. There is no CRC circuit available in the Xilinx chips used in the Correlator system and we rely on the Xilinx predictions and estimates made in [1]. In the final Correlator design, where the filtering function is implemented in the TFB cards, the mean time between two SEU events in the Xilinx chips on all correlator cards is predicted to be 716 hours at the AOS. This is about 1 event every 30 days to be compared to 10-11 events per day in the 512 TFB cards.

Clearly, the 8192 Altera chips in the TFB cards with more recent 90nm technology are more susceptible to SEU errors than other FPGA devices or the correlator chips in the entire Correlator system.

4.4 Observed radiation effects in TFB cards and mitigation

During the course of the ALMA Correlator test tasks at the AOS four TFB card failures were observed and identified with 4 different FPGA failures. Unfortunately the SEU monitoring routine was not active at that time but when the incriminated FPGAs were removed from the TFB cards we found that some FPGA balls were burnt and in one case the TFB board was damaged. By replacing the faulty FPGAs the functionality was fully restored. We suspect that

the observed apparent short-circuits on the 1.2V supply were due either to high SEU rates or latchups. To mitigate potential destructive effects the Quadrant Correlator Computer monitors the TFB 1.2V regulator currents to eventually shutdown the system beyond an adopted limit. No similar events were reported since the above current monitoring was implemented.

These reported failures demonstrate the potential destructive impact of radiations at the AOS and strengthen the interest of implementing an SEU monitoring policy.

5. SEU errors mitigation and data integrity, Other radiations measurements

5.1 Mitigation of SEU induced errors and Correlator operation

To mitigate the effects of SEU events it was proposed initially to download daily all the FPGA personalities (see [1]). The present work suggests that much more frequent reconfigurations would be desirable for the FPGAs in the TFB cards when the full Correlator system is at work. This would enhance the astronomical data integrity.

The exact procedure to follow after an SEU event is detected must still be worked out. The most conservative approach is to download the FPGA configuration in all TFB cards and/or download all FPGA personalities for all devices in the Correlator system when there are no observations or perhaps during large antenna slews. This is feasible because downloading the FPGA personalities is performed quickly compared to the approximate 30 seconds needed to reset the entire Correlator system. Our design and monitoring routines allow us to identify the faulty TFB card and we thus have the possibility to cure the fault at the most appropriate time. Preliminary discussions have suggested that the following sequence might be applicable for ‘real-time’ correction [9]. When the SCC finds an SEU error while monitoring various correlator parameters (about every 10 seconds), it reloads the faulty TFB card personality and the registers needed to make it operational. When the CCC receives the SEU error message it logs the SEU event so that downstream data processing can take it into account. In parallel the event may be recorded in a SEU data base for further analysis. However, this approach requires software development time and software development prioritization to be efficiently implemented in the ALMA Observatory.

Although not all TFB cards will be used for all types of observations, ‘real-time’ recovery of SEU events in the TFB cards is highly desirable to optimize the astronomical data integrity. Long term SEU monitoring and analysis will also be useful to precisely investigate the possible impact of cumulated radiation doses on integrated circuits and FPGAs at the AOS ; such a degradation is perhaps acceptable but is unknown. We further note that SEU monitoring should be combined with other error tracking approaches to optimize the system integrity and the data quality. For instance, when there are no observing sessions or between observing runs, pseudo-random data can be used to mimic observations and check the entire Correlator system. Or, when observations do not use the entire Correlator system, partial system checks could also be performed in parallel.

5.2 The ALMA Correlator as a ‘neutrons detector’, comparison with other measurements

This work demonstrates that the SEU events observed in the Correlator system are not negligible. In other words the ALMA Correlator can be considered as a ‘neutrons detector’ when the CRC circuit and SEU monitoring routines are active and we advocate that using this ‘new property’ is highly desirable for the system integrity. Enhanced exposure to ionized particles and neutrons at the ALMA site was clearly demonstrated in [2]. The dose rates of the

ionizing components was found to be around 3 times higher at Pampa La Bola (4800-m, near AOS site) than in Santiago (500-m elevation) whereas the measured neutron dose rate was greatly enhanced at Pampa La Bola. The latter result showing an exposure higher than observed in other sites at similar elevations was tentatively explained by the proximity of the Chilean site to the South Atlantic Anomaly (enhancing the rôle of the primary Cosmic Rays).

More simply here, we suggest that with appropriately calibrated and dedicated equipment as in [2] it would be possible to measure the exposure to neutron particles and gamma rays within the AOS (close to or within the Correlator room to avoid shielding effect corrections) and search for any correlation with the SEU induced errors measured in the Correlator room. In addition to bringing newer information to the very first results presented in [2], this could valuably help to characterize the ALMA site and perhaps even help to estimate the effects of human exposure to neutrons and radiations.

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