Atacama
Large
Millimeter
Array

ALMA Phasing Project
Correlator Upgrades Manual

ALMA-05.11.31.05-0001-A-MAN

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1 Description

1.1 Purpose

The purpose of this manual is to describe the custom hardware upgrades to the ALMA Correlator associated with the ALMA Phasing Project. It also includes a summary of the available documentation for the cards.

1.2 Scope

This document applies to the entire Phasing Interface Card Assembly(PICA), the TTL to LVDS Converter Card (TLC) Shifter, and The One Pulse Per Second Card. Descriptions are from a higher level functional perspective, as well as from a detailed circuit perspective.

2 Applicable Document, Reference Documents, Acronyms and Definitions

Applicable documents are necessary for the understanding of this document. In some cases, they provide additional requirements which are to be incorporated into the ICD. Reference documents are supplemental and simply provide further reference for various topics. In most cases, the acronyms used in this document are consistent with ALMA defined acronyms, however additional acronyms have also been listed which are outside the scope of ALMA definitions. No distinction is made between these two uses.

2.1 Applicable Documents

The following documents, of the exact issue shown, form part of this document. In the event of conflict between the documents listed here and this document, this document shall take precedence.

Number	Document Title	Document Number

Table 2-1. Applicable Documents for this ICD

2.2 Reference Documents

Number	Document Title	Document Number
[RD 01]		
[RD 02]	ROACH FPGA Requirements and Specifications	ALMA-05.11.31.15-0002-A-SPE
[RD 03]	PIC Assembly Block Diagram	ALMA-05.11.31.11-0001-A-DWG
[RD 04]	PIC Schematic	ALMA-05.11.31.11-0002-A-DWG
[RD 05]	PIC Assembly ZDOK to QXH Adapter Schematic	ALMA-05.11.31.11-0003-A-DWG
[RD 06]	PIC Assembly Misc Cables	ALMA-05.11.31.11-0004-A-DWG
[RD-07]	PIC Assembly Bill of Materials	ALMA-05.11.31.12-A-0001-BOM
[RD-08]	PIC Bill of Materials	ALMA-05.11.31.12-A-0002-BOM
[RD-09]	PIC Assembly ZDOK to QXH Adapter BOM and Assembly	ALMA-05.11.31.12-A-0003-BOM
[RD-10]	PIC PCB Files	ALMA-05.11.31.11-0003-A-DWG
[RD-11]	PIC Assembly ZDOK to QXH Adapter PCB Files	ALMA-05.11.31.11-0006-A-DWG
[RD-12]	APP_Project_Plan, latest version	-
[RD-13]	TTL-LVDS Level Converter Schematic	ALMA-05.11.35.11-001-A-DWG
[RD-14]	TTL-LVDS Level Converter PCB Artwork	ALMA-05.11.35.11-002-A-DWG
[RD-15]	TTL-LVDS Level Converter PCB Assembly	ALMA-05.11.35.11-003-A-DWG
[RD-16]	TTL-LVDS Level Converter Bill of Materials	ALMA-05.11.35.12-001-A-BOM
[RD-17]	ATX PSU Panel	ALMA-05.11.32.11-001-A-DWG
[RD-18]	ATX PSU Panel Brackets	ALMA-05.11.32.11-002-A-DWG

Table 2-2. Reference Documents for this ICD

2.3 Abbreviations and Acronyms

AD	Applicable Document
ALMA	Atacama Large Millimeter Array radio telescope
AOS	Array Operations Site
APP	ALMA Phasing Project
ATX	Advanced Technology eXtended (standard for Personal Computers)
CAI	Correlator Antenna Input
CIC	Correlator Interface Card
GPS	Global Positioning Service
ICD	Interface Control Document

IPT	Integrated Product Team
LRU	Line Replaceable Unit
LVDS	Low Voltage Differential Signal
M&C	Monitor and Control
NRAO	National Radio Astronomy Observatory
PAI	Preliminary Acceptance In-House
PAS	Provisional Acceptance On-Site
PCB	Printed Circuit Board
PIC	Phasing Interface Card
PICA	Phasing Interface Card Assembly
PPS	Pulse Per Second
TE	Timing Event (a 48-msec timing tick which is the heartbeat of the ALMA control system)
TLC	TTL Level Change Card
UPS	Uninterruptable Power Supply
VDIF	VLBI Data Interchange Format
VEX	VLBI EXperiment
VLBI	Very Long Baseline Interferometry

3 Phasing Interface Card Assembly

3.1 Overview

This manual presents an overview of the design of the functionality of the PIC and of the documentation available for it. Future versions will present the circuit operation in more detail. A block diagram of the assembly is presented. This is followed by a short summary of the available documentation.

The Phasing Interface Card (PIC) historically has referred to the electronics module that fits into certain slots of the ALMA 64-Antenna Correlator and that serves the purposes described in **[rd 09]**. During the design process the NRAO-designed-card that serves as the "motherboard" for the PIC has also become known as the PIC. When it is necessary to distinguish between these two uses, a second acronym, PICA, has been adopted. PICA (PIC Assembly) always refers to the entire assembly consisting of the "motherboard", daughter cards, cables and hardware.

3.2 Block Diagram Description

The block diagram of the PICA is shown below. It presents the board mostly from a mechanical and electrical point of view. A second block diagram is available in Figure 4.1 of **[RD-2].** It presents the board from a signal-flow, functional point of view. Both aspects of the board are presented in the following sections.

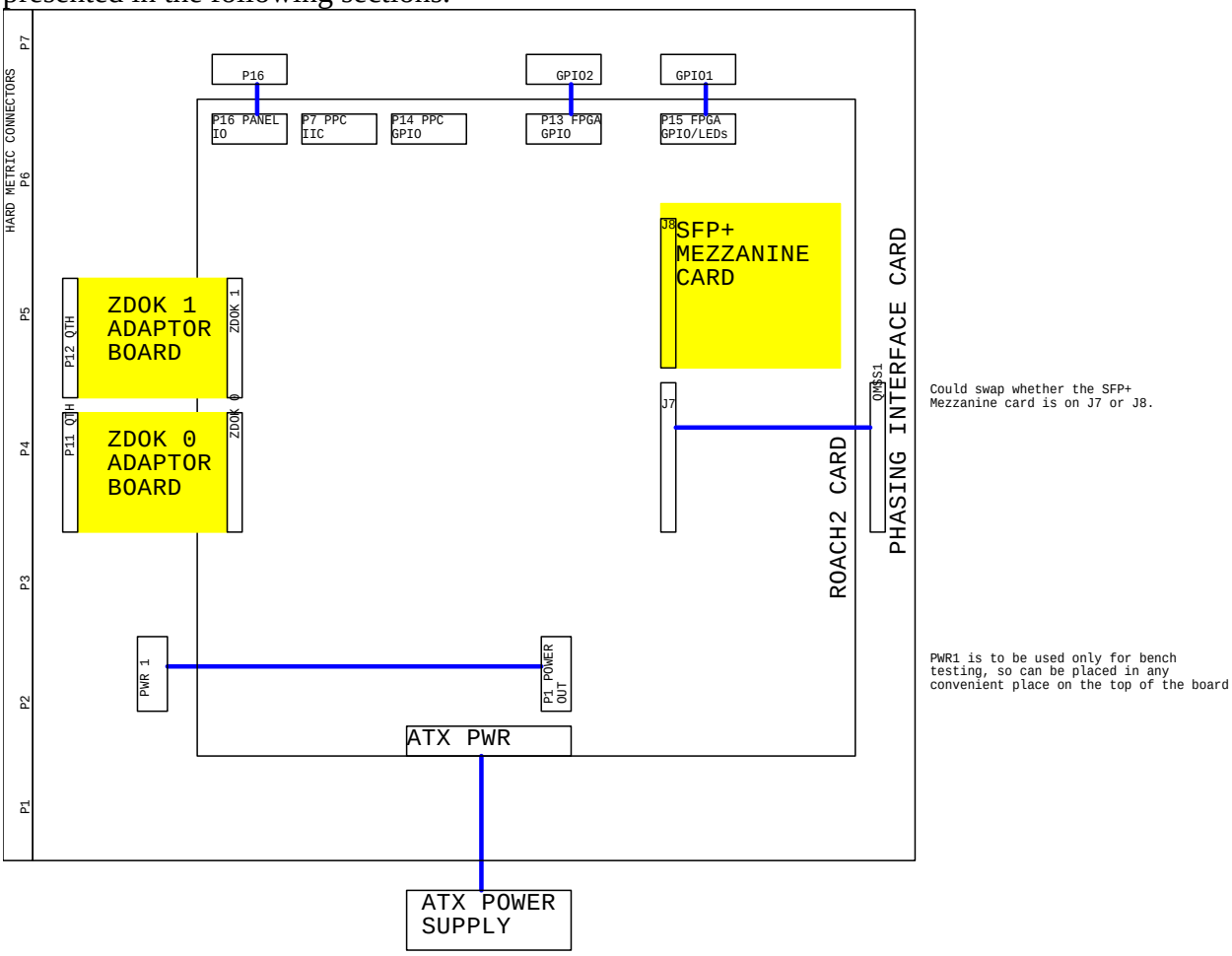


Figure 1 PIC Assembly Block Diagram

3.2.1 Mechanical and Electrical Description

As shown above the PICA consists of the following major components:

- PIC (“motherboard”)

- ROACH2 Card
- SFP+ Mezzanine Card
- Two ZDOK Adaptor Boards
- Six cables (shown in blue)

The function of each of these is described in the following five sections. A photo of the assembled prototype is show in the figure below.

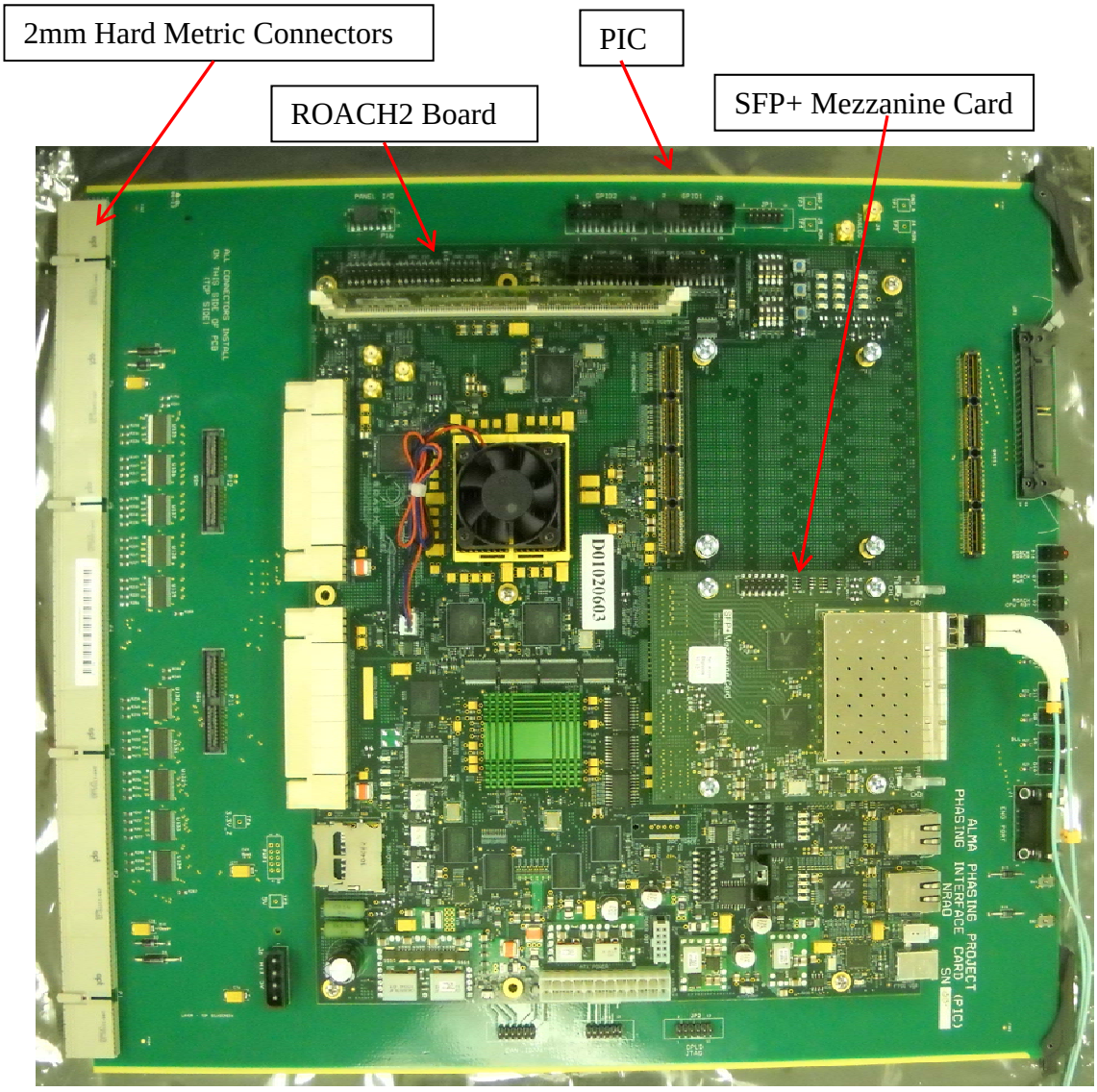


Figure 3 Phasing Interface Card Assembly (PICA). Electrical cables not installed.

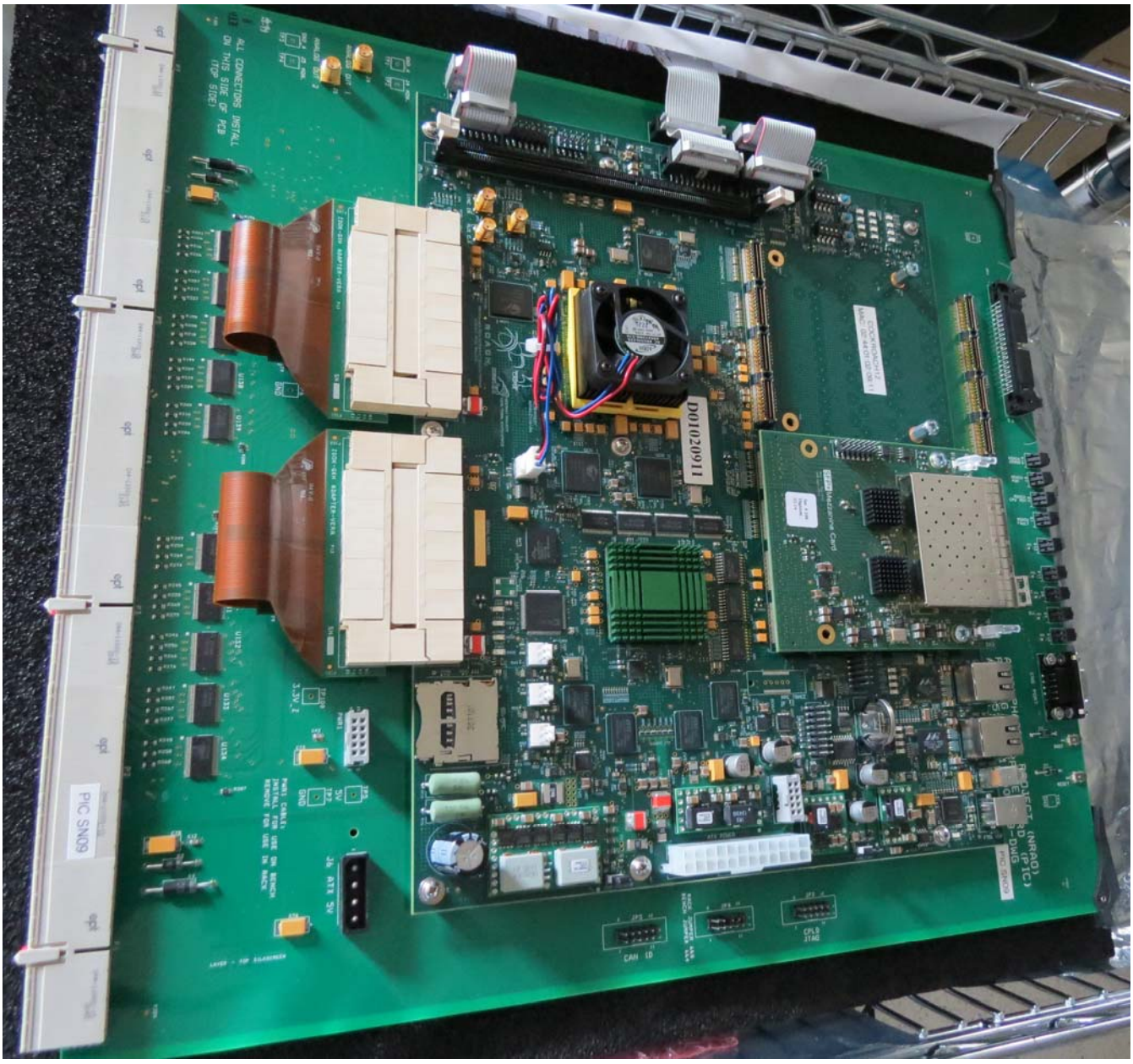


Figure 4 PICA with ZDOK and Microprocessor Cables Installed

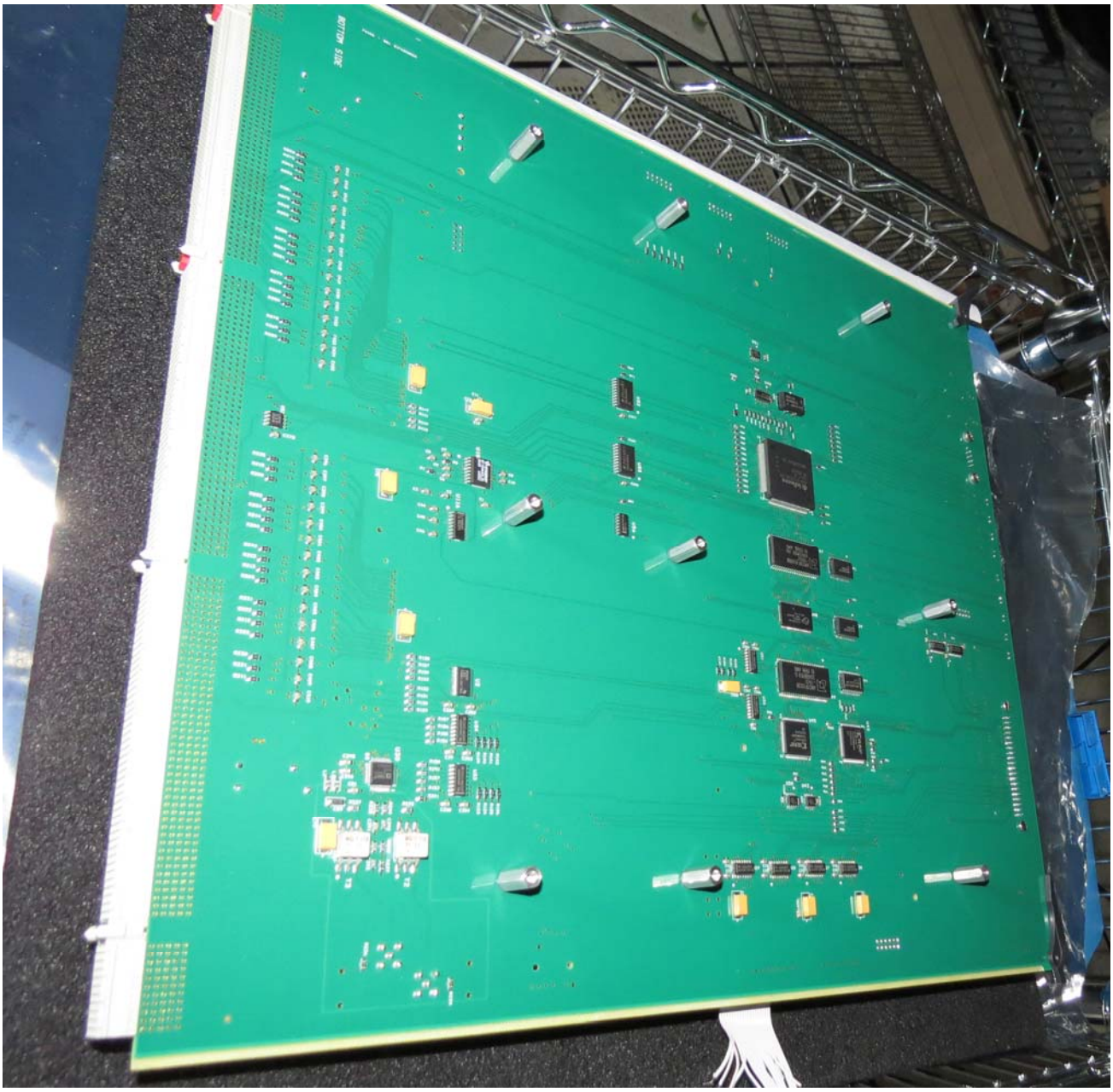


Figure 5 Backside of PIC

3.3 Phasing Interface Card (PIC)

The PIC serves as a motherboard on which all the rest of the components are mounted. It also provides the interface to the Correlator Bin's backplane via the hard-metric 2mm connectors P1 through P7. Several connectors are provided for interface with the ROACH2 Card. P11 and P12 on the left-side of the drawing make the phased-sum signals available to the ROACH 2 card via ZDOK Adaptor Boards. P16, GPIO2 and GPIO1, along the top of the drawing, are provided for communication with the FPGA on the ROACH2 board. QMSS1, on the right side of the drawing is used to receive test signals from the ROACH2 board. Its outpus are buffered and connect to test points on the front edge of the card (not shown).

The backside of the PIC contains the C167 microprocessor components. These mimic the functionality of the other control cards in the correlator. This gives the PIC the same look and feel as the other ALMA Correlator control cards.

3.4 ROACH2 Board

This is a commercially available board designed for signal processing. It is widely used in the astronomical community. See the following link for a more detailed description.

https://casper.berkeley.edu/wiki/ROACH2

It has a large Xilinx FPGA for signal processing and a PowerPC for interfacing to the FPGA. It also has provisions for two mezzanine cards. Design information for this board will be attached to the EDM entry for this manual. In the APP application, its primary function is to format the phased-sum data into VDIF frames for recording.

3.5 SFP+ Mezzanine Card

This is also a commercially available board. It interfaces to the ROACH2 and provides four ports for 10 GbE optical communications conformant with the SFP+ standard. In the APP application, one port is required to transmit the formatted, phased-sum data to the recorders via the Fiber Mux and Demux. The port must be populated with an SFP+ module to drive a fiber. This module is included in the PICA BOM **[RD 07]**. Design information for this board will be attached to the EDM entry for this manual.

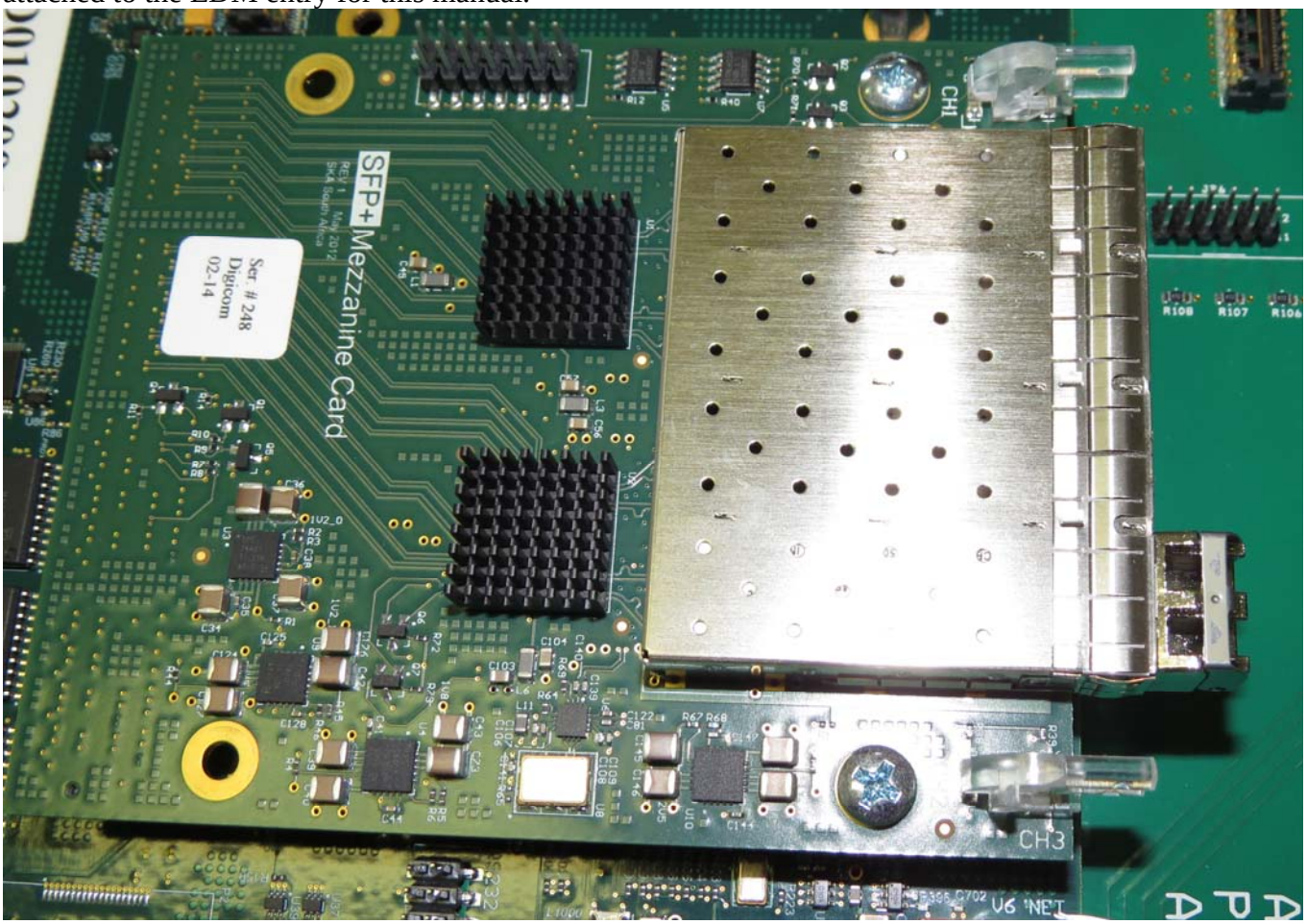


Figure 6 SFP+ Card on PICA

3.6 ZDOK Adaptor Boards (ZDOK 1 and ZDOK 2)

3.6.1 Introduction

These two identical boards route the phased-sum signals from the PIC to the ROACH2. These were designed by NRAO. Electrically, they preserve the high-quality impedance control of the connectors on either end. Mechanically, they are constructed using "flex-board" and so limit mechanical stresses which would exist with a "hard" connection. The boards also route power from the Roach to the PIC.

3.6.2 Installation

The below photo shows two ZDOK Boards installed on the PICA.

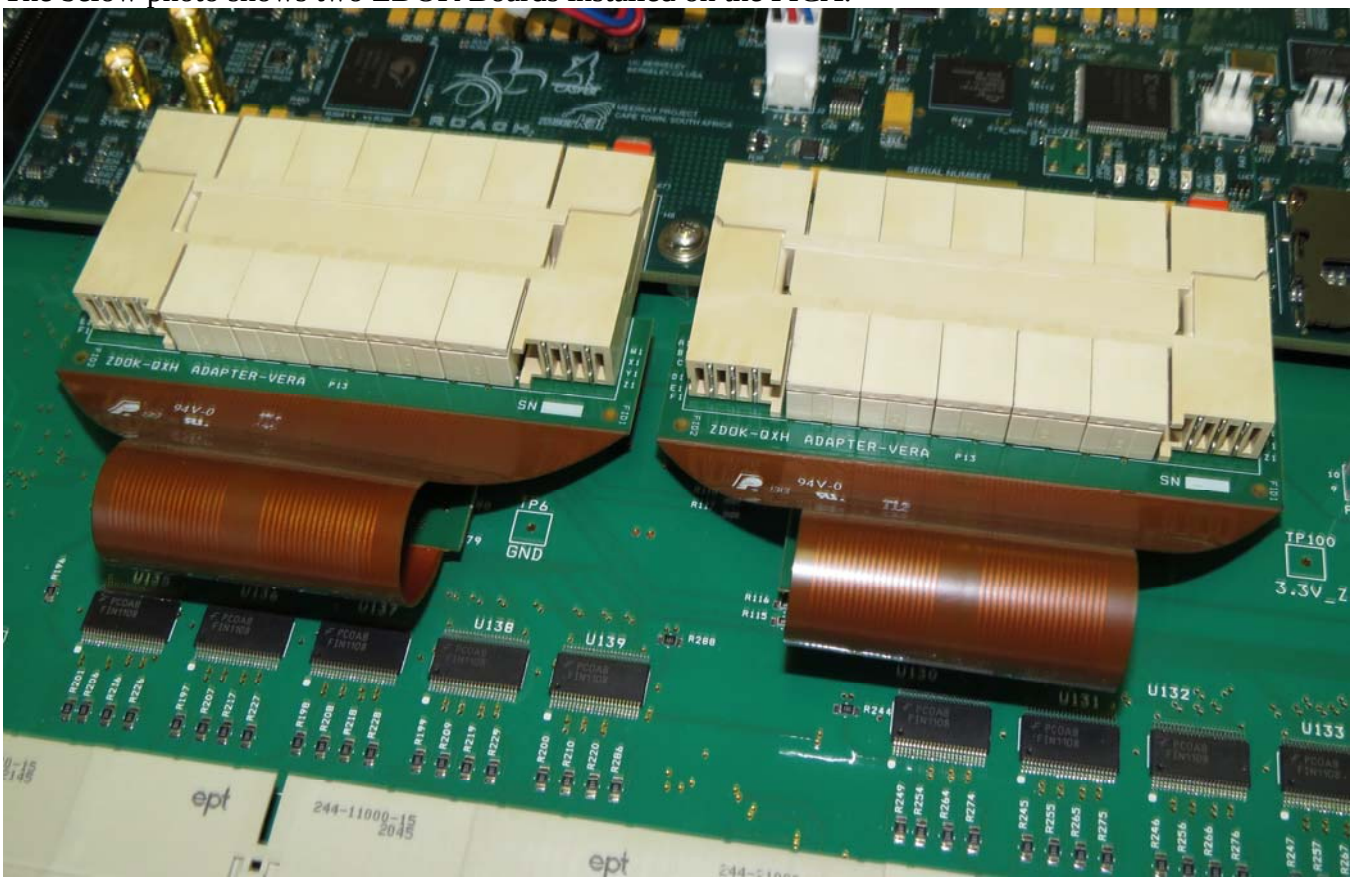


Figure 7 ZDOK Adaptor Boards on PICA

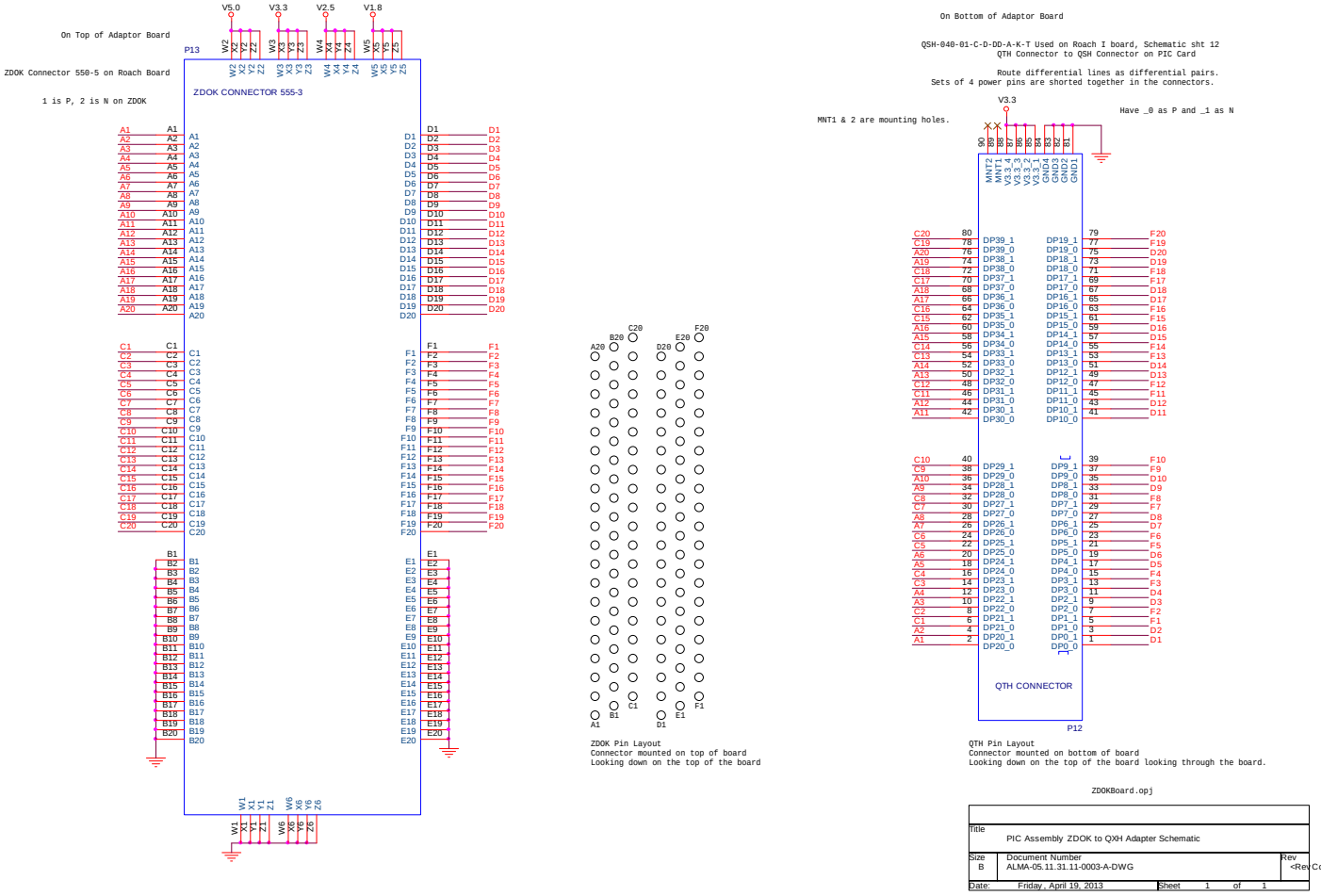


Figure 8 Schematic of ZDOK Board

3.6.3 Schematic

The above schematic shows a simple point to point wiring between the ZDOK connector to the Roach board and the QTH connector to the PIC.

3.7 Miscellaneous Cables

3.7.1 Introduction

The three ribbon cables in the below photograph, provide a communications pathway between the PIC and ROACH2. The communications is directly between the microprocessor system on the PIC and the FPGA on the ROACH2.

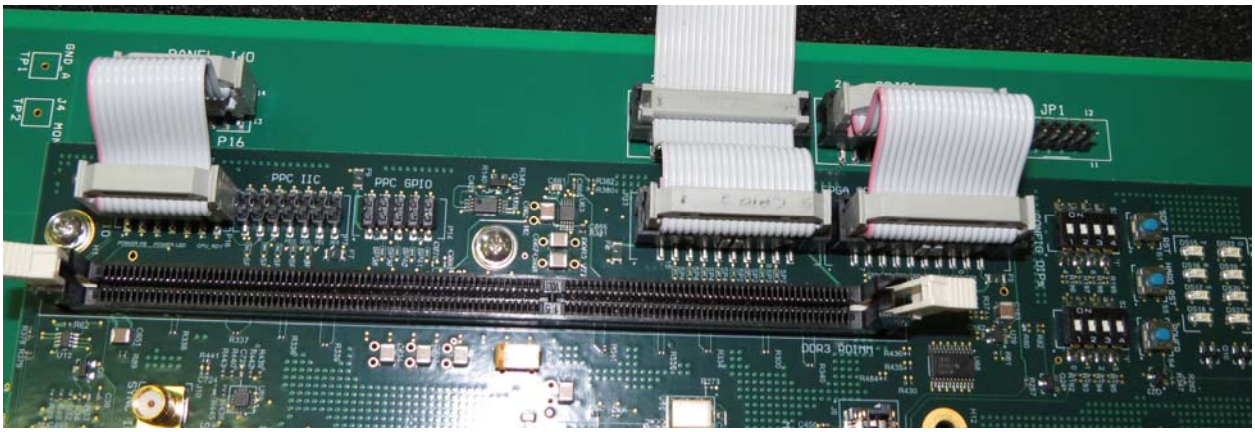


Figure 9 Three Cables for Microprocessor Communications. L to R: P16, P13, P15

3.7.2 P13 and P15 Cable Pinout

The signals on the cables are:

P13

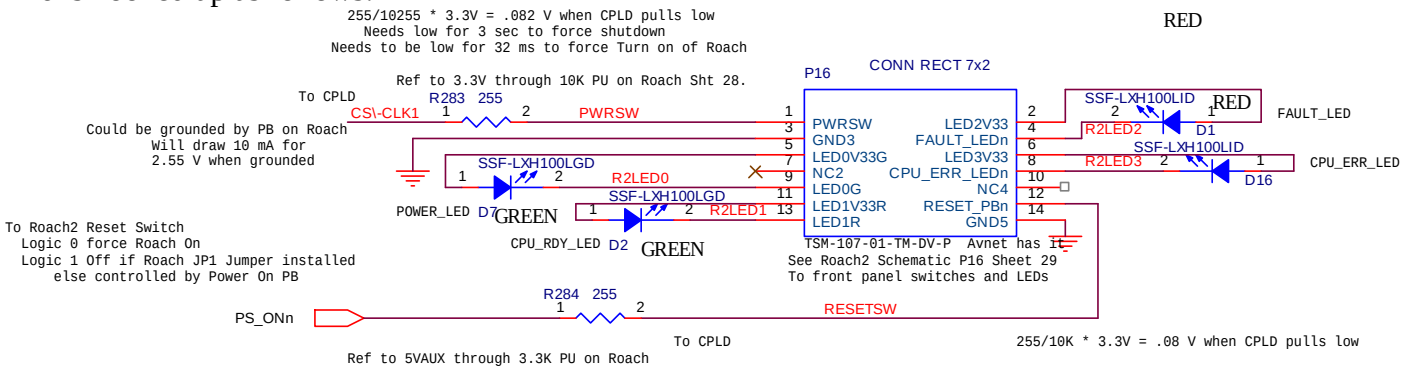
Pin	Function
1	1.5V out to PIC
3	CS\-CLK0 from uP
5	CCLK0 from uP
7	ROACHTP1 to uP
9	ROACHTP2 to uP
11	WRITE\ from uP
13	Spare output from uP
15	PROG\ from uP
17	CTRL/DATA from uP

P15

Pin	Function
1	1.5V out to PIC
3	Data Bus bit 7 from uP
5	Data Bus bit 6 from uP
7	Data Bus bit 5 from uP
9	Data Bus bit 4 from uP
11	Data Bus bit 3 from uP
13	Data Bus bit 2 from uP
15	Data Bus bit 1 from uP
17	Data Bus bit 0 from uP

3.7.3 P16 Pinout and Functionality

P16 is hooked up as follows:



This provides for status LEDs. The control for turning the Roach On and Off is via Pin 12.

3.7.4 PWR1 Connector

The cable between the PWR1 connector on the PIC (bottom right) and the P1 Power Out connector on the Roach is used only for testing. It can provide power to the microprocessor on the PIC from the ROACH2. See the below figure.

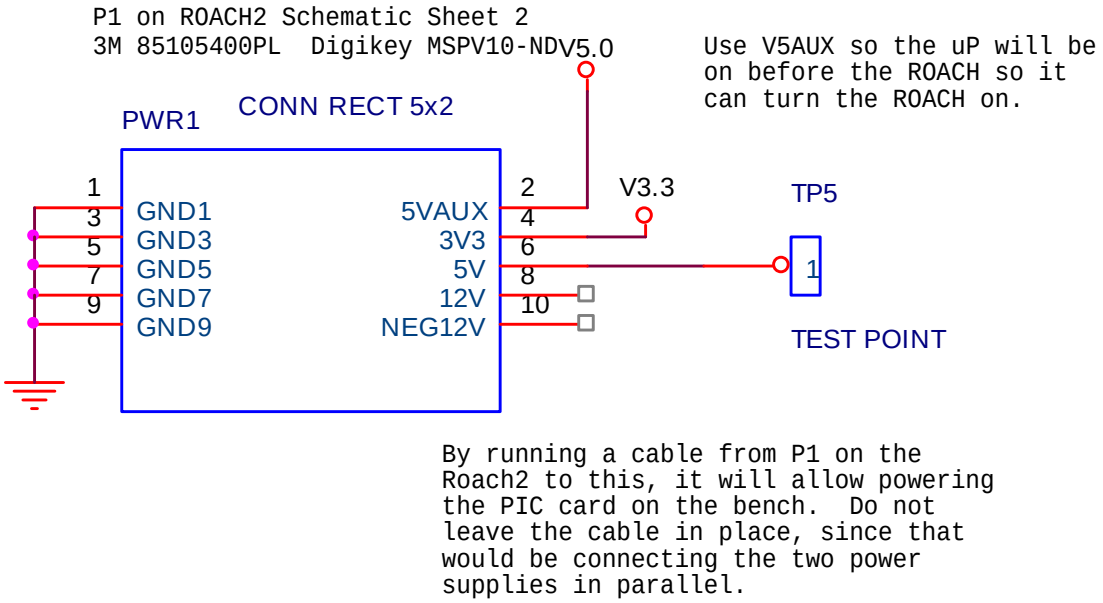


Figure 10 PIC PWR1 Connector

3.8 ATX Power Supply

An ATX Power Supply is used to power the Roach Board. There is one dedicated to each PICA. These supplies are commonly used in PCs. The supply inputs 48 Volts instead of the usual AC Voltage. The supply is mounted on a plate which is mounted on the side of a correlator rack.

See RD-17 and RD-18 for the ATX PSU Panel and the ATX PSU Panel Brackets.

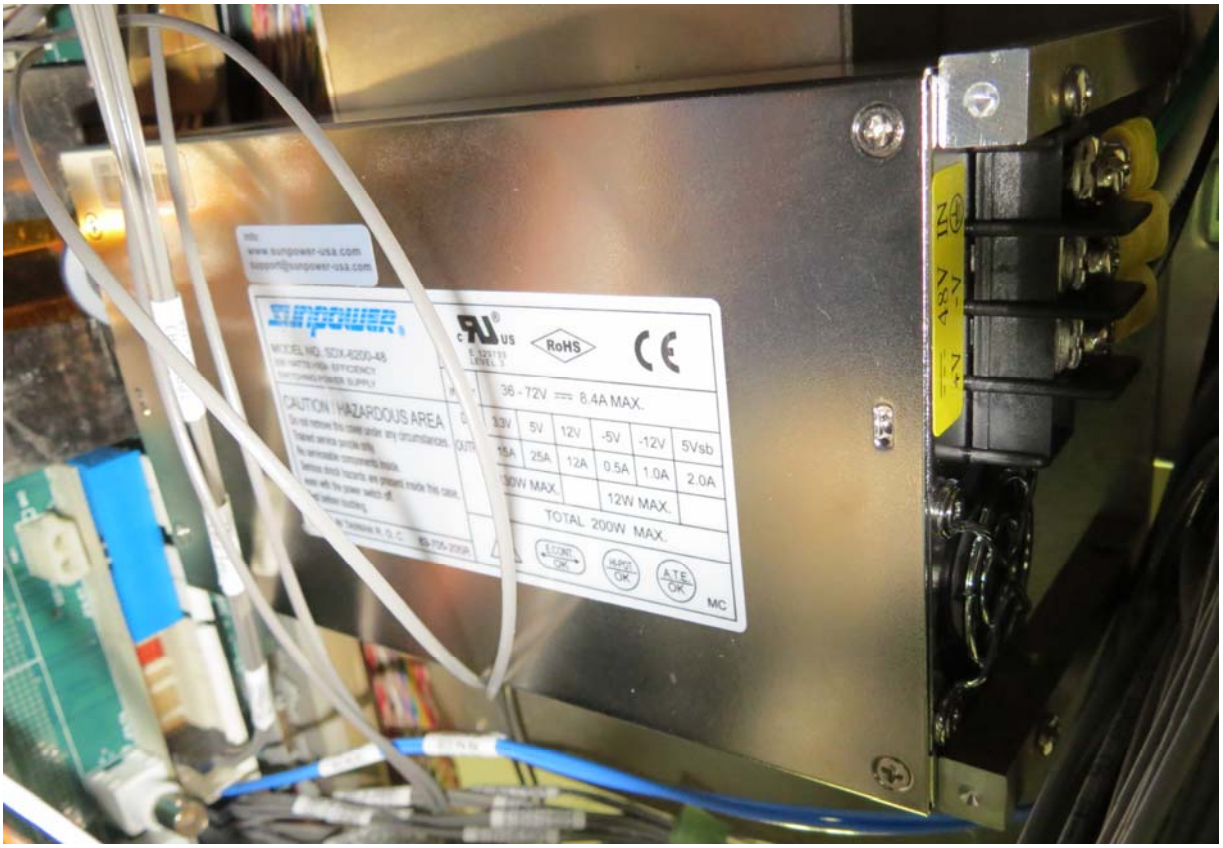


Figure 11 ATX Power Supply Mounted in Correlator Rack.

The supply is connected to the correlator's 48volt bus. This provides the ability to shut the ROACH2 board down via the 167 microprocessor to save power. It also maintains the system safety feature of shutting down when the -48-volt bus is powered down due to anomalies

detected by the Quadrant Control Card.

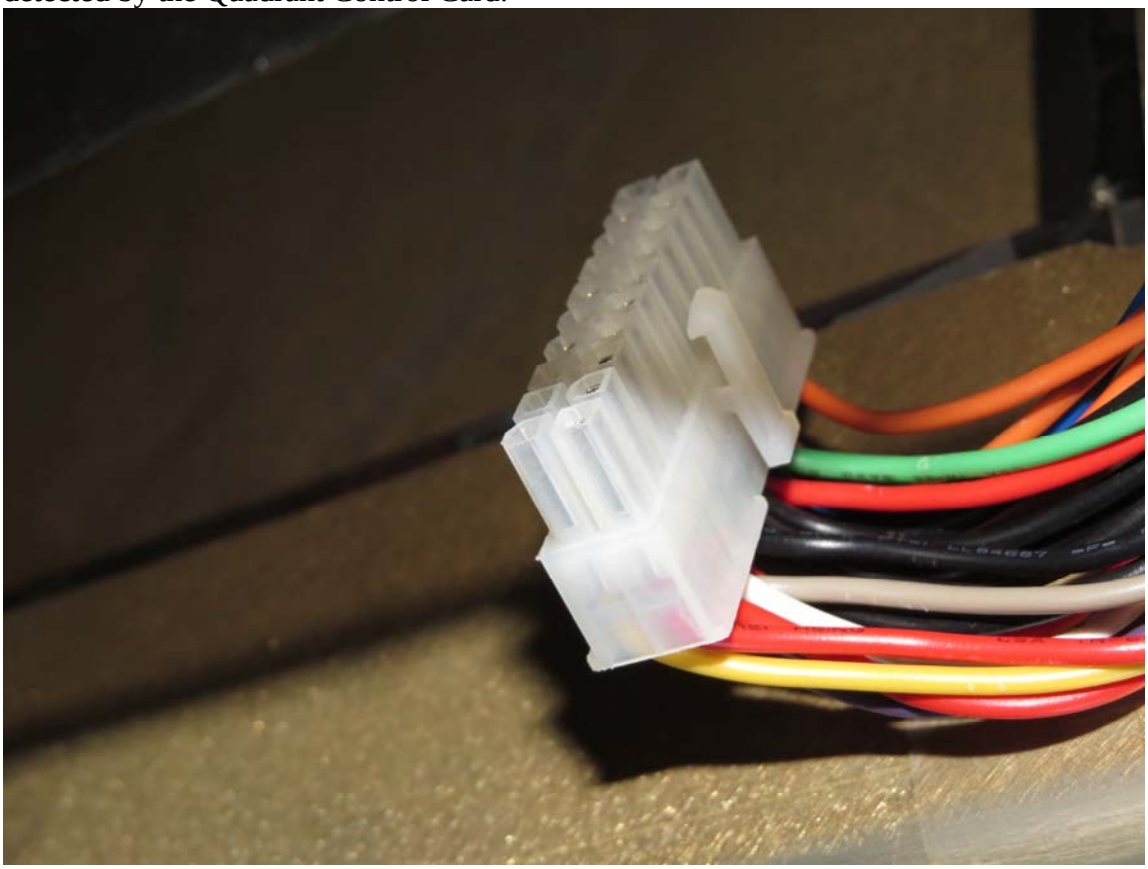


Figure 12 Cable from ATX Power Supply

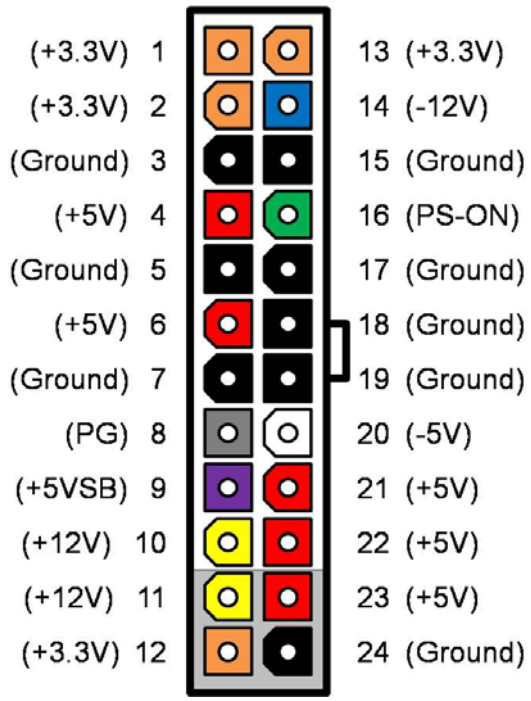


Figure 13 ATX Cable Pinout

The cable and its pinout are shown above. The PS-ON line is used to turn on and off the ATX supply from the PIC.

3.9 Functionality to Turn the Roach Board On and Off

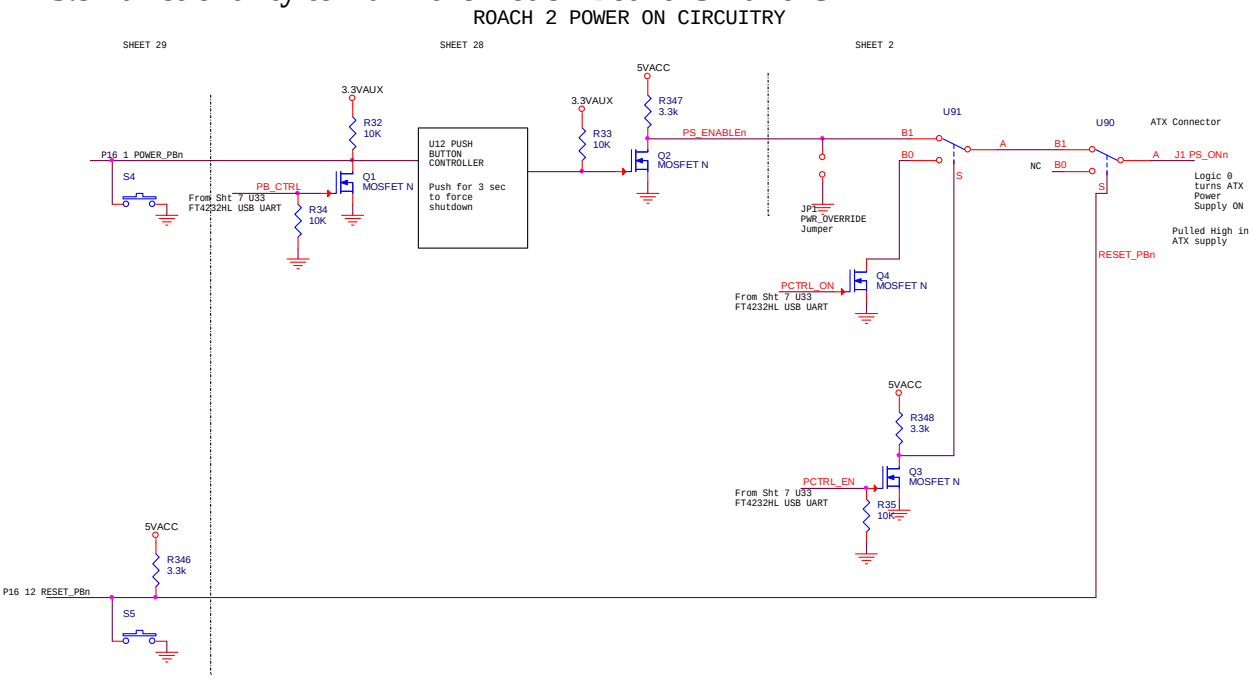


Figure 14 Roach 2 Power On Circuitry

The Roach 2 can be turned On and Off by controlling the PS_ON signal to the ATX power supply. The above schematic summarizes the Roach 2 Board circuitry for controlling this signal.

Power Control Options:

1. Controlled via USB UART
   RESET_PBn momentarily going low turns off the ROACH momentarily.

2. Controlled by holding low POWER_PBn for 3 seconds.
   RESET_PBn momentarily going low turns off the ROACH momentarily.

3. Put Jumper JP1 in place.(recommended option for PIC)
   When RESET_PBn is logic 1 the unit is turned ON.
   When RESET PBn is logic 0 the unit is turned OFF.

Option 3 is used to allow the C167 to control the Roach power via P16 pin 12.
The Engineering port functions ROACHON and ROACHOFF are used to control this bit.

3.10 PICA Signal Flow Description

3.10.1 Introduction

The signals present on the PICA can be classified into four categories: data, timing, monitor and control, test. The paragraphs below present a functional overview of the PICA and describe the various signals present with reference to Figure 4.1 in **[RD 02]**. For convenience, this drawing is reproduced on the following page. Note that, in this figure, dotted lines are used to denote the PIC, ROACH2 and the FPGA on the ROACH2. The FPGA does most of the signal processing. Also for convenience, the signal names are highlighted in **bold** to make them easier to find in the text.

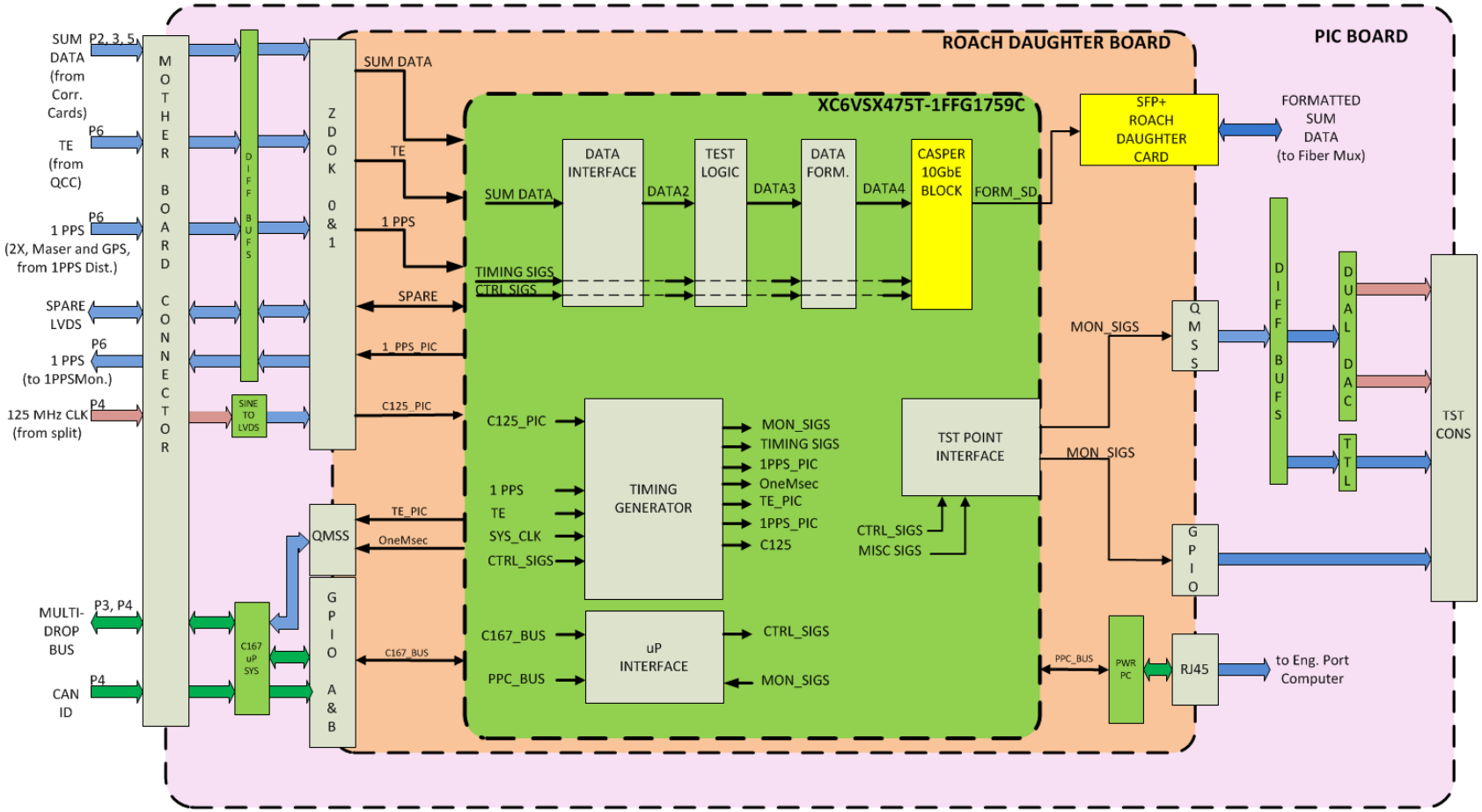


Figure 3-15. ROACH signal flow block diagram. Reproduction of Figure 4.1 from [RD 02].

The main purpose of the PICA is to format the phased sum data into frames suitable for recording. The framing requirements are detailed in **[RD 02]**. It must also maintain the "look and feel" of other board of the correlator to simplify software development and mechanical constraints. These requirements are accomplished by providing the PIC "motherboard" and the ROACH2 board. The PIC includes the standard ALMA Correlator microprocessor and the standard connection to the Correlator Bin Motherboard. Thus, it is "just another card on the multi-drop bus", greatly simplifying monitor and control from both the Correlator Control Computer and the Engineering Port Computer. It also has the standard interfaces to the correlator timing signals "TE" and "125 MHz". The ROACH2 provides the signal processing power, in the form of a large FPGA, for formatting the data.

3.10.2 Data Signals

Two-bit samples from each of 32 sub-bands at a data rate of 125 Ms/s are routed from the Correlator Card sum port connectors on the correlator motherboards to the PIC motherboard connectors. These are labeled **SUM DATA** in the above figure. These signals flow through differential buffers to protect the expensive FPGA from large external transients. They then flow through the ZDOK connector to the FPGA on the ROACH. They are captured on the FPGA and transformed from differential to single-ended signal in the Data Interface block. They then flow to the test logic. This logic has several capabilities. It can monitor the statistics of the incoming data (the number of occurrences of each of the four possible states for each sample stream), test the data against a known pseudo-random data pattern and generate various flavors of test data to substitute for the Sum Data in the downstream blocks. The Data Formatter combines the Sum Data with a header that provides time and station information. The CASPER 10 GbE Block further formats the data stream for 10 GbE transmission. The output of this block is routed to the SFP+ ROACH Daughter Card where it is converted to an optical signal for transmission to the recorders via the Fiber Mux/Demux sub-system.

3.10.3 Timing Signals

As originally designed, the 64-Antenna ALMA correlator uses the **TE** signal as its main time reference. (The TE signal is a pulse that occurs precisely at 48 msec intervals.) VLBI requires a 1-PPS signal for its timing purposes. The **TE** signal is exactly coincident with the **1-PPS** signal at seconds 0, 6, 12, … 54 of every minute. Rather than design a second precision time distribution system in the correlator for 1-PPS, the PIC uses TE pulse, along with a command

from the CCC, to generate an internal 1-PPS signal. The TE input signal is seen near the top left of the above figure. It is routed through the motherboard connector, through a buffer, and through a ZDOK connector to the FPGA. In the FPGA it is the primary time reference to the Timing Generator which produces the time signals required for formatting the Sum Data.

Two **1-PPS** signals are routed from the backplane to the FPGA. One is derived from the Maser and the other from a GPS receiver. The FPGA compares these signals against its internally generated 1-PPS signal and provides time difference measurements which can be read over the CAN bus by the CCC. High level software can thus verify the timing of the PICA. A copy of the internally generated **1-PPS** is provided on the motherboard connector for monitoring purposes.

The clock for the correlator is a 125 MHz sine wave. It has the name **C125** on the block diagram. It is derived from the primary frequency reference for the site which, for VLBI, is the Hydrogen Maser. At the input connector, this signal is a sine wave. It is converted to single-ended and differential square waves on the PIC. One of the differential copies is used on the FPGA as the primary frequency source for time keeping. A higher frequency clock is used in the formatter to combine the sum data with the header.

The FPGA generates two timing signals which are transmitted to the C167 microprocessor. These are the **TE_PIC** and **OneMsec** signals, which are tied to microprocessor interrupt lines.

3.10.4 Monitor Signals

To preserve the look and feel of the correlator from the software point of view, the PICA is connected to the **Multi-Drop Bus** as shown in the bottom left corner of the above figure. Like other boards in the correlator, the PIC gets is **CAN ID** from the DIP switches located on the correlator motherboard. This is also shown in the bottom left of the above figure.

The C167 microprocessor on the PIC control a bus, labeled the **C167 Bus**, to communicate with the FPGA on the ROACH2. This bus has the same topology as other busses which communicate with other FPGAs in the correlator.

Another microprocessor, a PowerPC, on the ROACH2 board also communicates with the FPGA over a bus labeled **PPC_Bus** in the bottom-right part of the above figure. This microprocessor is responsible for loading the FPGA personality at power up. It also provides a “back door” into the FPGA for debugging purposes, both during development and operations.

3.10.5 Test Signals

Several monitor signals are driven from the **TST POINT INTERFACE** located in the middle-right of the above figure. These signals are buffered and routed to the test connector in the middle-right part of the above figure. Two groups of signals drive Digital to Analog Converters and can provide 4-bit analog representations of whatever bits are selected in the FPGA. This feature may be useful in future upgrades by providing an analog representation of sum data.

3.11 Available Documentation

The Reference Documents Table, Table 2-2, on page 7 lists the documentation available for the PICA in the time frame of the CDR. This paragraph provides a short description of the relevant documentation. A block diagram and BOM for the PIC Assembly are available (**[RD 03]** and **[RD 07]** respectively**).** Schematics, BOMs and PCB files are available for the PIC and the ZDOK to QXH adapters (**[RD 04], [RD 05], [RD 08], [RD 09], [RD 10], [RD 11]**). A requirements and specifications document for the FPGA personality is available **[RD 02]** and has been instrumental in enabling development by individuals at three institutions. A schematic that includes electrical and assembly information for the miscellaneous cables is available **[RD 06].** Eventually, **[RD 01]** will become the PIC Assembly Requirements and Specifications.

This tells what the various files are for the PIC Card. See MMA Correlator\APP\PIC
PICROACH2B.DSN - This is the primary schematic of the PIC Card
PIC.DSN This is the old initial version of the PIC card.
PICCABLES.DSN - This gives the schematic of cables used in the PIC assembly.
PICCARDLAYOUT.DSN - This gives a drawing of the card layout for the PIC assembly.
PICSYSTEMDIAGRAM.DSN - This gives a system level diagram of the Black Hole Two Antenna Correlator/PIC Test Fixture.
PICTESTFIX.DSN - This has:
The cheat sheet for the new registers for ASUMMID.
The analog sum block diagram. The ATX to PWR1 Cable. The Bin layout. The Block Diagram. The CI Changes.
The LoopBack Delay diagram. The Roach Xilinx.
ROACH2ONOFF.DSN - This shows a schematic representation of the ON/OFF logic of the Roach Board.
ZDOKBOARD.DSN - This is the schematic of the flexible board that connects the Roach ZDOK to the PIC.
ALMA-05.11.31.12-0001-A-BOM - The BOM for the PIC assembly.

ALMA-05.11.31.12-0002-A-BOM - The BOM for the PIC Card.

4 Additions to Existing Cards to Accommodate the PIC

This documents modifications to the firmware and software of baseline correlator cards to accommodate the addition of the PICs to the system.

4.1 QCC Xilinx (NEWQCC) Modifications

The TE for the PIC comes from the QCC. The outputs used were originally labeled QCC0 and QCC1. These outputs were unused. These outputs did not have integer and fractional delays out, as did the TE outputs to the FA, LTA, and STA cards. The modification adds the integer and fractional delay to these outputs.

The fractional delay is accomplished by using various phases of clocks. It is critical that the elements be close together on the Xilinx to minimize routing delays. Thus floor planning is used to control the routing. The below chart details the floor planning for the TE outputs for FA[1:0], LTA[15:0],STA[15:0}, and the added PIC[1:0]. PIC[1:0] is highlighted in green on the second chart.

													COLUMNS			
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	1															
P3R22	2	LTA15	LTA15	LTA15												
P3R21	3	LTA14	LTA14	LTA14												
P3R20	4	LTA13	LTA13	LTA13												
P3R19	5	LTA12	LTA12	LTA12												
P3R18	6	LTA11	LTA11	LTA11												
P3R17	7	LTA10	LTA10	LTA10												
P3R16	8	LTA9	LTA9	LTA9												
P3R15	9	LTA8	LTA8	LTA8												
P3R11	10	LTA7	LTA7	LTA7												
P3R10	11	LTA6	LTA6	LTA6												
P3R9	12	LTA5	LTA5	LTA5												
P3R8	13	LTA4	LTA4	LTA4												
P3R7	14	LTA3	LTA3	LTA3												
P3R6	15	LTA2	LTA2	LTA2												
P3R5	16	LTA1	LTA1	LTA1												
P3R4	17	LTA0	LTA0	LTA0												
	18	STA15		STA14		STA13		STA12	STA11	STA10		STA9	STA8			
	19	STA15		STA14		STA13		STA12	STA11	STA10		STA9	STA8			
	20	STA15		STA14		STA13		STA12	STA11	STA10		STA9	STA8			
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
		P3R1		P2R25		P2R24		P2R23	P2R22	P2R21		P2R20	P2R19		COLUMNS	

Shows row for wafer from QCC

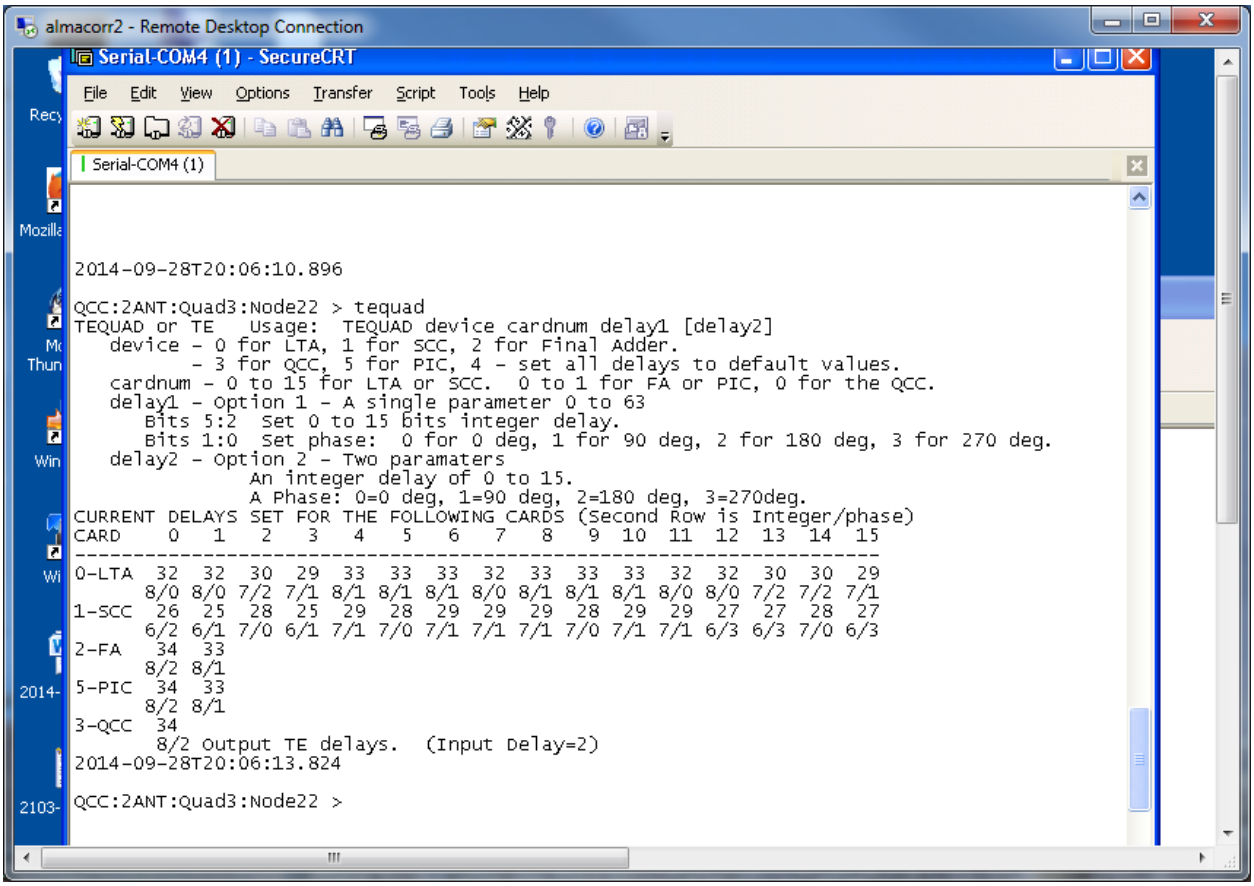
Floor Planning for QCC Xilinx Left side

18	19	20	21	22	23	24	25	26	27	28	29	30			
													1		
													2		
													3		
													4	R	
													5	O	
													6	W	
													7	S	
													8		
													9		
													10		
													11		
										FA1			12		
										FA0	FA1		13		
										QCC	FA0	FA1	14	P4R5	
											QCC	FA0	15	P4R4	
										PIC1		QCC	16	MasterAuxT	
										PIC0	PIC1		17		
STA7	STA6		STA5	STA4	STA3			STA2	STA1	STA0	PIC0	PIC1	18	P4R2	
STA7	STA6		STA5	STA4	STA3			STA2	STA1	STA0		PIC0	19	P4R1	
STA7	STA6		STA5	STA4	STA3			STA2	STA1	STA0			20		
18	19	20	21	22	23	24	25	26	27	28	29	30			
P2R14	P2R13		P2R12	P2R11	P2R7			P2R6	P2R5	P2R4					

Floor Planning for QCC Xilinx Right side
Note the QCC output rows P4R2 and P4R1 are shown as where the LVDS cables can be connected.

4.2 QCC C167 Software Modification

The QCC software function TEQUAD was modified to allow the adjustment of the TE delay to the PIC.
This functions in a manner similar to the adjustment of the TE to the other cards. This is explained in the below screen shot of the function.



To adjust the PIC TE delay, a typical command would be:
TEQUAD 5 0 34
Where 5, specifies the PIC, 0 card 0, and 34 the delay.
The two lsb's of the delay give the fractional delay, and the remaining bits the integer delay. For example 34 is binary 100010 gives a fractional delay of 2 and an integer delay of 8.
Note the PIC should not care about the integer delay.
The fractional delay can be adjusted for good capture. The PIC can be used for viewing the capture in the Roach Xilinx.
Once a delay is decided on, it can be made a default by recompiling the default delays in qccmon.c.

4.3 Correlator Card Xilinx Modifications

The correlator card Xilinxs ASUMEND, ASUM2ND, and ASUMMID. Contained the initial hooks for providing for the summing. This is shown in the below diagram:

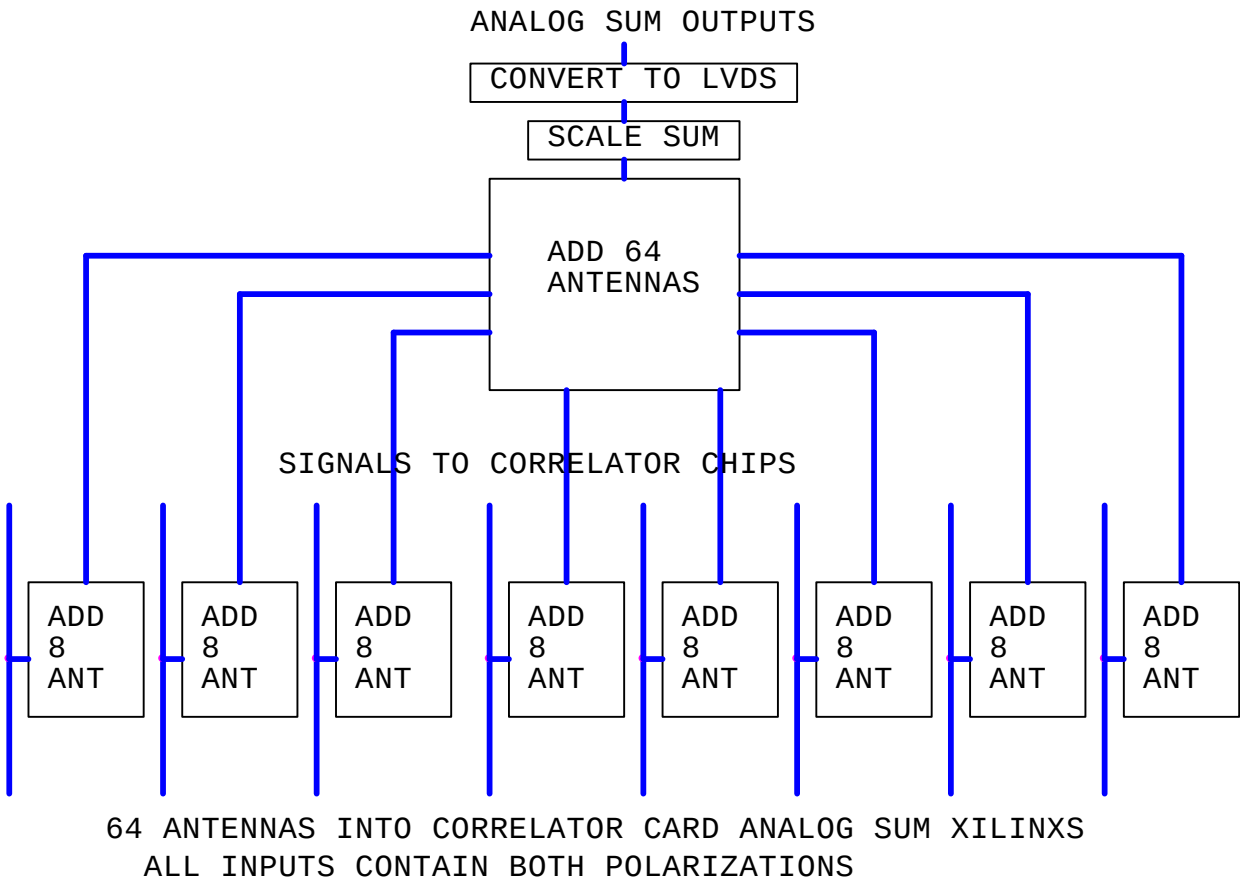


Figure 16 Diagram of Signal Summing in Correlator Card

The following diagram includes modifications were made to ASUMMID to accommodate the current design.

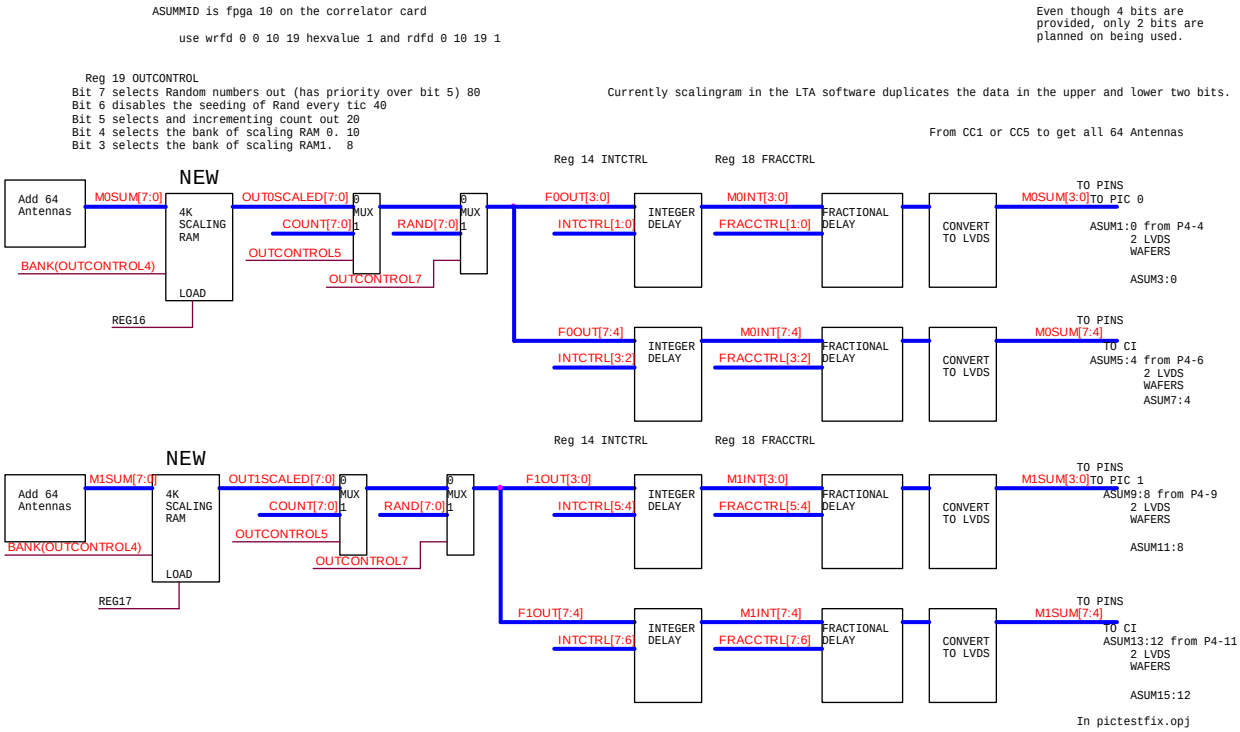


Figure 17 ASUMMID Modifications

The adding of the 64 antennas is unchanged from the original design.
A new addition is a 4K scaling RAM. This allows the scaling of the data based on whatever scheme is desired. Downloading tables into the RAM is implemented in LTA software.
The output of the RAM is then routed to a mux. The mux can select a count or random numbers for test purposes. The 8 bit number is split into two 4 bit numbers, one for the PIC and one for the path back to the CI card. One would expect these normally to be identical. These then go through integer and fractional delays before being converted to LVDS. The LVDS signals go to the PIC or CI card.

4.4 Correlator Interface Card Modifications

The CI Card had its Xilinx modified to allow the loopback of the sum output from the correlator card back into the input path as Antenna 63. This is diagrammed below:

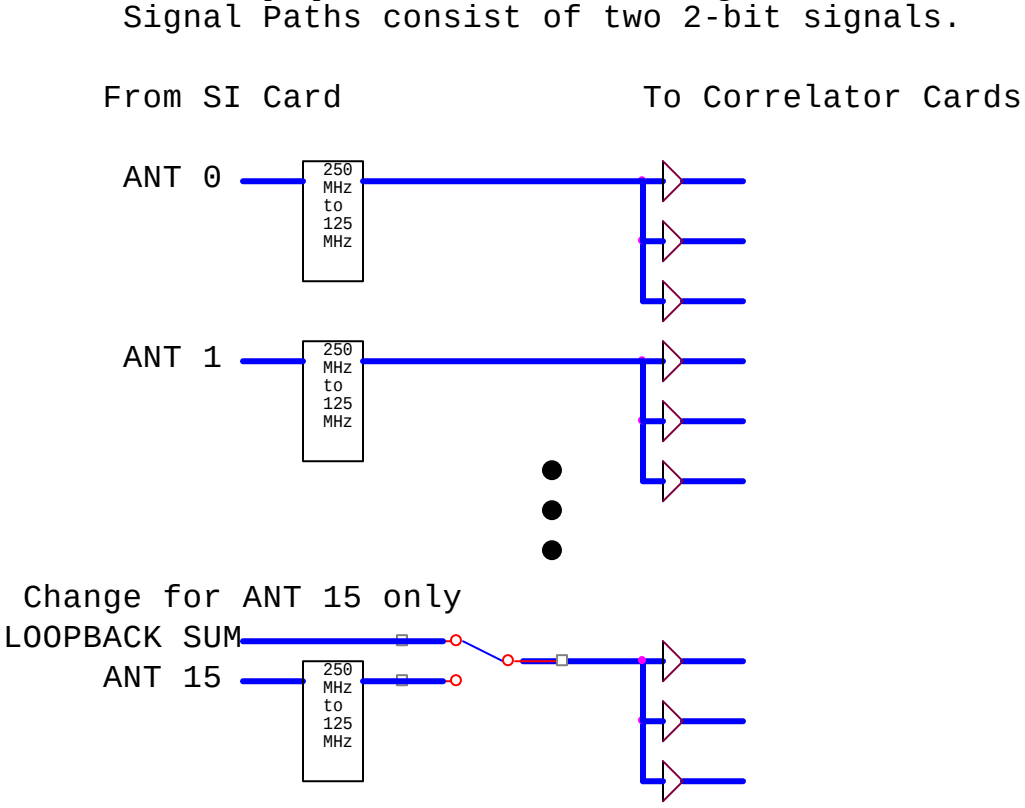


Figure 18 CI Card Modifications

The delays in this path are shown in the below figure.

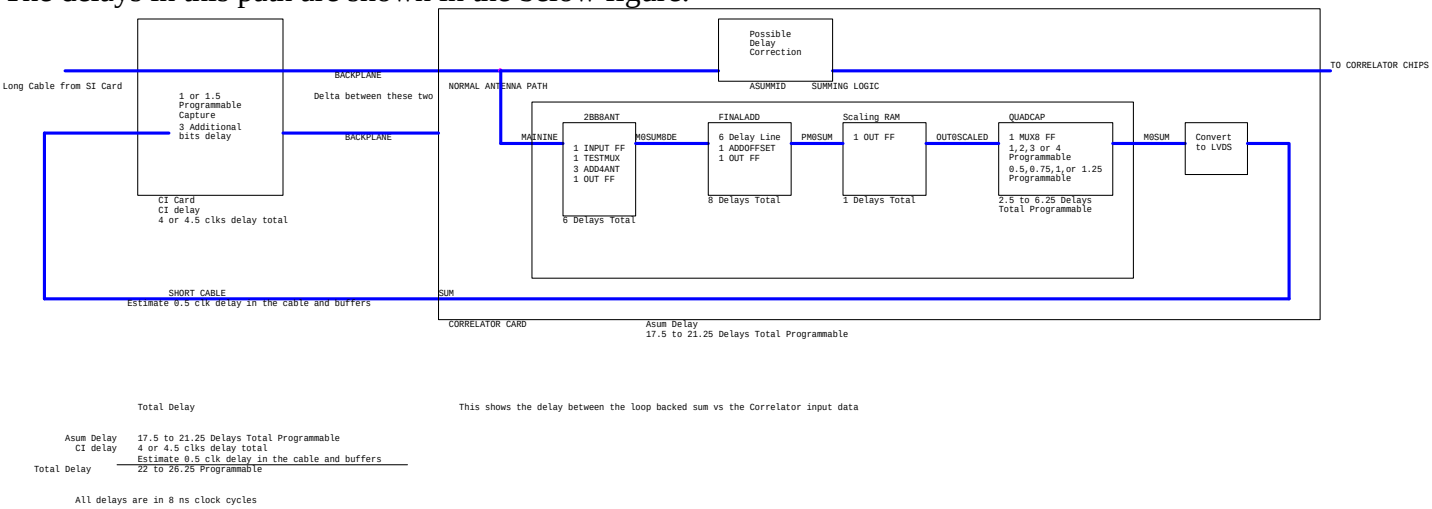


Figure 19 Delays in CI Feedback Path

The added delay can be removed by post processing software.

4.5 Changes to Corrmonitor in the C167 Software

Corrmonitor is the section of code that is common to all the control cards.
Changes were made to allow the recognition of the new control cards the PIC and OPS cards. These changes were compiled into the new cards. The old cards will work fine without having their corrmonitor code updated. However when the old cards are updated to the latest corrmonitor, they should work fine as well.

5 ONE PPS Card

5.1 Introduction

A single one PPS distribution card is added. This card is physically identical to a Final Adder (FA) card. Unique software is added to allow it to function on the LTA bus with the ID OPS. There are also custom Xilinx personalities.

The function of the card is to input a single LVDS TE from the MASER and GPS. These come from the TLC card. The two signals are buffered and 8 LVDS copies are sent out to the 8 PIC cards in the four quadrants.

The card can be placed in any vacant FA slot. Note if placed adjacent to a QCC, it will not require a separate cable for the multi-drop bus.

5.2 Microprocessor Code

In Wincvs there is a project for loading the C167 microprocessor titled Keil/Projects/One-PPS-Distributor.

5.3 Xilinx Personalities

In Wincvs, there is custom code for the fa-in-x and faoutnb Xilinx personalities in FPGA-CPLD/64AntSystem/One-PPS-Distributor.
The remaining Xilinx personalities should be loaded with the standard Final Adder Personalities. These are used for timing signal distribution.

6 TTL Level Change (TLC) Card

6.1 Introduction

Reference:

[RD-13]	TTL-LVDS Level Converter Schematic	ALMA-05.11.35.11-001-A-DWG
[RD-14]	TTL-LVDS Level Converter PCB Artwork	ALMA-05.11.35.11-002-A-DWG
[RD-15]	TTL-LVDS Level Converter PCB Assembly	ALMA-05.11.35.11-003-A-DWG
[RD-16]	TTL-LVDS Level Converter Bill of Materials	ALMA-05.11.35.12-001-A-BOM

This inputs on two BNC connectors 1 PPS signals from the GPS and from the Maser. The input impedance is 50 Ohms. The card shifts the TTL levels to LVDS and provides wafer outputs which can then be routed to the OPS card. Power input is 3.3Volts.

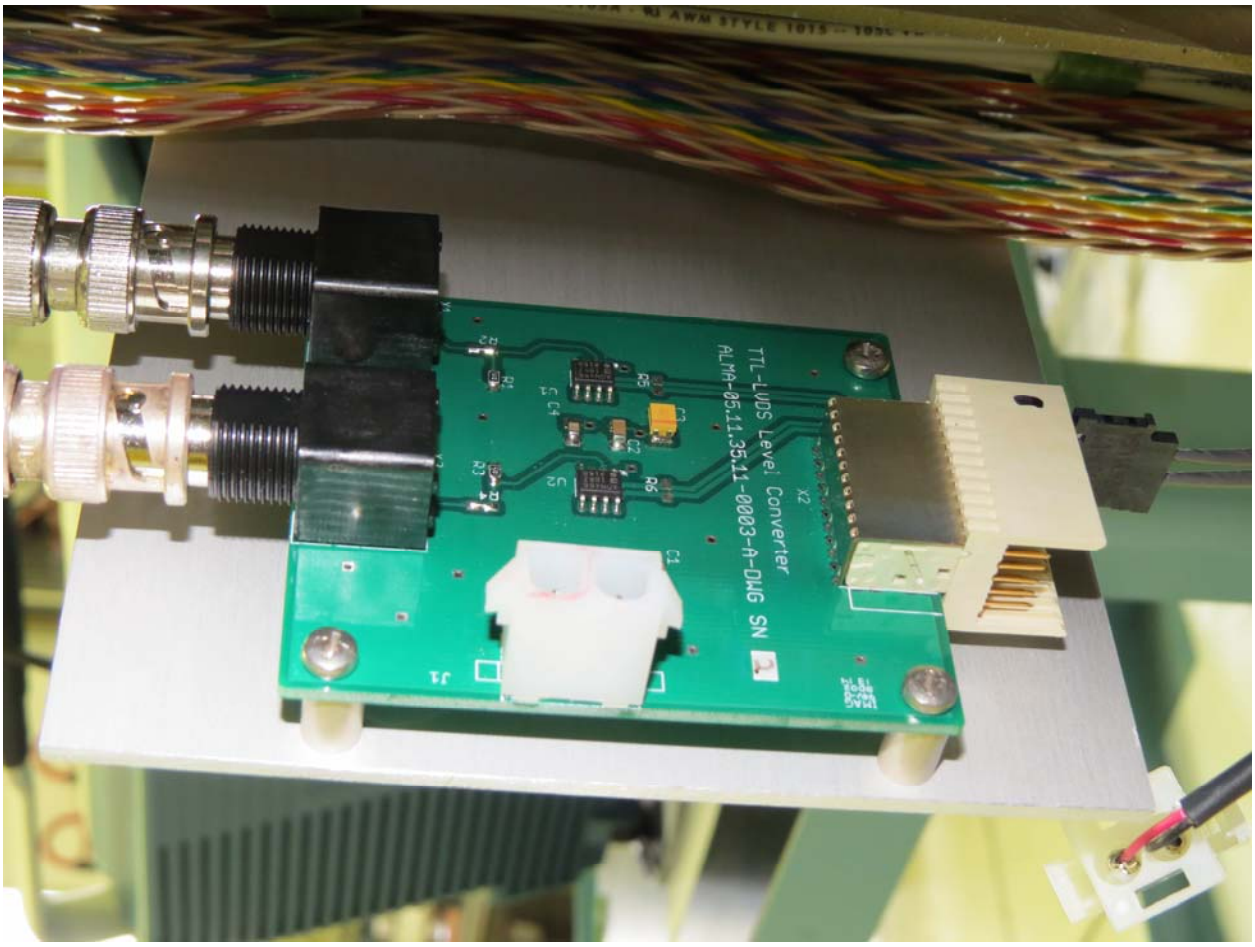


Figure 20 TTL Level Change Card mounted on plate

6.2 TLC Schematic

The below figure reproduces for convenience the simple schematic.

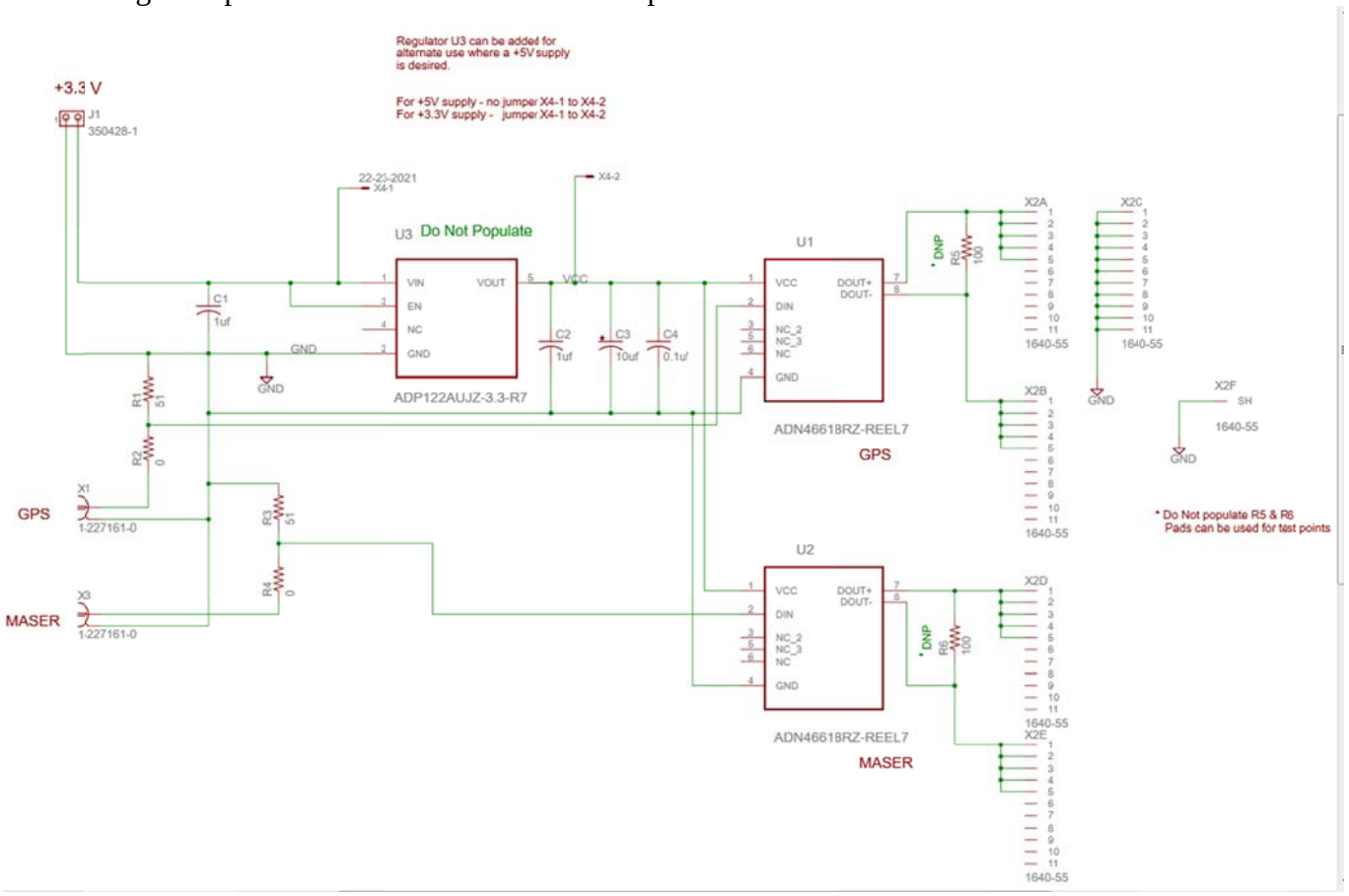


Figure 21 TLC Card Schematic

6.3 Changes to be implemented in building the TLC's

Note U3 the regulator is omitted, with Vout jumpered to Vin. Originally a 5Volt input was regulated down to 3.3 Volts. It was deemed simpler to input 3.3 Volts directly.

R5 and R6 are omitted since the termination resistor is in the LVDS receiver chip, so should not be here.