Atacama
Large
Millimeter
Array

ALMA Phasing Project
Phasing Interface Card Manual

ALMA-05.11.31.05-0001-A-MAN

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1 Description

1.1 Purpose

The purpose of this manual is to describe the Phasing Interface Card both from a higher level functional perspective as well as from a detailed circuit perspective. It also includes a summary of the available documentation for the card.

1.2 Scope

This document applies to the entire Phasing Interface Card Assembly, as described below.

2 Applicable Document, Reference Documents, Acronyms and Definitions

Applicable documents are necessary for the understanding of this document. In some cases, they provide additional requirements which are to be incorporated into the ICD. Reference documents are supplemental and simply provide further reference for various topics. In most cases, the acronyms used in this document are consistent with ALMA defined acronyms, however additional acronyms have also been listed which are outside the scope of ALMA definitions. No distinction is made between these two uses.

2.1 Applicable Documents

The following documents, of the exact issue shown, form part of this document. In the event of conflict between the documents listed here and this document, this document shall take precedence.

Number	Document Title	Document Number

Table 2-1. Applicable Documents for this ICD

2.2 Reference Documents

Number	Document Title	Document Number
[RD 01]		
[RD 02]	ROACH FPGA Requirements and Specifications	ALMA-05.11.31.15-0002-A-SPE
[RD 03]	PIC Assembly Block Diagram	ALMA-05.11.31.11-0001-A-DWG
[RD 04]	PIC Schematic	ALMA-05.11.31.11-0002-A-DWG
[RD 05]	PIC Assembly ZDOK to QXH Adapter Schematic	ALMA-05.11.31.11-0003-A-DWG
[RD 06]	PIC Assembly Misc Cables	ALMA-05.11.31.11-0004-A-DWG
[RD-07]	PIC Assembly Bill of Materials	ALMA-05.11.31.12-A-0001-BOM
[RD-08]	PIC Bill of Materials	ALMA-05.11.31.12-A-0002-BOM
[RD-09]	PIC Assembly ZDOK to QXH Adapter BOM and Assembly	ALMA-05.11.31.12-A-0003-BOM
[RD-10]	PIC PCB Files	ALMA-05.11.31.11-0003-A-DWG
[RD-11]	PIC Assembly ZDOK to QXH Adapter PCB Files	ALMA-05.11.31.11-0006-A-DWG
[RD-12]	APP_Project_Plan, latest version	-

Table 2-2. Reference Documents for this ICD

2.3 Abbreviations and Acronyms

AD	Applicable Document
ALMA	Atacama Large Millimeter Array radio telescope
AOS	Array Operations Site
APP	ALMA Phasing Project
ATX	Advanced Technology eXtended (standard for Personal Computers)
CAI	Correlator Antenna Input
CIC	Correlator Interface Card
GPS	Global Positioning Service
ICD	Interface Control Document
IPT	Integrated Product Team
LRU	Line Replaceable Unit
LVDS	Low Voltage Differential Signal
M&C	Monitor and Control
NRAO	National Radio Astronomy Observatory
PAI	Preliminary Acceptance In-House

PAS	Provisional Acceptance On-Site
PCB	Printed Circuit Board
PIC	Phasing Interface Card
PPS	Pulse Per Second
TE	Timing Event (a 48-msec timing tick which is the heartbeat of the ALMA control system)
UPS	Uninterruptable Power Supply
VDIF	VLBI Data Interchange Format
VEX	VLBI EXperiment
VLBI	Very Long Baseline Interferometry

2.4 Definitions

None so far…

3 Overview

Version A of this manual presents an overview of the design of the functionality of the PIC and of the documentation available for it. Future versions will present the circuit operation in more detail. A block diagram of the assembly is presented. This is followed by a short summary of the available documentation.

The Phasing Interface Card (PIC) historically has referred to the electronics module that fits into certain slots of the ALMA 64-Antenna Correlator and that serves the purposes described in **[rd 09]**. During the design process the NRAO-designed-card that serves as the "motherboard" for the PIC has also become known as the PIC. When it is necessary to distinguish between these two uses, a second acronym, PICA, has been adopted. PICA (PIC Assembly) always refers to the entire assembly consisting of the "motherboard", daughter cards, cables and hardware.

3.1 Block Diagram Description

The block diagram of the PICA is available as **[RD 03]**; it presents the board mostly from a mechanical and electrical point of view. A second block diagram is available in Figure 4.1 of **[RD-2].** It presents the board from a signal-flow, functional point of view. Both aspects of the board are presented in the following sections.

3.1.1 Mechanical and Electrical Description

As shown in **[RD 03]** the PICA consists of the following major components:

- PIC ("motherboard")
- ROACH2 Card
- SFP+ Mezzanine Card
- Two ZDOK Adaptor Boards
- Six cables (shown in blue)

The function of each of these is described in the following five sections. A photo of the assembled prototype is show in Figure 3-1 below.

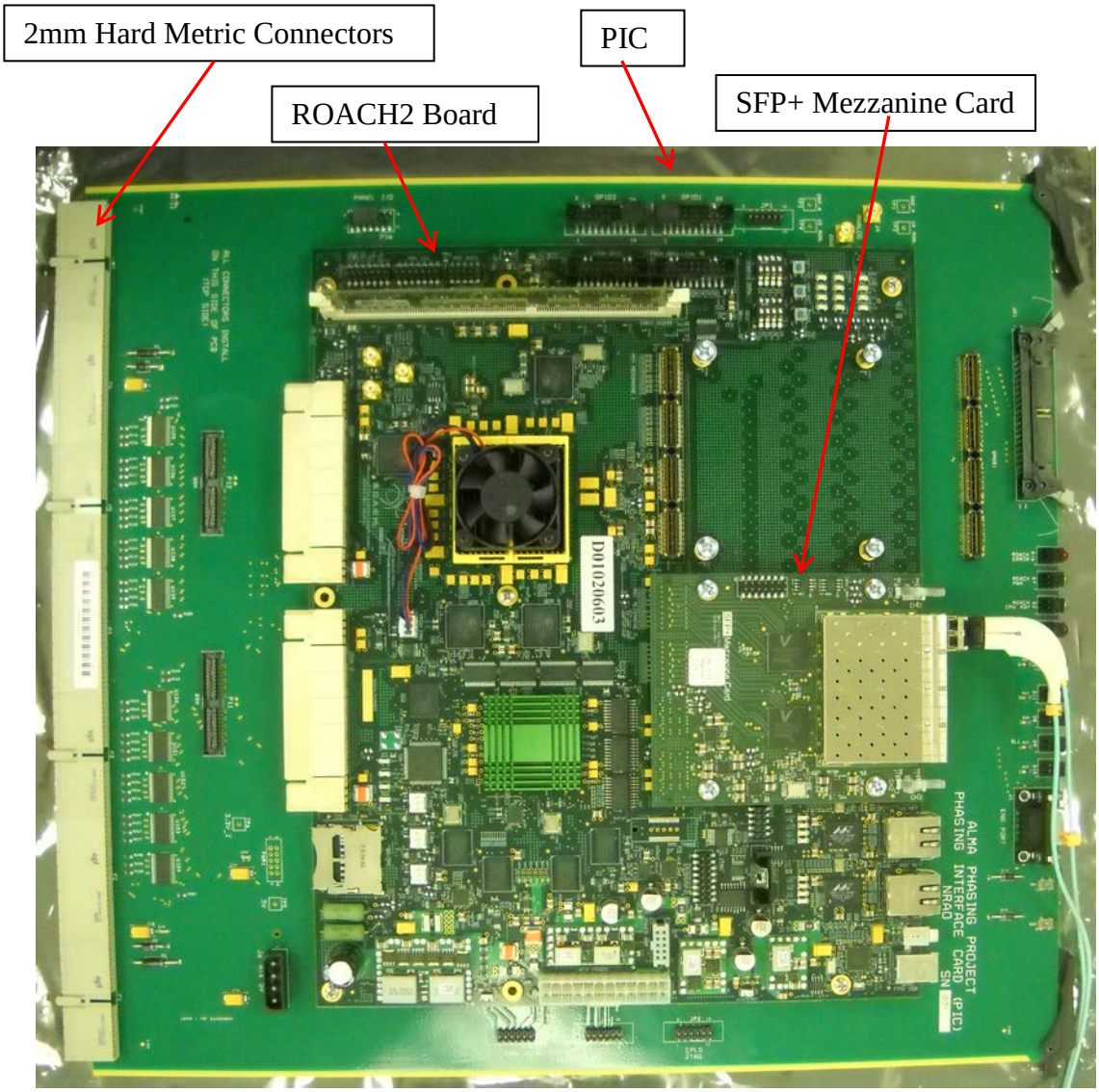

Figure 3-1. Phasing Interface Card Assembly (PICA). Electrical cables not installed.

3.1.1.1 Phasing Interface Card (PIC)

The PIC serves as a motherboard on which all the rest of the components are mounted. It also provides the interface to the Correlator Bin's backplane via the hard-metric 2mm connectors P1

through P7. Several connectors are provided for interface with the ROACH2 Card. P11 and P12 on the left-side of the drawing make the phased-sum signals available to the ROACH 2 card via ZDOK Adaptor Boards. P16, GPIO2 and GPIO1, along the top of the drawing, are provided for communication with the FPGA on the ROACH2 board. QMSS1, on the right side of the drawing is used to receive test signals from the ROACH2 board. Its outpus are buffered and connect to test points on the front edge of the card (not shown).

3.1.1.1 ROACH2 Board

This is a commercially available board designed for signal processing. It is widely used in the astronomical community. See the following link for a more detailed description.

https://casper.berkeley.edu/wiki/ROACH2

It has a large FPGA for signal processing and a PowerPC for interfacing to the FPGA. It also has provisions for two mezzanine cards. Design information for this board will be attached to the EDM entry for this manual. In the APP application, its primary function is to format the phased-sum data into VDIF frames for recording.

3.1.1.1 SFP+ Mezzanine Card

This is also a commercially available board. It interfaces to the ROACH2 and provides four ports for 10 GbE optical communications conformant with the SFP+ standard. In the APP application, one port is required to transmit the formatted, phased-sum data to the recorders via the Fiber Mux and Demux. The port must be populated with an SFP+ module to drive a fiber. This module is included in BOM **[RD 07]**. Design information for this board will be attached to the EDM entry for this manual.

3.1.1.2 ZDOK Adaptor Boards (ZDOK 1 and ZDOK 2)

These boards route the phased-sum signals from the PIC to the ROACH2. Electrically, they preserve the high-quality impedance control of the connectors on either end. Mechanically, they are constructed using “flex-board” and so limit mechanical stresses which would exist with a “hard” connection.

3.1.1.1 Miscellaneous Cables

The three cables along the top of the drawing provide a communications pathway between the PIC and ROACH2. The communications is directly between the microprocessor system on the PIC and the FPGA on the ROACH2.

The cable on the right side of the drawing is used for routing test signals from the ROACH2 FPGA to a test point connector on the PIC.

The cable between the PWR1 connector on the PIC (bottom right) and the P1 Power Out connector is used only for testing. It can provide power to the microprocessor on the PIC from the ROACH2.

A cable to an ATX supply is shown near the bottom middle of the drawing. The ROACH2 receives its power from this power supply. In turn the supply is connected to the correlators -48-volt bus. This provides the ability to shut the ROACH2 board down via the 167 microprocessor to save power. It also maintains the system safety feature of shutting down when the -48-volt bus is powered down due to anomalies detected by the Quadrant Control Card.

3.1.2 Signal Flow Description

The signals present on the PICA can be classified into four categories: data, timing, monitor and control, test. The paragraphs below present a functional overview of the PICA and describe the various signals present with reference to Figure 4.1 in **[RD 02]**. For convenience, this drawing is reproduced on the following page as Figure 3-2. Note that, in this figure, dotted lines are used to denote the PIC, ROACH2 and the FPGA on the ROACH2. The FPGA does most of the signal processing. Also for convenience, the signal names are highlighted in **bold** to make them easier to find in the text.

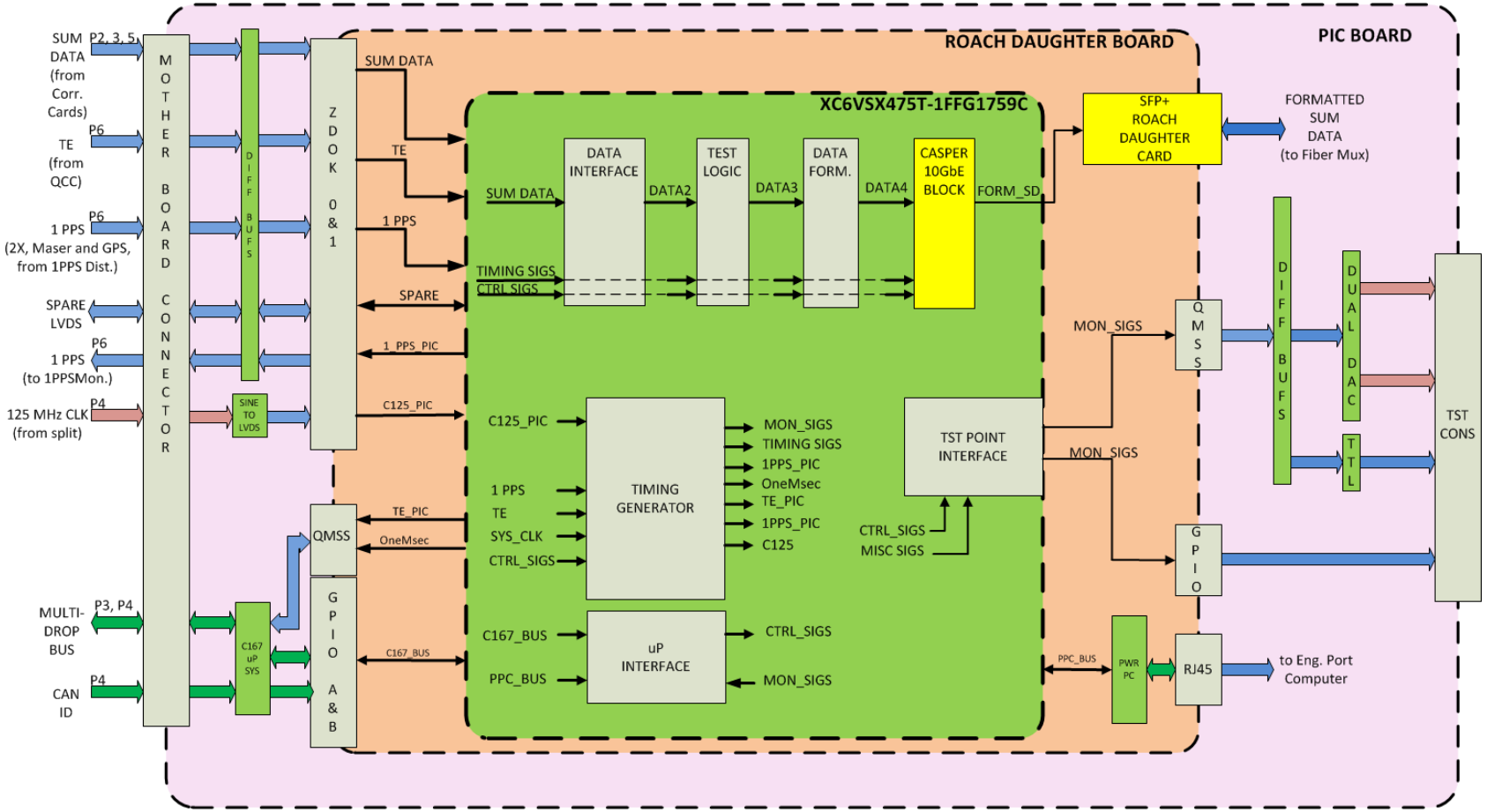

Figure 3-2. ROACH signal flow block diagram. Reproduction of Figure 4.1 from [RD 02].

3.1.2.1 Functional Overview

The main purpose of the PICA is to format the phased sum data into frames suitable for recording. The framing requirements are detailed in **[RD 02]**. It must also maintain the "look and feel" of other board of the correlator to simplify software development and mechanical constraints. These requirements are accomplished by providing the PIC "motherboard" and the ROACH2 board. The PIC includes the standard ALMA Correlator microprocessor and the standard connection to the Correlator Bin Motherboard. Thus, it is "just another card on the multi-drop bus", greatly simplifying monitor and control from both the Correlator Control Computer and the Engineering Port Computer. It also has the standard interfaces to the correlator timing signals "TE" and "125 MHz". The ROACH2 provides the signal processing power, in the form of a large FPGA, for formatting the data.

3.1.2.2 Data Signals

Two-bit samples from each of 32 sub-bands at a data rate of 125 Ms/s are routed from the Correlator Card sum port connectors on the correlator motherboards to the PIC motherboard connectors. These are labeled **SUM DATA** in Figure 3-2. These signals flow through differential buffers to protect the expensive FPGA from large external transients. They then flow through the ZDOK connector to the FPGA on the ROACH. They are captured on the FPGA and transformed from differential to single-ended signal in the Data Interface block. They then flow to the test logic. This logic has several capabilities. It can monitor the statistics of the incoming data (the number of occurrences of each of the four possible states for each sample stream), test the data against a known pseudo-random data pattern and generate various flavors of test data to substitute for the Sum Data in the downstream blocks. The Data Formatter combines the Sum Data with a header that provides time and station information. The CASPER 10 GbE Block further formats the data stream for 10 GbE transmission. The output of this block is routed to the SFP+ ROACH Daughter Card where it is converted to an optical signal for transmission to the recorders via the Fiber Mux/Demux sub-system.

3.1.2.3 Timing Signals

As originally designed, the 64-Antenna ALMA correlator uses the **TE** signal as its main time reference. (The TE signal is a pulse that occurs precisely at 48 msec intervals.) VLBI requires a 1-PPS signal for its timing purposes. The **TE** signal is exactly coincident with the **1-PPS** signal at seconds 0, 6, 12, … 54 of every minute. Rather than design a second precision time distribution system in the correlator for 1-PPS, the PIC uses TE pulse, along with a command

from the CCC, to generate an internal 1-PPS signal. The TE input signal is seen near the top left of Figure 3-2. It is routed through the motherboard connector, through a buffer, and through a ZDOK connector to the FPGA. In the FPGA it is the primary time reference to the Timing Generator which produces the time signals required for formatting the Sum Data.

Two **1-PPS** signals are routed from the backplane to the FPGA. One is derived from the Maser and the other from a GPS receiver. The FPGA compares these signals against its internally generated 1-PPS signal and provides time difference measurements which can be read over the CAN bus by the CCC. High level software can thus verify the timing of the PICA. A copy of the internally generated **1-PPS** is provided on the motherboard connector for monitoring purposes.

The clock for the correlator is a 125 MHz sine wave. It has the name **C125** on the block diagram. It is derived from the primary frequency reference for the site which, for VLBI, is the Hydrogen Maser. At the input connector, this signal is a sine wave. It is converted to single-ended and differential square waves on the PIC. One of the differential copies is used on the FPGA as the primary frequency source for time keeping. A higher frequency clock is used in the formatter to combine the sum data with the header.

The FPGA generates two timing signals which are transmitted to the C167 microprocessor. These are the **TE_PIC** and **OneMsec** signals, which are tied to microprocessor interrupt lines.

3.1.2.1 Monitor Signals

To preserve the look and feel of the correlator from the software point of view, the PICA is connected to the **Multi-Drop Bus** as shown in the bottom left corner of Figure 3-2. Like other boards in the correlator, the PIC gets is **CAN ID** from the DIP switches located on the correlator motherboard. This is also shown in the bottom left of Figure 3-2.

The C167 microprocessor on the PIC control a bus, labeled the **C167 Bus**, to communicate with the FPGA on the ROACH2. This bus has the same topology as other busses which communicate with other FPGAs in the correlator.

Another microprocessor, a PowerPC, on the ROACH2 board also communicates with the FPGA over a bus labeled **PPC_Bus** in the bottom-right part of Figure 3-2. This microprocessor is responsible for loading the FPGA personality at power up. It also provides a “back door” into the FPGA for debugging purposes, both during development and operations.

3.1.2.1 Test Signals

Several monitor signals are driven from the **TST POINT INTERFACE** located in the middle-right of Figure 3-2. These signals are buffered and routed to the test connector in the middle-right part of Figure 3-2. Two groups of signals drive Digital to Analog Converters and can provide 4-bit analog representations of whatever bits are selected in the FPGA. This feature may be useful in future upgrades by providing an analog representation of sum data.

3.1 Available Documentation

The Reference Documents Table, Table 2-2, on page 6 lists the documentation available for the PICA in the time frame of the CDR. This paragraph provides a short description of the relevant documentation. A block diagram and BOM for the PIC Assembly are available (**[RD 03]** and **[RD 07]** respectively**).** Schematics, BOMs and PCB files are available for the PIC and the ZDOK to QXH adapters (**[RD 04], [RD 05], [RD 08], [RD 09], [RD 10], [RD 11]**). A requirements and specifications document for the FPGA personality is available **[RD 02]** and has been instrumental in enabling development by individuals at three institutions. A schematic that includes electrical and assembly information for the miscellaneous cables is available **[RD 06].** Eventually, **[RD 01]** will become the PIC Assembly Requirements and Specifications.