Atacama Large Millimeter / submillimeter Array

Interface Control Document Between ALMA Phasing Project And ALMA Correlator

ALMA-05.11.10.00-60.00.00.00-A-ICD

2014-10-08

Prepared By:	**Organization Role:**	**Date and Signature:**
R. Lacasse	NRAO	
Approved By:	**Organization Role:**	**Date and Signature:**
Richard Lacasse	APP SE/Lead Engineer	
Nick Whyborn	ALMA Array Lead Engineer	
Alejandro Saez	IET Correlator Group	
Released By:	**Organization Role:**	**Date and Signature:**
Michael Hecht	APP Project Manager	

Change Record

Version	Date	Affected Section(s)	Author	Reason/Initiation/Remarks
A.1	2013-04-01	ALL	None	First Issue
A.2	2013-04-03	ALL	None	Incorporate comments from Saez
A.3	2013-04-22	Doc #	None	Correct doc. Number error on title page and header.
A.4	2013-08-09	Doc #	None	Update document number to latest format
A.5	2014-09-10	Doc.	Alex Caceres	Regular ICD number has been assigned.
A.6	2014-09-29		F. Sepulveda	Signature matrix updated according to N. Whyborn's comments
A	2014-10-08	Several	R. Lacasse	Updated [AD04] Updated 1-PPS distribution scheme

Table of Contents

List of Figures

1 Description

1.1 Purpose

This ICD covers the interfaces between the ALMA Phasing Project and ALMA 64-Antenna Correlator.

1.2 Scope

The ALMA Phasing Project provides ALMA with the capability of phasing and summing up to 63 Antennas and recording the resulting data for later correlation at another facility (e.g., Haystack Observatory). Equipment associated with the project includes a hydrogen maser for VLBI phase stability, various upgrades to the 64-Antenna Correlator (hardware, firmware and FPGA personalities), an optical data transmission system to transmit data over a single fiber from the AOS to OSF and a data recording system. This equipment is more fully described in **[AD01].** Some of these subsystems may have several interfaces to the ALMA Observatory (e.g. site and computing). This document covers only the interfaces with Correlator.

2 Applicable Document, Reference Documents, Acronyms and Definitions

Applicable documents are necessary for the understanding of this document. In some cases, they provide additional requirements which are to be incorporated into the ICD. Reference documents are supplemental and simply provide further reference for various topics. In most cases, the acronyms used in this document are consistent with ALMA defined acronyms, however additional acronyms have also been listed which are outside the scope of ALMA definitions. No distinction is made between these two uses.

2.1 Applicable Documents

The following documents, of the exact issue shown, form part of this document. In the event of conflict between the documents listed here and this document, this document shall take precedence.

Ref.	Document Title	Reference
[AD01]	APP Project Plan *Release 1.1 11-Oct-12*	ALMA Phasing Project, Project Plan 1.1, 11-Oct-12
[AD02]	ALMA Environmental Specification	ALMA-80.05.02.00-001-B-SPE
[AD03]	Seismic Design Specifications for ALMA-AOS and ALMA-OSF	SYSE-80.10.00.00-002-B-REP
[AD04]	APP Correlator Cabling	PIC_Sequence_Nrs_short.xls and NRAO_APP_Misc_Cables available on Deki

2.2 Reference Documents

Ref.	Document Title	Reference
[RD01]	AOS Technical Building Completion Package Construction Specifications	SITE-20.01.02.03-027-A-SPE
[RD02]	Interface Control Document Between 64-Antenna Correlator And Correlator Computing System	ALMA-60.00.00.00-70.40.00.00-E-ICD
[RD03]	64 Antenna Correlator Specifications and Requirements	ALMA-60.00.00.00-001-C-SPE
[RD04]	General Safety Design Specification	ALMA-10.08.00.00-003-B-SPE
[RD05]	Product Assurance Requirements	ALMA-80.11.00.00-001-B-GEN
[RD06]	Interface Control Document Between ALMA Phasing Project and Site	ALMA-.05.11.10.49-20.00.00.49-A-ICD
[RD07]	ALMA 64-Antenna Correlator Four Quadrants PAS acceptance tests report	CORL-60.00.00.00-0127-A-REP

2.3 Abbreviations and Acronyms

All acronyms and abbreviations used within this document are given at the ALMA Acronym Finder web page.

3 Interfaces to the 64-Antenna Correlator

The specification for the 64-Antenna Correlator **[RD03]** includes a requirement that the correlator provide “hooks” for VLBI. Mechanically, these include certain connectors, spare card slots and extra space in internal cable trays. Electrically, these include excess capacity of the power supply system. Also there is sufficient excess cooling capacity to handle the power dissipated by the APP electronics **[RD07]**. To take advantage of these hooks, various modifications to the correlator are required. These are detailed in the following sections.

3.1 Mechanical

Table 1 provides a summary of the components that will be added to the correlator. The following paragraphs provide additional detail on each component.

Component	Num.	Locations
PICA	8	All quads, Corr. Racks 2 and 3, Bin 4, FA slot
LVDS cables	256	All quads from correlator cards to PICs
LVDS cables	256	All quads from correlator cards to CICs
Multi-drop cables	8	Correlator backplane, near PICs
Maser 1-PPS copies	8 twinax, 8 LVDS	From 1 PPS Distributor to PIC backplane connector
GPS 1-PPS copies	8 twinax, 8 LVDS	From 1 PPS Distributor to PIC backplane connector
PIC 1-PPS	8 twinax, 8 LVDS	From PIC backplane connector to 1 PPS Distributor
PIC Comm. Ethernet	8	From PIC to Engineering Port Computer Ethernet switch
PIC Comm Ethernet switch	1	To consolidate Ethernet signals from the PICs for the Engineering Port
PIC Comm Ethernet Card	1	To provide a second Ethernet port on the Engineering Port computer for ROACH-2 troubleshoting.
ATX Power supply assembly	8	In rear of the correlator racks, near the locations of the PICs
Bin cable guide assembly	8	In correlator bins containing PICs.

Table 1: Summary of components added to the correlator

3.1.1 Phasing Interface Card Assemblies (PICAs)

The PICAs are card assemblies designed to fit into spare slots in the correlator bins. They consist of a PIC with a ROACH-2 board as a daughter card. In turn the ROACH-2 board has a SFP+ daughter card to allow it to communicate using 10 Giga-bit Ethernet. Several cables inter-connect the PIC and ROACH-2. Two PICAs are required per quadrant. They shall be located in the "Final Adder Slots" of Correlator Racks 2 and 3, Bin 4 in each quadrant. The slots chosen are near the bottom of the racks for best cooling and near the physical middle to minimize cable lengths. Also, the cards located directly above these slots are relatively low power, so no cooling issues are foreseen. Of course, the temperatures in the rack will be measured as part of system testing. See Figure 1.

Figure 1: Photo of one correlator quadrant showing the selected locations for the PICs

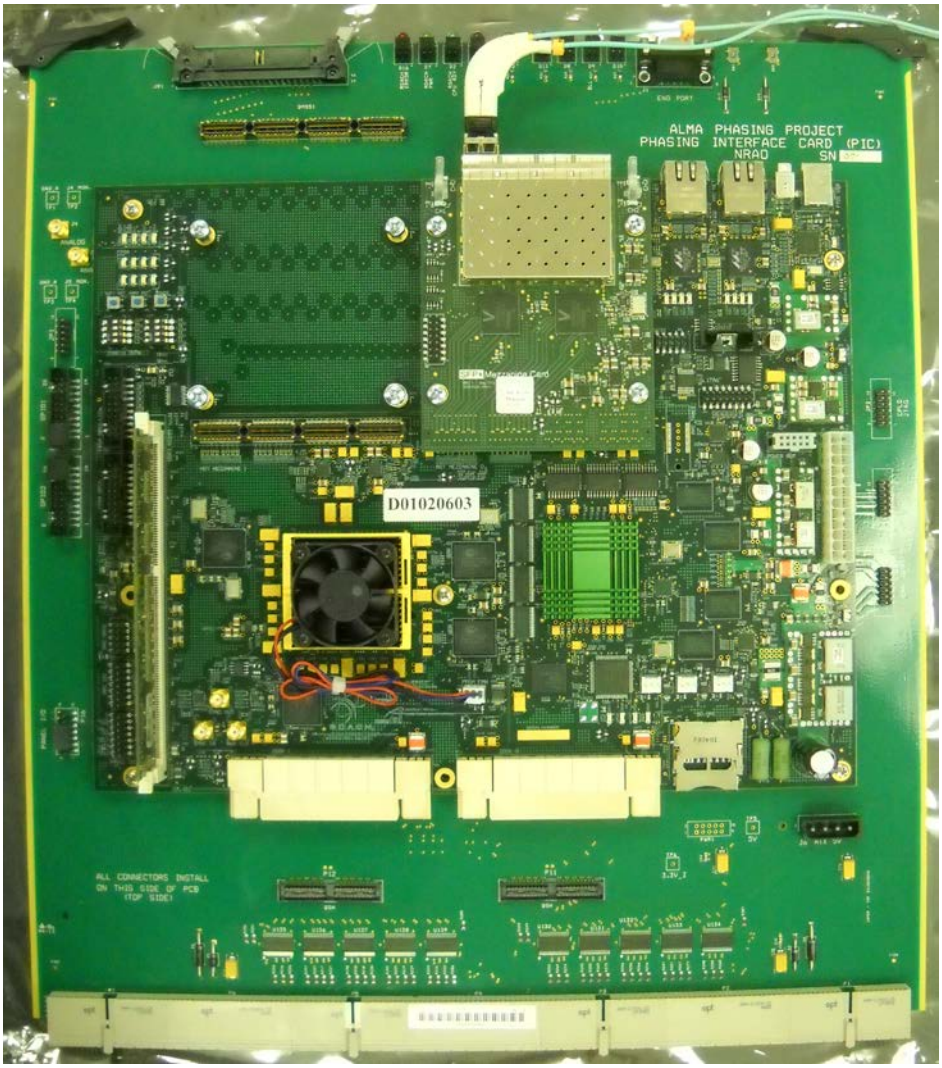

Figure 2: Photo of the Phasing Interface Card Assembly, including the PIC, the ROACH-2, the SFP+ Card and 10GbE cable

3.1.2 LVDS Cables from Correlator Cards to PICs

The sum of the selected antennas is computed in the correlator cards. The sum signals are made available on the Correlator Bin backplane on 2-mm "LVDS" connectors. These signals must be routed to the motherboard connectors associated with the PICs. The cables to be used for this purpose are "LVDS" cables similar to those which interconnect the Station Interface and Correlator Interface Cards. In this case, however, they are "1-row" cables and not "2-row" cables like those used to interconnect the Station and Correlator bins. There are a total of 64 such cables per quadrant and so a total of 256 (32 planes x 2 polarizations x 4 quadrants) for the entire correlator. They shall be routed using existing cable trays in the correlator. A "from – to" list for these cables is provided in **[AD04].**

3.1.3 LVDS Cables from Correlator Cards to CICs

The system is designed such that the sum of the antennas can be fed back into the correlator matrix as if it were antenna input 63. The feedback path is from the correlator sum connectors to the input connector of some CICs. Again "LVDS" cables are used for this purpose and a "from-to" list is included in **[AD04].** A total of 256 cables are required.

3.1.4 Multi-drop Bus Cables

Like many cards in the correlator, the PICs and 1-PPS Distributor must communicate with the CCC and Engineering Port via the multi-drop bus. This cable is a 26-conductor ribbon cable that includes CAN communications, Engineering Port communications and the Reset and Boot signals. One additional ribbon cable per PIC must be added to splice the PIC into the multi-drop bus. Similarly, one cable the the 1-PPS distributor (only on quadrant 2) must be added. This will extend the length of the bus by 0.5 to 0.75 meters, which should be of no consequence. The operation of bus will, of course, be verified similarly to the procedure in **[RD07].** The required cabling change is detailed in **[AD04].**

3.1.5 Maser 1-PPS copies

Each PIC shall receive a copy of a maser 1-PPS timing reference. This will allow it to compare an internally generated 1-PPS signal with the maser-generated reference. The difference between the two shall be available to Computing via a CAN command. One of the twisted pairs in a 2-wafer LVDS cable will be used for the Maser 1-PPS.

3.1.6 GPS 1-PPS copies

Each PIC shall receive a copy of a GPS 1-PPS timing reference. This will allow it to compare an internally generated 1-PPS signal with the GPS-generated reference. One of the twisted pairs in a 2-wafer LVDS cable will be used for the GPS 1-PPS.

3.1.7 PIC 1-PPS

Each PIC shall provide a copy of its internally-generated 1-PPS signal on its backplane connector. This signal shall be routed to the 1-PPS Distributor to allow comparison with other 1-PPS signals via a portable oscilloscope or optional counter (per **[RD06]** located in the communications rack. One of the twisted pairs in a 2-wafer LVDS cable will be used for the GPS 1-PPS.

3.1.8 PIC Comm. Ethernet

The ROACH-2 boards on the PICAs have available an Ethernet port for trouble-shooting purposes. A CAT-5 cable shall be routed from this port, to the rear of the correlator rack and on to the PIC Comm Ethernet Switch described below.

3.1.9 PIC Comm. Ethernet Switch

The ROACH-2 boards on the PICAs have available an Ethernet port for trouble-shooting purposes. CAT-5 cables shall be routed from this port on each PIC to an Ethernet switch which will consolidate them for the Engineering Port Computer. The switch will be mounted in the rack containing the Engineering Port computer. A 16-port switch will be provided by the APP. If ALMA has preferences on makes or models of switches, they must make this known to the APP before the switch is purchased. Initially, the PICs will be connected directly to the site Ethernet network rather than to the Engineering Port since this is more convenient for testing and development. ALMA will decide if or when to connect the PICs to the Engineering Port.

3.1.10 PIC Comm. Ethernet Card

The ROACH-2 boards on the PICAs have available an Ethernet port for trouble-shooting purposes. CAT-5 cables shall be routed from this port on each PIC to an Ethernet switch which will consolidate them for the Engineering Port. An Ethernet Network Interface Card will be provided by the APP for installation in the Engineering Port Computer to allow communication with the

Ethernet ports on the ROACH-2. If ALMA has preferences on makes or models of boards, they must make this known to the APP before the board is purchased.

The network between this card and the PICs will be a private network. To facilitate this, the IT staff shall

1. Configure the Engineering Port so that it cannot act as a "gateway" between the ALMA network and the PIC private network;
2. Enable DHCP and DNS service in order to always have the same IP and name for every PIC card.

ALMA will decide if or when to connect the PICs to the Engineering Port.

3.1.11 ATX Power Supply Assembly

The ROACH-2 cards are designed to be used with ATX power supplies. These are similar to those commonly used in PCs. One ATX supply per PIC will be mounted in the rear of the correlator rack. It will draw -48-volt power from an existing unused connector in the correlator backplane (PWR2) and provide it to the ROACH-2 board via a cable routed from one side to the other of the motherboard, via an existing hole. The Phasing Project will supply the adapter plate, mounting hardware, power supply and cables. The assembly will also include the adaptor mentioned in 3.1.5 and a bend-radius limiter for the fiber from the PIC to the Fiber Mux module.

3.1.12 Bin Cable-Guide Assembly

There is an optical fiber connecting each PIC with the Fiber Mux. Care must be taken to limit the bend radius of this cable to avoid optical power loss. An assembly which includes a bend radius limiter and other cable supports shall be provided for each PIC. This shall be installed in the bins, near the PICs using existing mounting holes.

3.1.13 Other Interfaces

For the sake of completeness, it should be mentioned that a minor mechanical modification to the bins containing the PICs is under discussion. In the event that the cooling to the PICs is marginal, it may be desirable to cut away some material designed to support a card which will never be used in the bins. (It is mechanically impossible to house both the PIC and a card in the adjacent spare slot.) This would provide better airflow. It should be emphasized that this is simply an option at this point and won't be exercised unless all parties are comfortable with it. The main consideration is not structural but electrical; it would be necessary to remove the material without creating any metal debris.

3.2 Thermal and Electrical Interfaces

The APP equipment will result in a negligible load to the correlator. The total load of all installed equipment will be about 2000 watts (out of about 140,000 watts in the existing system).

3.3 Firmware and FPGA Personalities

The APP requires some modifications to firmware and FPGA personalities. In particular:

- The Correlator Card Sum FPGA personalities (a total of three different personalities) will be modified to provide an adder tree that is suitable for APP purposes. Note that the existing adder tree logic was originally designed to be used for phasing ALMA. Since the APP is the first instance of phasing ALMA, the there is no impact to the correlator functionality.

- The Correlator Interface Card FPGA personality will be modified to provide a feedback path, via antenna input 63, for correlating the sum against other antennas. The modification will effectively be a single-pole-double-throw switch which will allow for the current correlator configuration as well as the new capability.
- Firmware in the SCC and LTA (just the C167 application code) will be modified to support the protocols listed in **[RD02]**. These are additional capabilities which should have no impact on existing capabilities.
- A new FPGA personality and firmware will be associated with the PICA.
- A new FPGA personality and firmware will be associated with the 1-PPS Distributor.

All firmware and FPGA personalities will be documented in the same repository as existing correlator firmware and FPGA personalities.

3.4 Installation Assistance

The APP feels strongly that the Correlator Group in Chile would gain a large training benefit from installing the APP equipment in the correlator room. The APP also acknowledges that a more-professional-looking installation will result from the assistance of the Correlator Group. Therefore the APP respectfully requests assistance from the Correlator Group in installing all APP equipment associated with the correlator in cooperation with the design team.

Members of the APP met with ALMA Staff in January of 2013. One of the outcomes of the meetings was a decision to install equipment incrementally as it becomes available. This has two benefits. First, if operational problems result from an installation, it will be much simpler to isolate the responsible components. Second, much of the installation can be done during test and engineering time saving the valuable telescope time which would be used during a major installation effort. Therefore, the APP plans to work cooperatively with the Correlator Group, providing equipment for installation as it becomes available along with detailed installation instructions.