Digital Base-Band Converter
– a multi-purpose digital backend –

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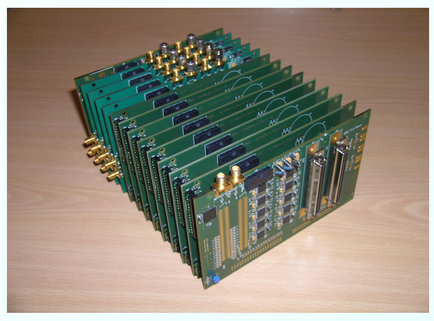
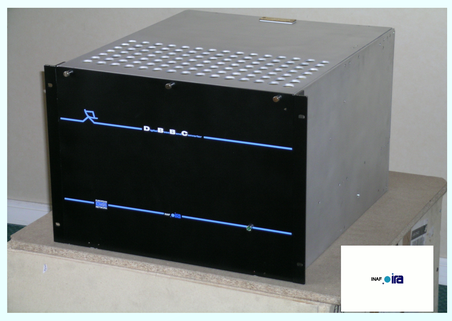
Collaborators: *G. Tuccari, S. Buttaccio, G. Nicotra (INAF, Noto) Y. Xiang (SHAO-CAS, Shanghai)*

What it Looks Like



Heart of the DBBC



DBBC complete

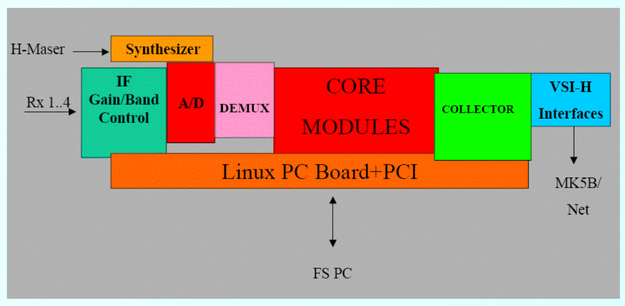
Analogue Mark IV terminal
> 25 years old

- DBBC developed by EVN (Noto, MPIfR, Shanghai)
- Fully backwards compatible with Mark IV terminal
- Replaces Mark IV terminal completely
- Cost of DBBC + Mark5B recorder << 100 kEUR

- DBBC version 1 developed July 2005
- DBBC version 2 with more processing power (Virtex 5) under development 2007/8

DBBC + recorder (eg Mark 5B) = complete VLBI data cquisition system << 100 kEUR

How it Works

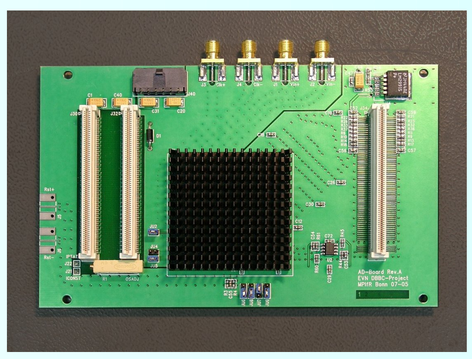


- A/D samples an input IF bandwidth of 512 MHz, in range 0 GHz to 2.2 GHz, 10 bit samples, one A/D card can sample one IF. Core module carries an FPGA processor

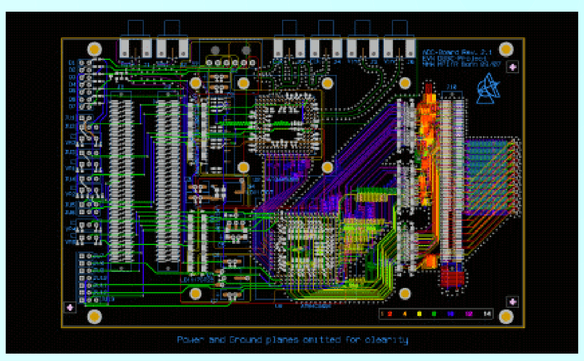
- Data flows to FPGA core modules for gain control, filtering (0.25 MHz to 16 MHz bandwidth selectable) and single-sideband digital downconversion (one FPGA core board = 4 analogue BBCs)
- Output board gives optionally data on VSI to recorder or 10 GE on fibre
- Stackability -> extensible
  Stack up to four A/D boards, depending on the number of IF inputs needed
  Stack up to sixteen FPGA core boards as more processing power is needed
  Plus some auxilliary components
- Flexibility! With FPGA code updates DBBC becomes:
  - a spectrometer (under development at Arcetri)
  - a pulsar search engine (under development at Arcetri)
  - a digital receiver (under development at MPIfR)
  - a converter linear to circular pol'n (under development at MPIfR)
  - a polarimeter (under development at MPIfR)

MPIfR Contribution

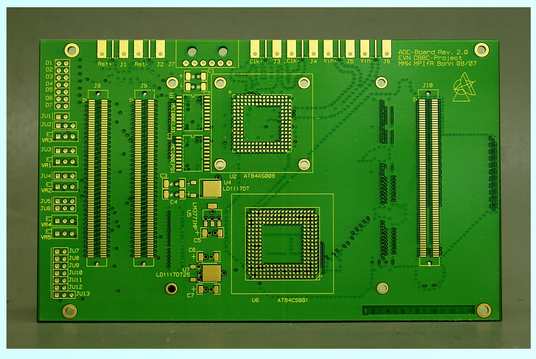
- A/D board design & assembly
- FPGA Core board assembly
- Board layout and firmware for input and output over 10 GE
- Firmware for use as a digital receiver
- Firmware for polarimeter & polarization conversion



ADBoard1 showing one differential analogue IF input and one differential clock input on SMA connectors at top and connectors (HSI) to the FPGA cards



Schematic of 14 layer ADBoard2



Top view of the unpopulated ADBoard2

Board Specifications:

Board	Date	Input BW	Sample Rate	bits / sample	De-mux	Layers	Internal structures	External structures
DBBC1: ADB v1	Jul 2005	2.2 GHz	1.5 GHz	8	2 selectable on-chip	8 layer	100 um	200 um
Core v1	Jul 2005	Virtex II						
DBBC2: ADB v2	Oct 2007	3.3 GHz	2.2 GHz	10	2 or 4 selectable on-board	14 layer	80 um	100 um
Core v2	Oct 2007	Virtex 5						

- Boards are impedance and delay controlled.
- Due to fine structures and lead-free technology, boards are manufactured and populated by an external contractor
- **Open design** for flexibility to adapt to new applications, eg digital receivers
- Daughter boards can be added for several purposes
- All the signals on the board are available for future extensions.

Production Timeline

2005 mid	Project begin
2006 early	DBBC1 prototype running
2007 Nov	Delivery of first DBBC1, to Wettzell
2007 Dec	Testing of DBBC1's for Irbene and Arcetri
2008 Jan	ADBoard2 prototypes ready for testing
2008 Mar	FiLa-10G board prototype ready for testing

Project Web Page

http://www.noto.ira.inaf.it/dbbc/index.htm

Future

FiLa-10G board:
- Optical link (10 Gbps ethernet) to separate the noisy FPGA processing units far from the front ends and samplers.
- Three-way interface: DBBC internal bus (HSI) <-> 2 x VLBI standard Interface (VSI) <-> 10GE optical network.
- Can be placed at beginning or end of chain of boards
- Hardware specifications have been defined
- Optical link tests have been done
- First results by early 2008

Applications:
- FiLa-10G card connected to A/D card version 2 gives transmission of pure sampled data on optical fibre
- FiLa-10G card connected to FPGA card gives transmission of processed output data
- Use as stand-alone converter between VSI and 10G ethernet

Firmware:
- spectrometer / pulsar search engine / digital receiver /converter linear to circular pol'n / polarimeter