DBBC – MK4/VLBA-like Backend Implementation
Status Report for CDR 2007

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Content

1. System Overview

An overview of the DBBC system in the MK4/VLBA-like backend implementation is shown in fig. 1. In a standard rack 19 " rack is inserted the number of element necessary for realizing the functionality of a MK4 backend system, with output for VSI compliant recorders. The same case is able to accommodate the update version of the ADB and Core boards, together with FiLa10G boards. One of such boards is able to establish a connection for data communication with 2x10Gbps data rate. Any FiLa10G board can be accommodated as piggyback element on a ADB2 board, and one can be connected on the output of the processed data.

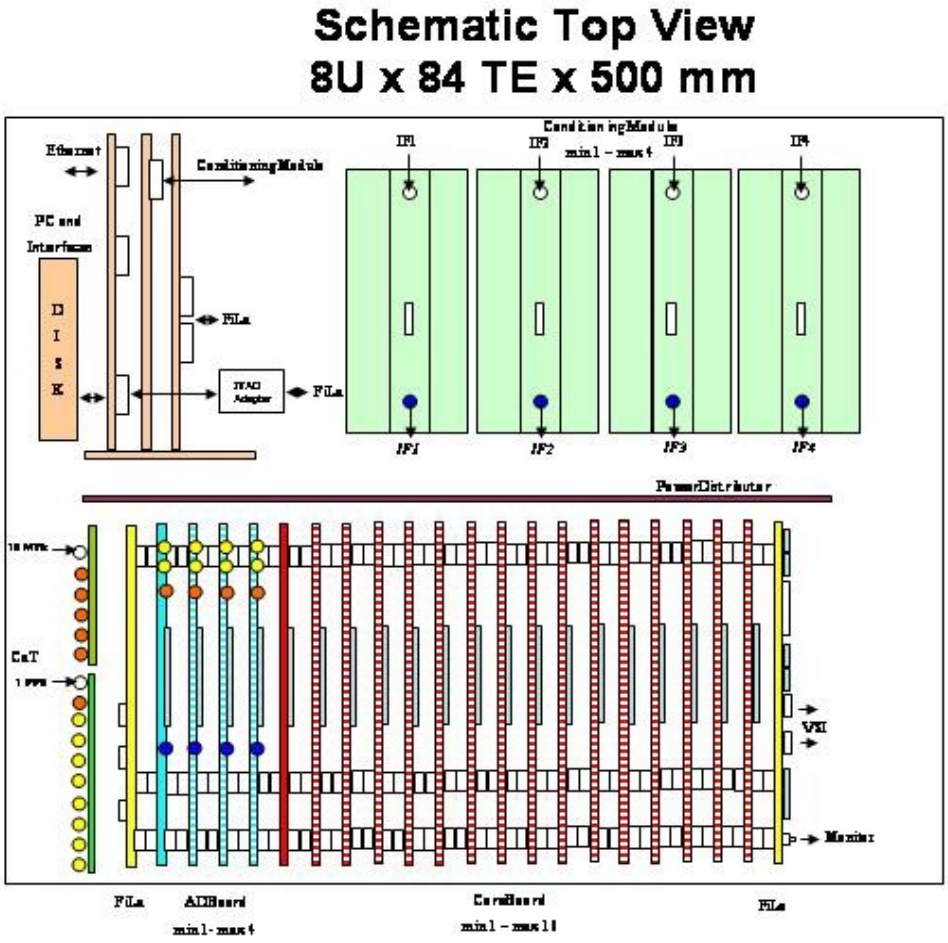


Fig. 1 DBBC System Overview

The logical data flow starts with the Conditioning Modules (green blocks) where RF/IF is inserted. Such modules are used for define the pre-sampling Nyquist zone and adjust the signal levels in order to fit the ADBoard requirements. A connection with the PCSet is dedicated to evaluate the total power and to set the appropriate total gain.

Signals out fro the four Conditioning Modules are sent to the AD Boards for their sampling. Such ADBoards receive also the general sampling clock, generated by the CaT Clock board and the alignement reset from the CaT Timing board.

The CaT Clock board is indeed involved in generating the sampling clock frequency (variable between different values) from a 10 MHz input signal coming fro the H-Maser, while the CaT Timing board is producing the proper timing signals necessary for synchronize the ADBoards.

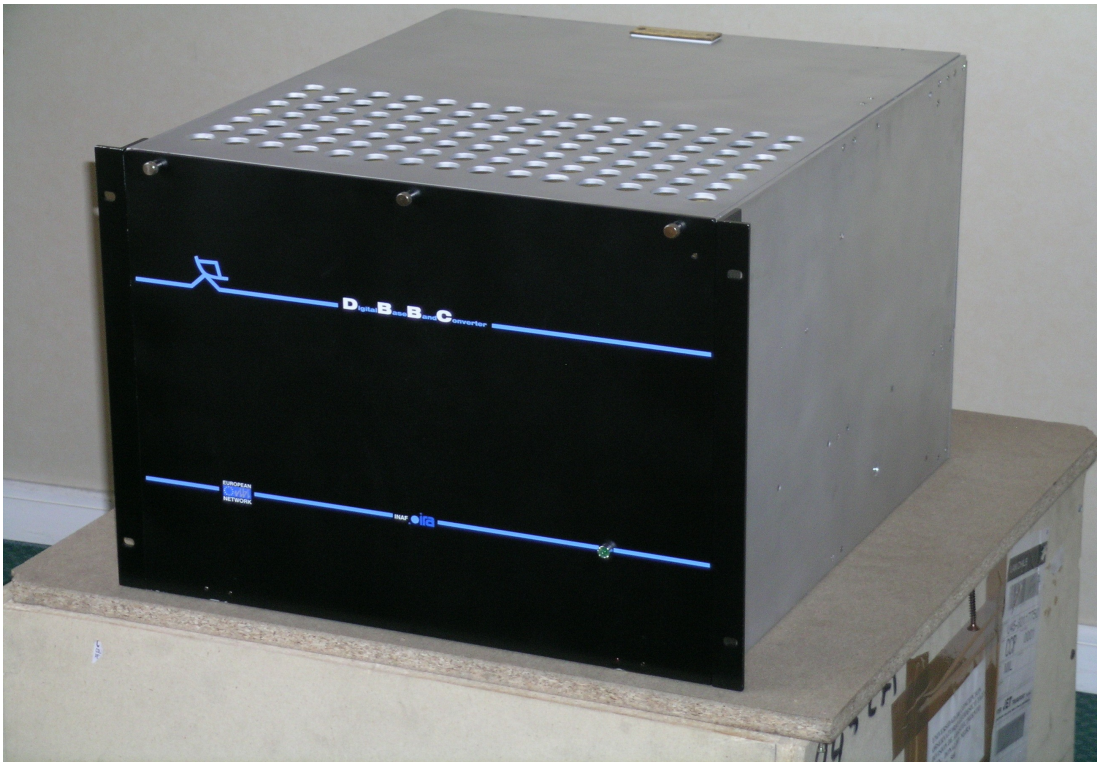
Sampled data from the four AD Boards is propagated to the Core Boards, that can be present in the version 1 in a number between 1 and 16. Any of the Core boards is able to process any of the four sampled RF/IF and then can produce a down-conversion at an arbitrary tuning point. Processed output data is available on the common output bus, along the Core chain to rCduce the entire channelised output data set.

CoreBoards can be accessed through three entering points, one necessary for accessing the JTAG configuration programming chain, an other for have access to the registers functionalities of each board, a third for the timing feeding. Such needs are satisfied by the FiLa board placed at the beginning of the chain. A second of such FiLa boards is placed at the end of the chain to collect the output data bus and form the what is necessary for feeding two VSI connectors. Additional functionalities are yet accomplished with the FiLa boards.

A Power Distributor system is able to furnish the supply voltages with appropriate currents to the entire sent of boards. Any Core board has a separate low voltage generator and an accurate separation between all the power rails is assured in order to keep under an optimal control the noise superimposed to the power distribution.

The PCSet is composed by a compact PC baord on a PCI backplane, that in addition with two PCI commercial boards, an HD and a JTAG USB programmer complete the elements necessary for the full DBBC functionality.

In a very schematic representation the DBBC in this MK4/VLBA-like back-end configuration can be seen as a box where input is: 10MHz, 1PPS, 4xIFs; output is: 2xVSI connectors. The DBBC can also be a very different system, within the same hardware or with a subset of the hardware described.



A DBBC system

2. Conditioning Module

Signals coming from a receiver need to be adapted before to enter the ADBoard for several reasons: amplitude limitation and optimization, frequency limitation, equalization.

The AD device is able to convert signals in a well defined range, so having signals with higher values with respect to the maximum that can be represented is then going to introduce errors and additional noise contribution. On the other hand it would be worth to have the input signal at an amplitude that can take advantage by the 8-bit possible representation. So possibly the noise amplitude distribution coming from the receiver needs to be amplified or attenuated in order to meet both requirements: to have the maximum components in the amplitude less than the maximum allowed level, and to be enough wide to be represented. In other terms the signal levels needs to be optimised with respect to the AD noise figure and its compression point.

To do the job is then necessary to dispose of a certain redundancy of amplification and attenuation, considering the levels ordinary available by a receiver as today adapted to the MK4/VLBA terminal. A +-16dB is available for such purposes in the Conditioning Module. The total power level is measured in order to dynamically adjust at the optimal level of the signal to be sent at the AD converter. A loop between the variable gain and the total power measurement is closed with the PCI 9111 control board and software, in charge for all the Conditioning Modules settings and reading.

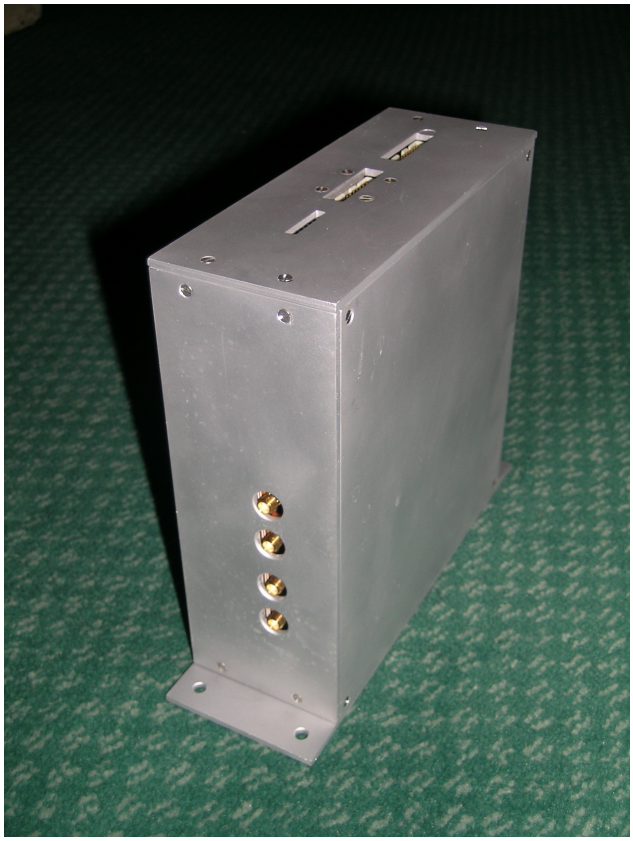
The ADBoard1is able to sample in a range up to nominally 2.2 GHz with a sample rate we choose as 1.024 GHz. So different 512 MHz Nyquist zones can be used in the full range. The proper selection of such ranges requires the insertion of pre-sampling filters able to select the portion to select before sampling without ambiguities. The conditioning Module includes four filters in the range: 10-512, 512-1024, 1024-1536, 1536-2048 MHz. The range from 2.048 up to 2.560 MHz can be used with an additional filter not included. Such range can be of particular interest because includes the observed S band that could be directly processed without the IF generation in the receiver.
The filter selection is realized through software.

The equalization functionality should be necessary for producing a flat image of the input RF/IF pre-sampling. Indeed receivers are not normally presenting a flat band, inside few dB, but shows large slopes. While this can be compensated in a narrow band channel system, it represents a severe limitation for wide band channels. So the equalization filters can be seen as irregular pass-band filter to compensate the slopes in the receivers band.

The band definition filters used for Nyquist zone selection have been developed with tuneable elements in order to accommodate a possible equalization factor. Of course this is appropriate with a defined receiver or similar band slopes for more receivers. Adopting different receivers with totally different slopes could suggest to produce such equalization externally to the DBBC system.

Additional elements included in a Conditioning Module, still selectable by software, is the choice between 4 different inputs.

A total power measure is available in the full range with the help of two different devices. The reading is realized with 16-bit precision.



A ConditioningModule

3. ADBoard1

The sampler board has the std shape selected for the DBBC system, with 3 couples of connectors forming three bus: HSI, HSO, CCM. The first is used to feed and distribute the sampled data, the second to propagate and feed the processed data, the third as general communication, configuration and monitoring bus.

The rear and front side connectors in the board receive and send, so that the three bus are integrated in the connector-tracks-device-tracks-connector set. This scheme is general and adopted in any board of the DBBC chain.

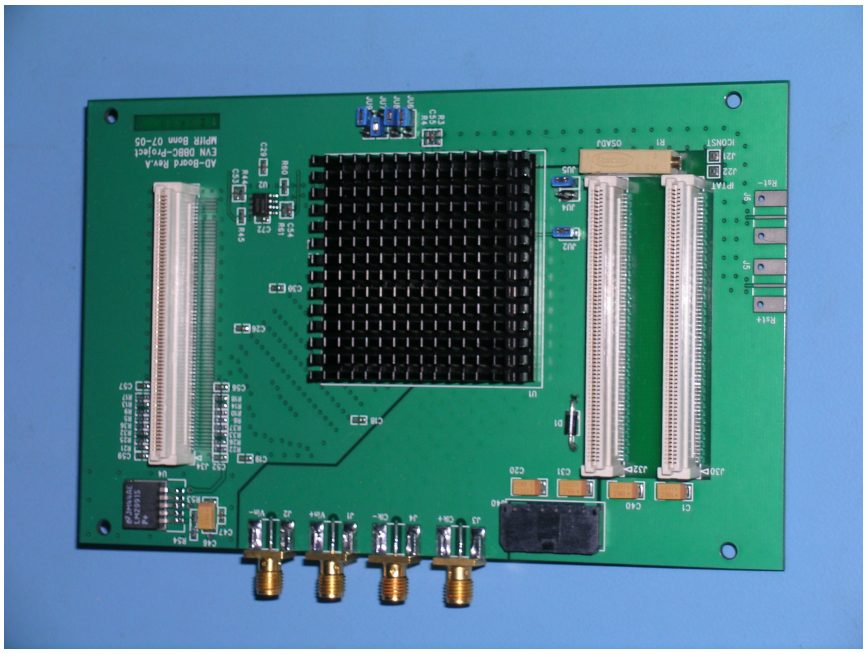
The device used in the ADB1 board is the MAX108 that is producing its output, for the sampling clock frequency selected 1.024 MHz, as two 8-bit demultiplexed bus at 512 MHz. The maximum data transfer rate within the DBBC bus with std levels LVPECL or LVDS is around 350 MHz in each of the differential lines, so the output data are propagated through the chain with the DDR method, that allows to limit the maximum digital signal frequency at 256 MHz.

RF input and clock are differential, but used as single-ended; the reset input is differential and used as differential. The reset is used to synchronise the different AD boards that are present in the chain with an appropriate high resolution 1PPS, produced by the Timing CaT board.

A number of additional features are included in the board in order to adapt it in different environment for a more general use.

The ADB1 simplified general features are as follows, while additional information can be found in the MAX108 datasheet:

Input RF: 0- 2.2 GHz
Max sampling clock: 1.5 GHz
Output Data: 2 x 8-bit @ ¼ Sampling clk DDR



ADBoard1 front view

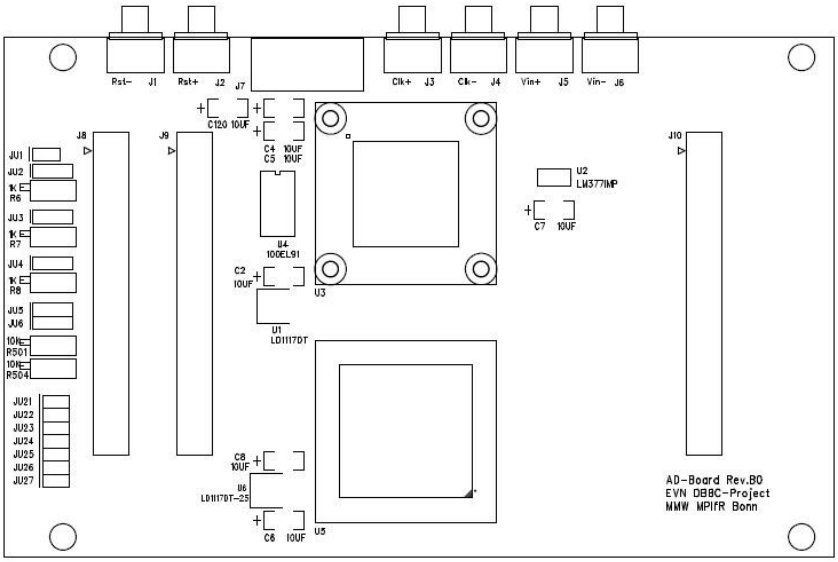
4. ADBoard2

An upgrade version of the sampler board is under development. Such board is able to replace the first in terms of geometry and interconnection compatibility and presents a number of improvements with respect to the first. It can be used with both types of CoreBoard.

The boards includes together with the sampling device a demultiplexer chip in order to be able to be used at the maximum rates

The main characteristics are:

Input RF: 0 – 3.5 GHz
Max Sampling clock: 2.2 GHz
Output Data: 2 x 8-bit @ 1/4 Sampling clk DDR , 4 x 8-bit @ 1/8 Sampling clk DDR, and several other modes.
Piggy-back module support for 10-bit output and connection with FiLa10G board.



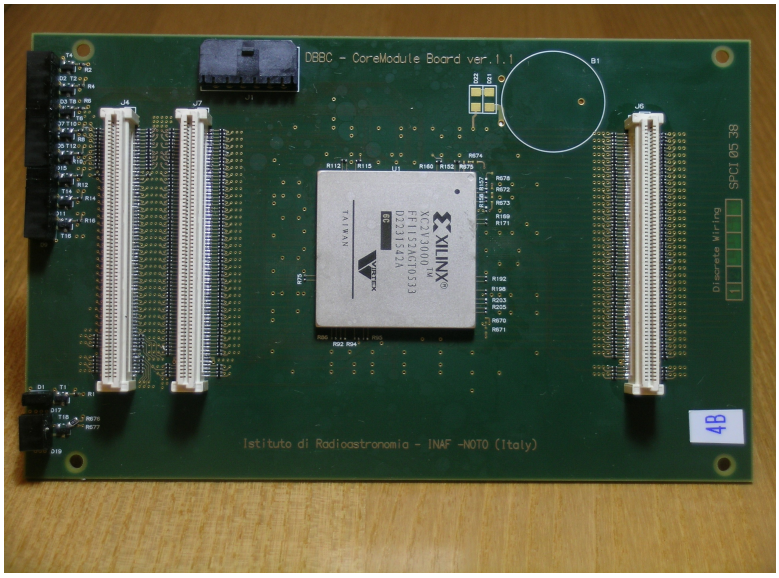
The schematic aspect of the ADBoard2

5. CoreBoard1

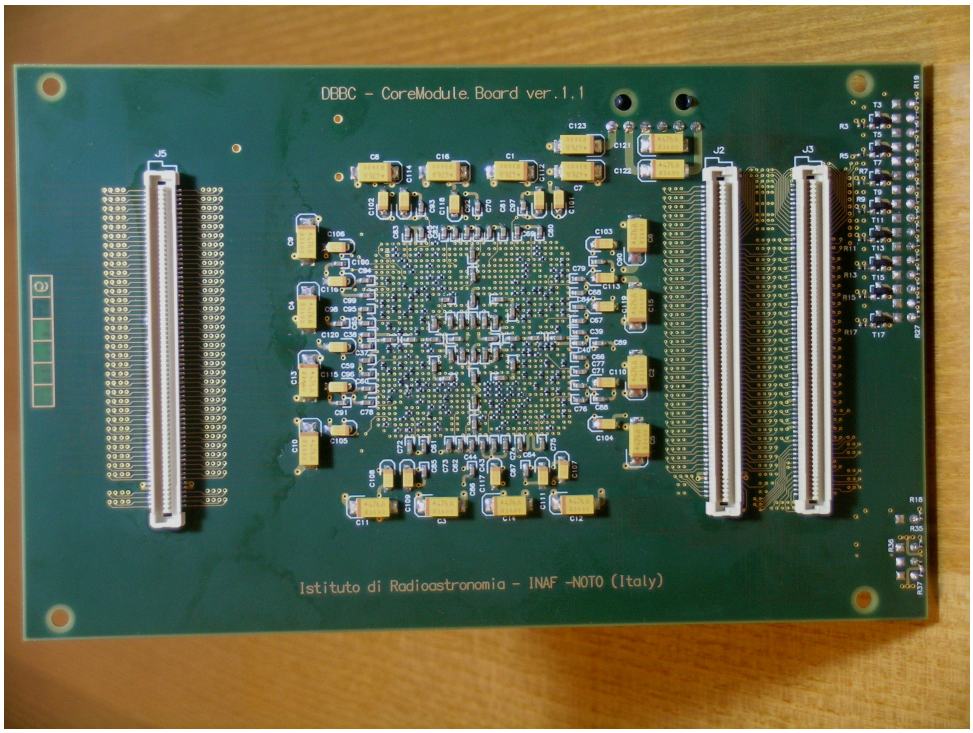
The CoreBoard1 is the main processing element of the DBBC chain. It includes a single FPGA device connectied to the three communication bus (described in the ADB1 section). The board features is a very high density interconnection scheme where impedance and length of the different bus are kept under a severe control. This allows to achieve satisfying performance at the planned maximum data rate. The standard differential levels adopted are LVPECL, but is possible to use LVDS under an appropriate resistors termination selection.

Sixteen leds are used to inform about 1PPS presence, DCM lock status, 80 Hz amplitude calibration presence, type of configuration loaded.

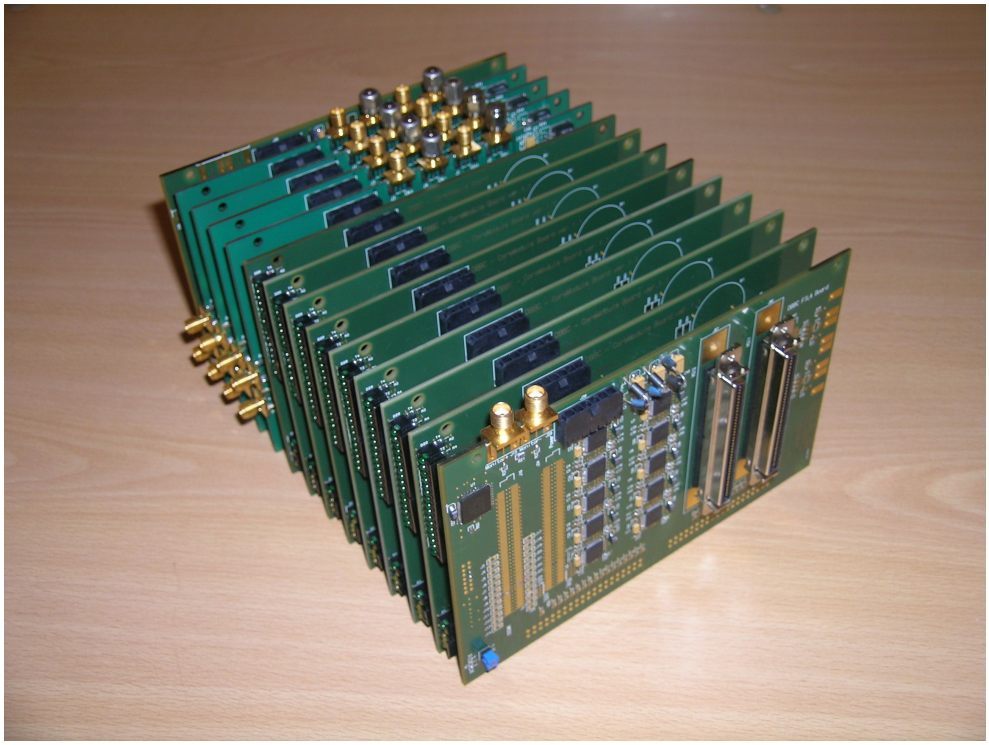
The device normally adopted is a Xilinx VirtexII 3000, that can be used for realise the functionality of a down conversion process, equivalent to an analog base band converter. Different FPGA devices could be adopted up to the biggest one available from the same family in the same board without any further modification for additional processing resources.



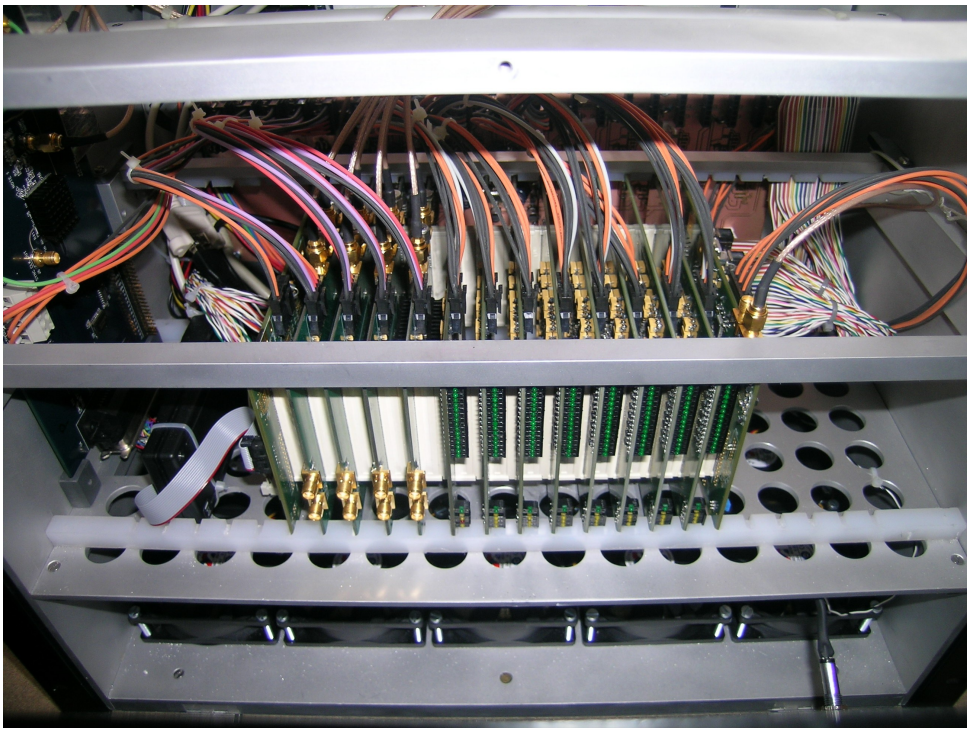
The CoreBoard1 in a front side view.



The CoreBoard1 in a rear side view.



4 ADBoard + 8 CoreModule Stack



4 ADBoard and 8 CoreModule Stack mounted in the rack

6. CoreBoard2

An upgrade of the processing board has been developed for improving the performance. Such board operates with LVDS only logic levels and perform the processing capability of four equivalent CoreBoard1 with the std 3000 device. So a maximum of four units of CoreBoard2 are necessary for performing the complete functionalities of a 16 BBCs analog equivalent system.

Similarly to the ADB2 the geometric elements and connections are compatible with the version 1 of the system.

At present such revision of board is under evaluation because of the very large number of additional features it should be able to offer. It is expected to be mounted in the two units (four boards each) for Tigo and O'Higgins stations and then it will be evaluated in the second part of this year. The first use will be with ADB1 sampler units.

No termination resistors are adopted as dynamic termination techniques offered by the Xilinx devices will be adopted. Such modification implies an important reduction in the board assembly efforts, while in the board realization the restrictions and tolerances have been further increased in for its use with the ADB2 sampler boards and possible future still faster system clock.

7. FiLa Board

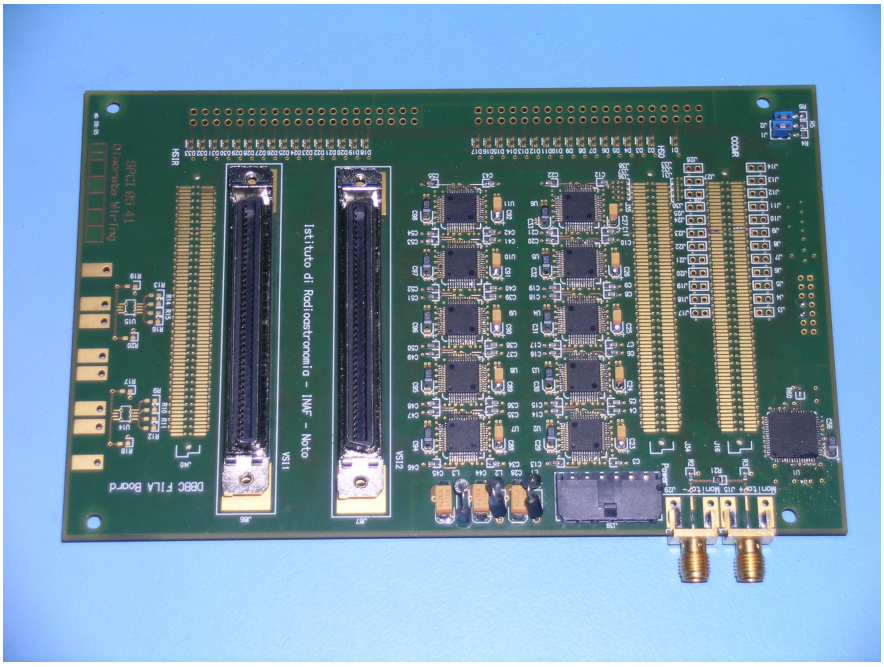
The first and last board of the chain is just the FiLa board. It's a pretty general purpose element supporting several functionalities.

As first element it is in charge for:

a) Communication Interface with Core Boards
b) JTAG programming channel
c) 1PPS chain insertion

As last element is used as:

a) Double VSI Interfaces with variable equalization factor
b) DA Converter
c) System 1PPS monitor output
d) Noise calibration 80 Hz output



FiLa - board Last

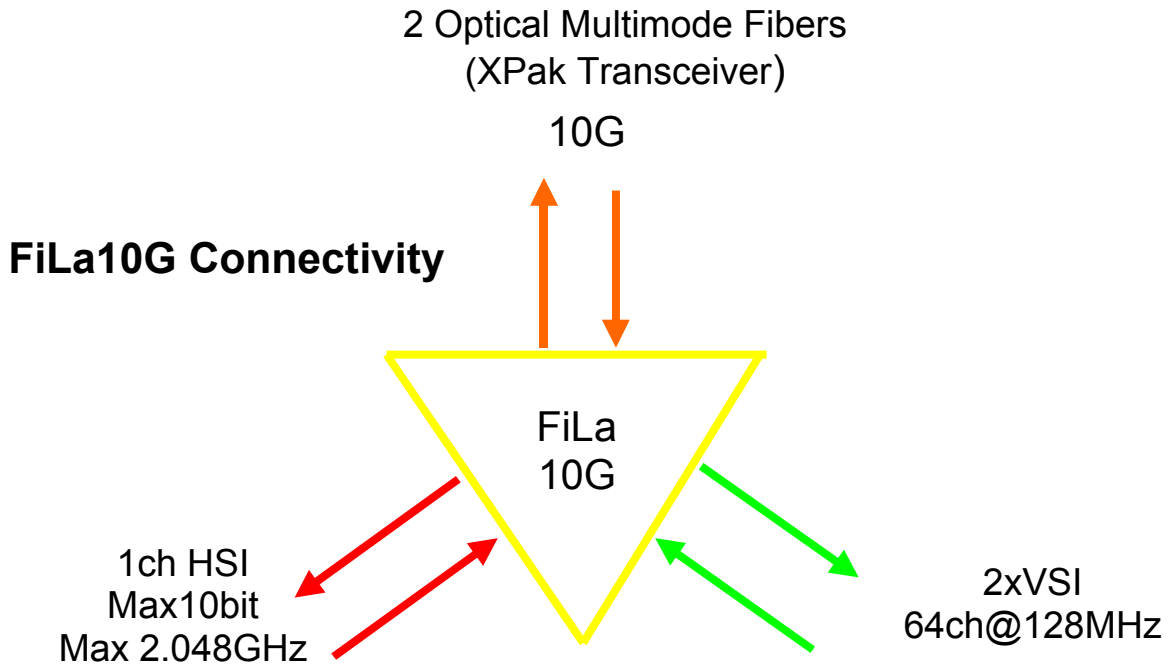
8. FiLa10G Board

It was felt as having VSI standard as unique output of the system was a limitation. Moreover it could have been useful to separate ADBoards from the system to have them placed in a receiver. So the necessity to join in both directions the processing chain with remote ADB should have been assured. Finally the pure sampled data available on VSI standard could allow to join a receiver with a recorder is an easy fashion.

In total a triangle connection is involved, and the FiLa10G board is under development to meet such requirements. The main features are:

- Piggy-back board of ADB2
- Triangle connection between HSI (DBBC fast sampled data bus) – 2xVSI – 2x10Gb link
- It can be placed either at the beginning of the chain or at the end (again First and Last)
- The ADB2 is able to support FiLa10G for *pure sampled* data transmission
- The FiLa output board is able to support FiLa10G for *processed* data transmission
- It is a 2xVSI < - > 10G converter
- DBBC output can be in parallel via 2xVSI and 10G

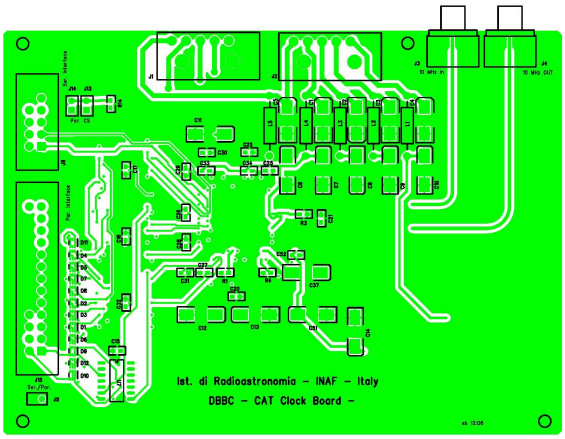
The hardware is expected in mid-2007, while the complete firmware development will adopt a dedicated development with the help of commercial macros. Time completion will depend by the number of interested users.



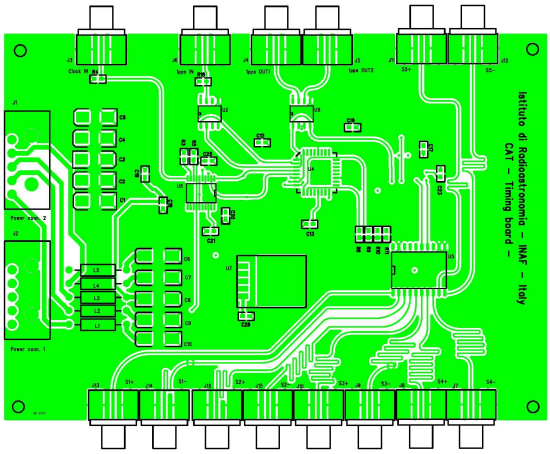
9. CaT Boards

The Clock and Timing boards are used to produce the clock and the synchronization signals. The Clock board is receiving a 10 MHz from as reference and is able to produce a programmable set of sampling clock values including 1024 MHz and 2^30 Hz. The first is used as std clock for the DBBC in the MK4/VLBA mode, while the second is usable for 1 Hz resolution without any phase correction algorithm.
Phase jitter performance have been evaluated only in prototypes while a final version is expected in few weeks for the final performance determination. Particular care has been placed in the substrate choice in order to minimise temperature dependant behaviours.

The Timing CaT board is developed to generate high resolution station 1PPS copies to be used by the AD Boards in both versions for synchronization purposes. Time synchronization is realized with system clock up to about 3 GHz.



CaT – Clock Board



CaT – Timing Board

10. Power Set

The PowerSet unit is composed by 4 commercial switching power supply elements and a Power Distributor Board. Such board is generating all the voltage rails necessary for powering the board in the chain, for a complete version. Great deal is assured to separate the different voltages of a same voltage value in those situations where digital and analog sections are supplied.

The maximum current for the FPGA core parts is around 6A for a maximum number of 16 units. Such voltage can be set to the standard adopted values by the different Xilinx FPGA families.

11. PC Set

The system includes a single board PC for managing all the operations related to communication and settings. This is realized with the additional presence of two commercial interface boards, operating on a PCI backplane, an hard disk where the configuration files and control software is placed.

The main functionalities realized by the PCSet are:

a) FPGA device configuration through USB – JTAG interface.

b) Communication with 32-bit bus with the CoreBoards for register setting, total power measurement, statistics of the state, single channel automatic gain control, etc.

c) Communication with Conditioning Modules for IF total power measure, automatic gain control, registers control.

d) Field System interface through a network connection.

12. Configuration Set

It is the collection of configuration files available for different IF input, base band number, bandwidth.

At present only down-conversion type has been designed, while several other architectures have been produced as prototype, including multi-channel equi-spaced, autocorrelation, RFI mitigation. Moreover a total 512 MHz version is available for very wide band observations.

The filter shape for the different bandwidth is the superimposition of several multirate filters and has been driven in order to follow, for what is possible, the analog shape of the filters at present used in the analog terminals.

The configuration available now are 16, 8, 4, 2, 1 MHz, with tuning ability related to the frequency step of 1024 x 10^6 / 2^32 = 0.23xxx Hz. When the integer required value is not met with the local oscillators, an additional software is adopted to take care of the residual phase difference, that is upgraded at each second.

13. Management Software and Field System Interface

This section describes the basic commands the DBBC is able to recognize. The structure and the meaning of the different commands is Field System based, so to simplify the dialogue with the FS and minimize efforts on the FS side. Any commands sent to the interpreter from the DBBC console is then identical to the command sent from the Field System environment. Similarly output information issued by any command are reported in FS style.

At present five commands are defined for the main functionalities:

1)

DBBCnn = freq, IF, bwdU, bwdL, gainU, gainL, tpint
(DownConverterConfiguration)

or

DBBCnn = mch[2^k]
(MultiChannelEquiSpacedConfiguration)

where

nn => 01, .. ,16 indicates the number of CoreModule;

freq => is the base band frequency in MHz, in the range 0010.000000 - 2,200.000000;

IF => i1(i2i3i4) set the input channel between the four, A, B, C, D.
A mixed mode is possible with a maximum of all the four IFs feeding a CoreModule for not standard configurations;

bwdU => band width of the upper side, in MHz;

bwdL => band width of the lower side, in MHz;

gainU => gain of the upper side in dB, in the range 0 - 40, step 1. If AGC is indicated the gain is automatically set so to satisfy the optimal level for the magnitude bit.

gainL => gain of the lower side in dB, in the range 0 - 40, step 1. If AGC is indicated the gain is automatically set so to satisfy the optimal level for the magnitude bit.

tpint => total power integration time in seconds, in the range 0.25 - 60, step 0.25.

k => in the range 0 - 5.

DBBCnn

reports the setting of the CoreModule nn.

2)

DBBCIF = inputA, gainA, inputB, gainB, inputC, gainC, inputD, gainD

where

inputA/B/C/D => input channel of the four possible (1,2,3,4) for each of the four IFs (A,B,C,D); the following are possible: A1,A2,A3,A4, B1,B2,B3,B4, C1,C2,C3,C4, D1,D2,D3,D4.

gainA/B/C/D => the gain of the channel is set in manual mode if a number is indicated in the range -15.5 to +15.5 dB, step 0.5 dB. If AGC is indicated the gain is automatically set so to satisfy the optimal level for the analog to digital converter.

DBBCIF

reports the settings of the IFs modules.

3)

DBBCFORM = VSI mode

where

VSI mode => is the mapping of the 32 channels in the VSI1/2 interface. Possible predefined values are: GEO, ASTRO, as defined by the VSI MK4/VSIC mapping, and MCHMnn, for multichannel mapping. Other generic configurations can be defined with dedicated mapping definition files.

DBBCFORM

reports the settings of the VSI output mapping.

4)

DBBCMON= bnn[u|l]

set the Digital to Analog Channel source.

nn => 01, .. ,16 (in DCC), .. 64 (in MCHM) indicates the number of band;
u/l => upper or lower side band (in DCC)

DBBCMON

reports the Digital to Analog Channel source.

5)

DBBC = ' *direct string* '

send direct commands to the DBBC interpreter. It is used for testing functionality.

14. Feature of the system at the present status

- 4 RF/IF Input from 16 in a range up to 2.200 GHz
- Four polarizations or bands available for a single group of 64 output data channel selection (2 VSI output connectors with 1, 2 Gb/s each)
- 1024 MHz sampling clock
- Channel bandwidth ranging between 1 MHz and 16 MHz (MK4 modes), U&L
- Wide band 512 MHz
- Tuning step < 1Hz
- Multiple architecture using fully re-configurable FPGA Core Modules (Down-Converter, Equally Spaced Multi-channel, etc.)
- Modular realization for cascaded stack processing

15. Upgrade feature of the system with ADB2 – Core2 – FiLa10G

- 4 RF/IF Input from 16 in a range up to 3.500 GHz
- 4 RF/IF Input from 16 sent/received with bidirectional FiLa10G
- Four polarizations or bands available for a single group of 64 output data channel selection (2 VSI output connectors with 1, 2, 4 Gb/s each), and sent with FiLa10G
- 2048 MHz sampling clock
- Wide band 1024 MHz

16. Feature of the system at general level - firmware independent

- DBBC chain operates up to 350 MHz in a single differential line
- The HSI/HSIR and HSO/HSOR bus are each composed by 64 differential data lines and 4 clock lines for a total aggregate data rate each of about 44.8 Gbps with DDR