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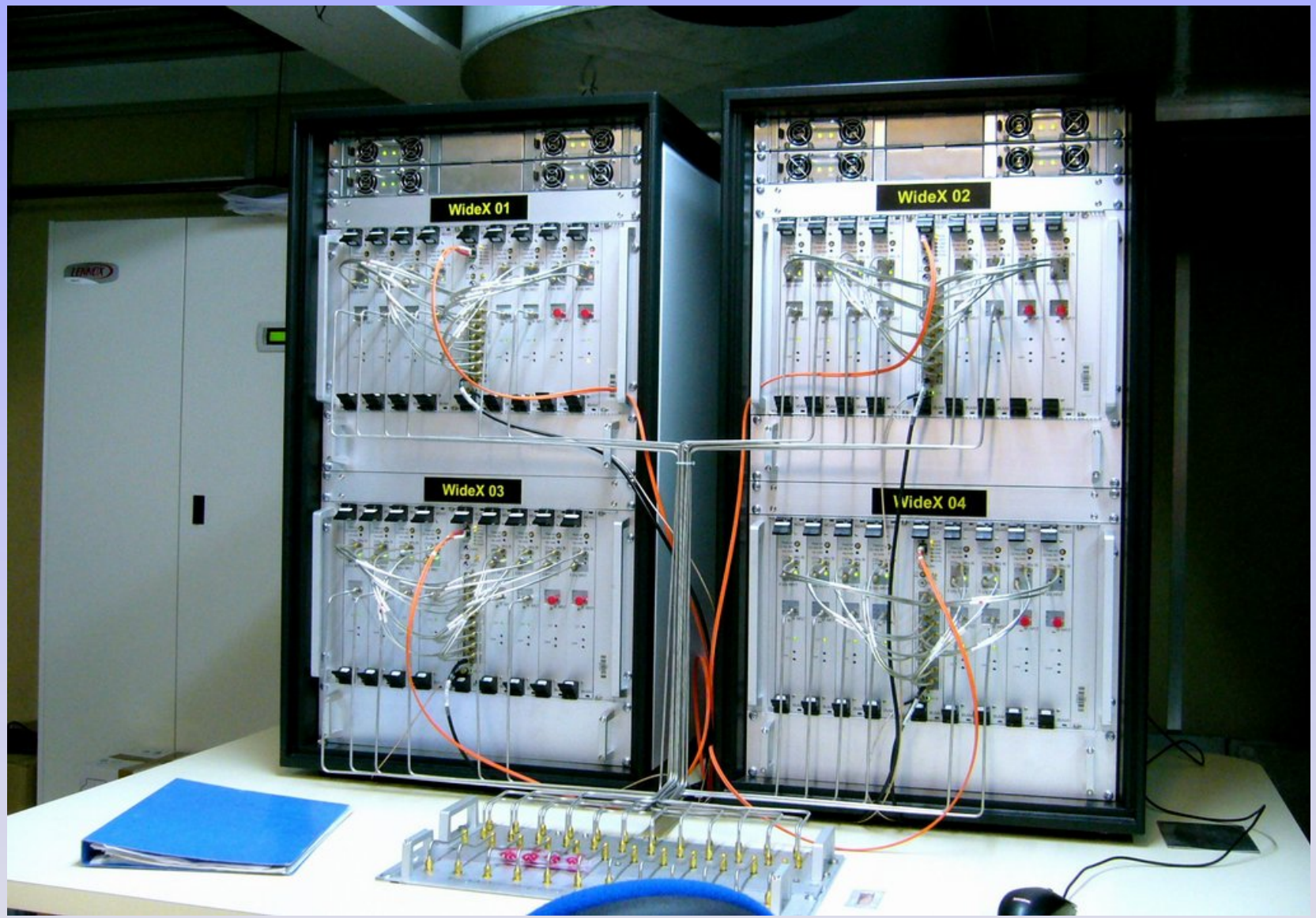
Correlators for the PdB interferometer :

Part 1 : The Widex correlator

Part 2: Development of next generation

Casper 2010

Marc Torres



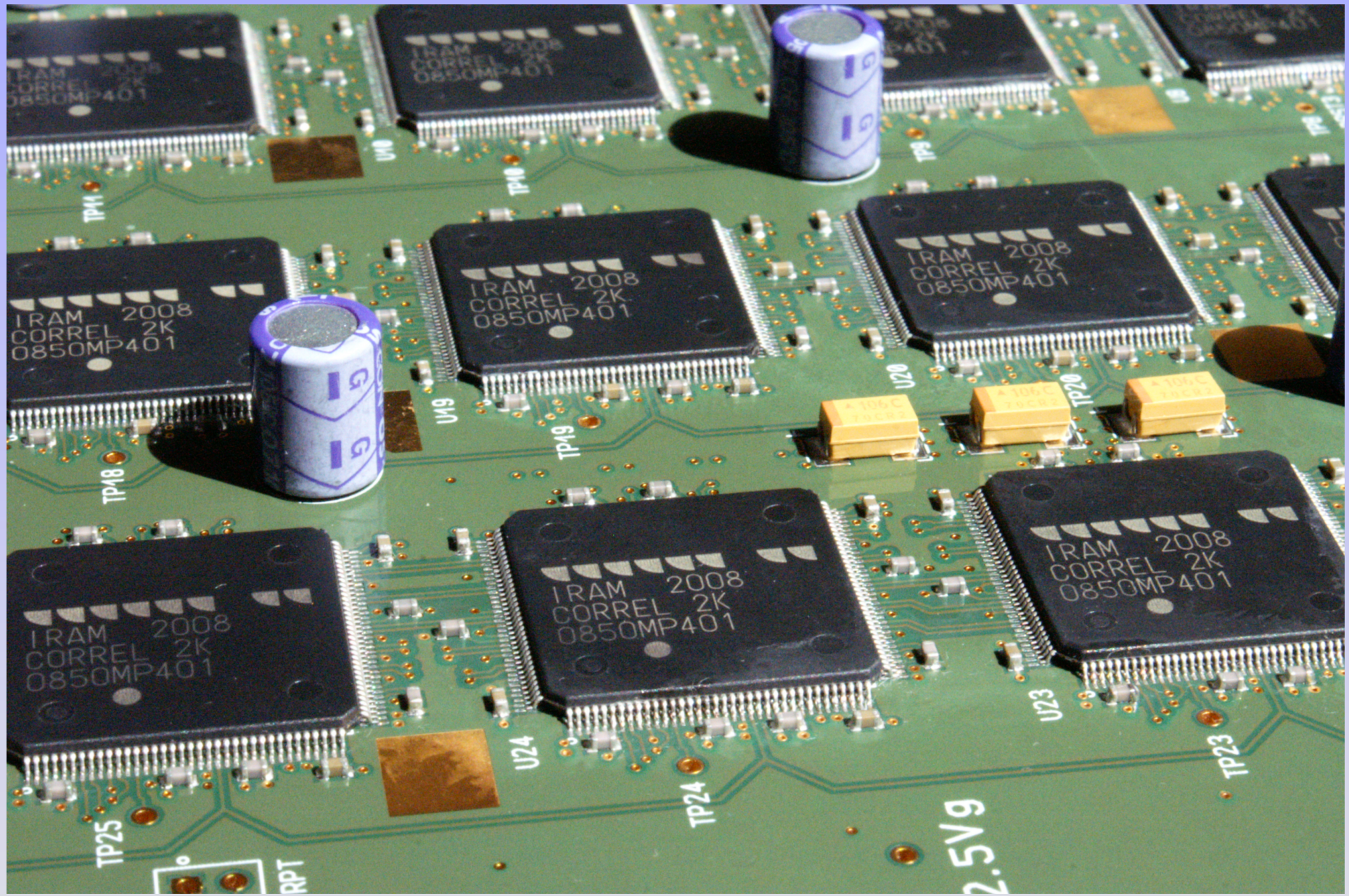
WideX : 4x2 GHz BW for 8 Antennas

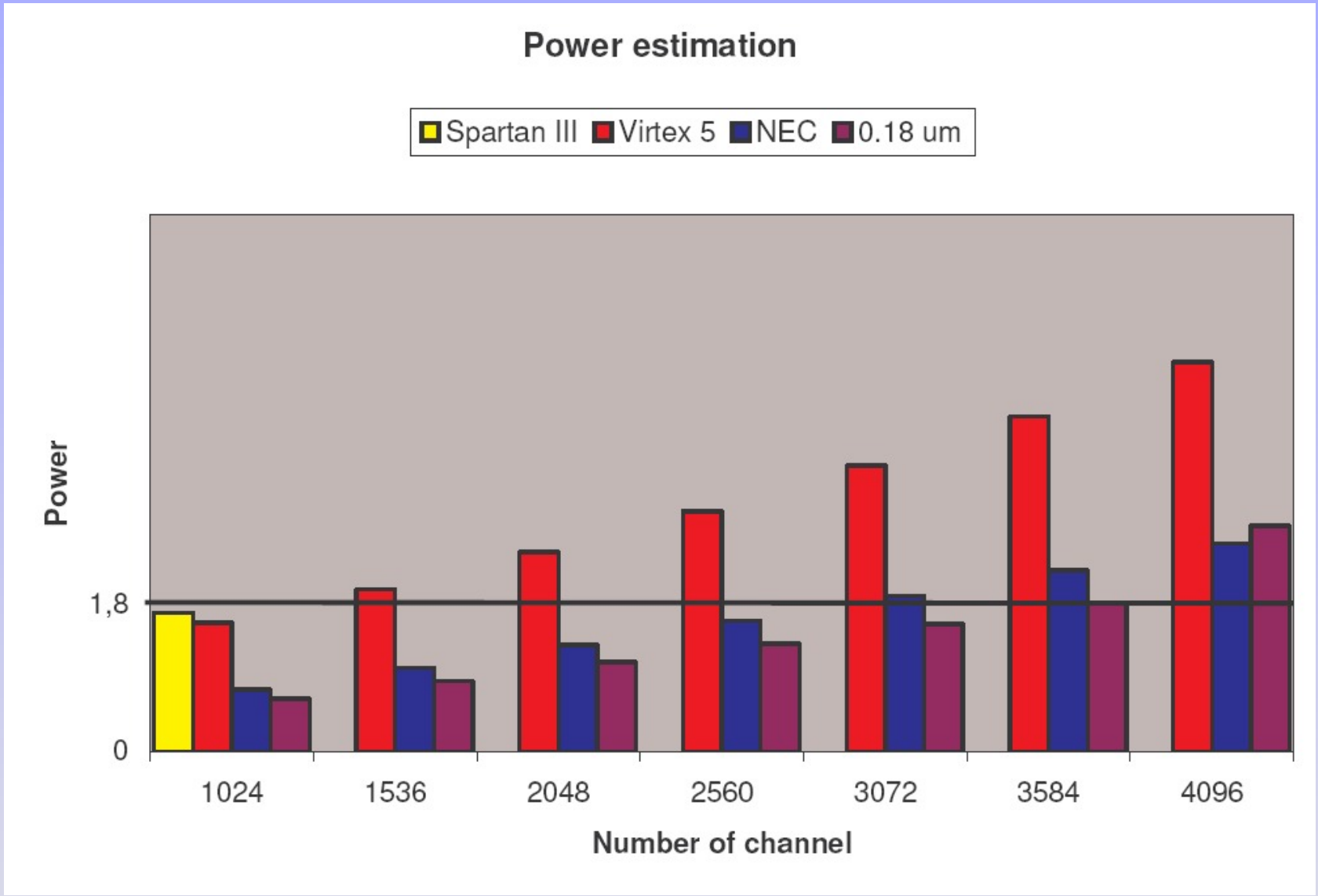
Sampling : 4 Gs/s , 2-bit 4-level, 2nd Nyquist window

Time multiplexed system : Format conversion to 16 streams, with bulk delay implemented in the Stratix3 FPGA internal RAM @250 MHz

Correlator chip	NEC 0.15um, 2048 lags, 250 MHz
Chips per board…	28
Boards per unit…	16
Correlator chip count…	1792

…. *(a flavour of ALMA, but reasonably sized)*


IRAM 2008
CORREL 2K
0850MP401
U19
U20
U23
U24
TP18
TP19
TP20
TP23
TP24
TP25
2.5V9



WideX correlator chip : ASIC vs. FPGA (Jan,2007)

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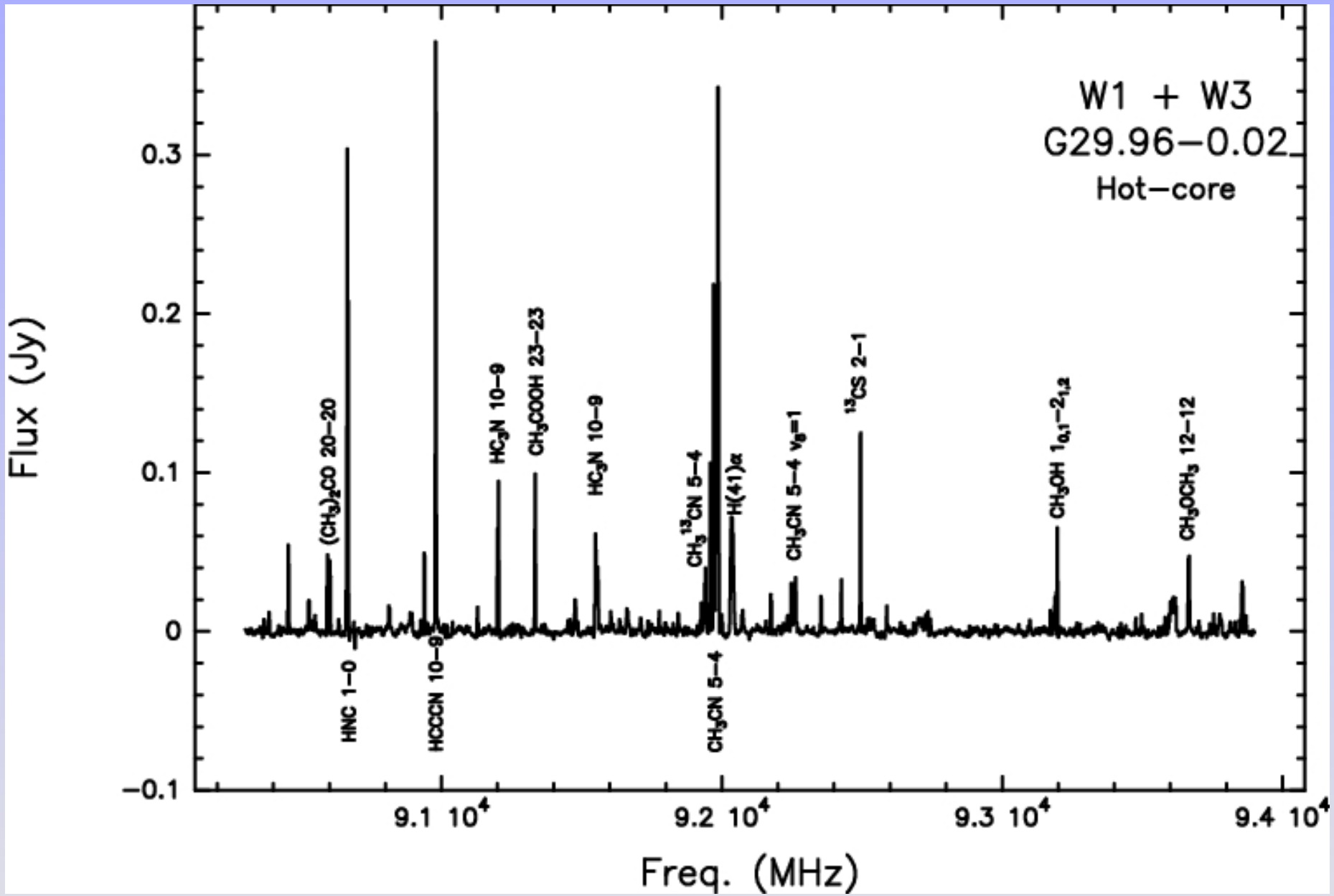
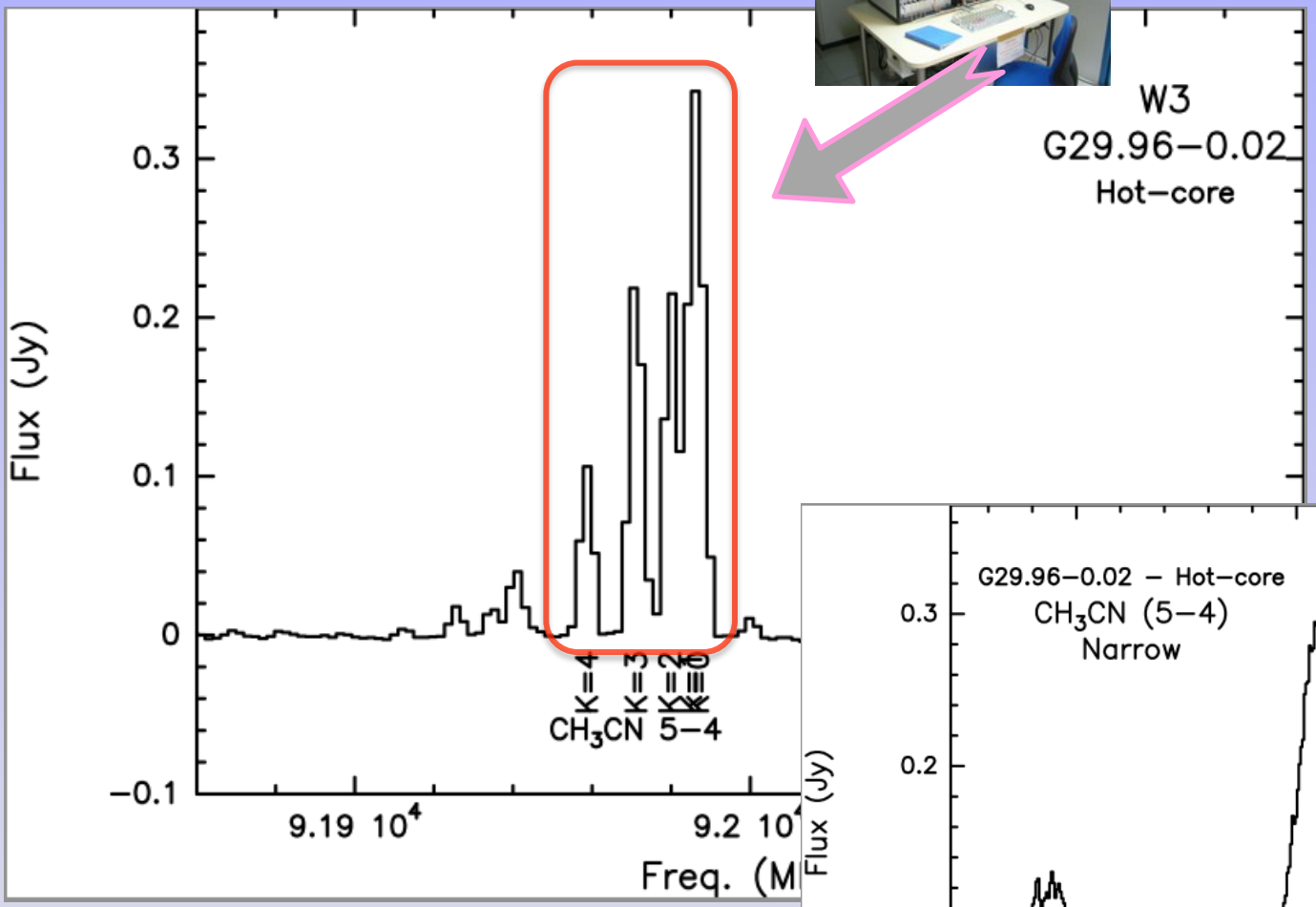
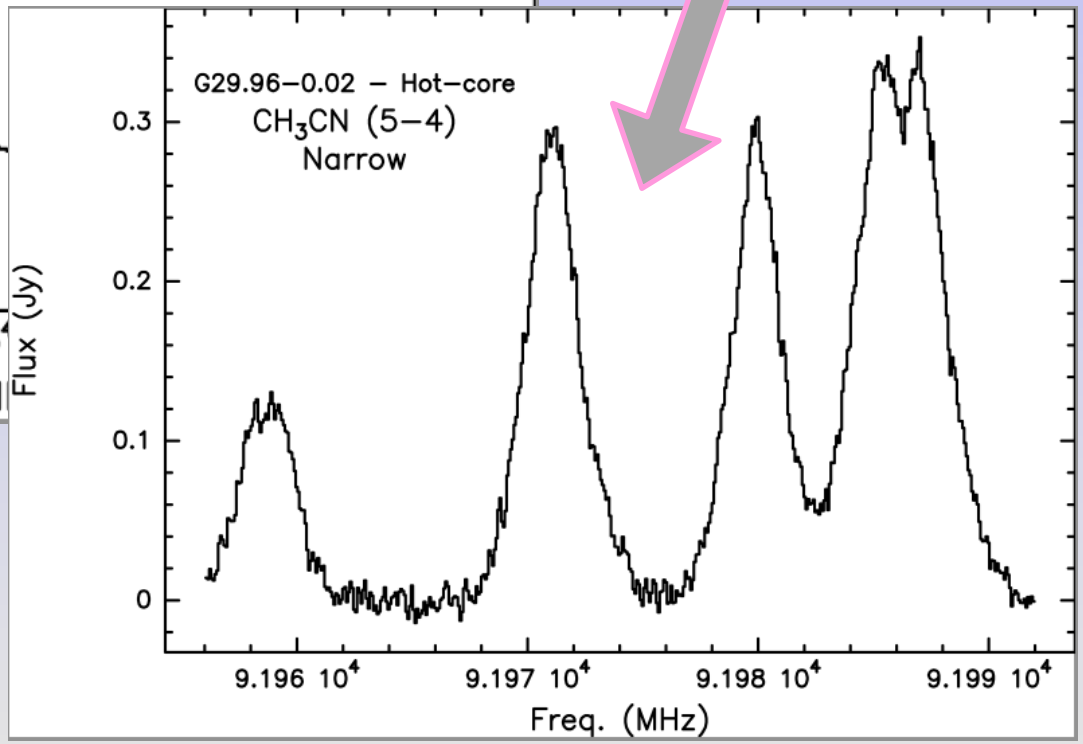
The total power
Is 5.1 KiloWatts

Probably the last
representative of an
extinguishing species…


W1 + W3
G29.96−0.02
Hot−core
Flux (Jy)
0.3
0.2
0.1
0
−0.1
9.1 10^4
9.2 10^4
9.3 10^4
9.4 10^4
Freq. (MHz)
(CH3)2CO 20−20
HNC 1−0
HCCCN 10−9
HC3N 10−9
CH3COOH 23−23
HC3N 10−9
CH3 13CN 5−4
CH3CN 5−4
H(41)α
CH3CN 5−4 v8=1
13CS 2−1
CH3OH 1a,1−2a,2
CH3OCH3 12−12


W3
G29.96−0.02
Hot−core
Flux (Jy)
0.3
0.2
0.1
0
−0.1
9.19 10^4
9.2 10^4
Freq. (M
K = 4
K = 3
K = 2
K = 1
K = 0
CH3CN 5−4


G29.96−0.02 − Hot−core
CH3CN (5−4)
Narrow
Flux (Jy)
0.3
0.2
0.1
0
9.196 10^4
9.197 10^4
9.198 10^4
9.199 10^4
Freq. (MHz)

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Part 2: Building blocks for the next generation

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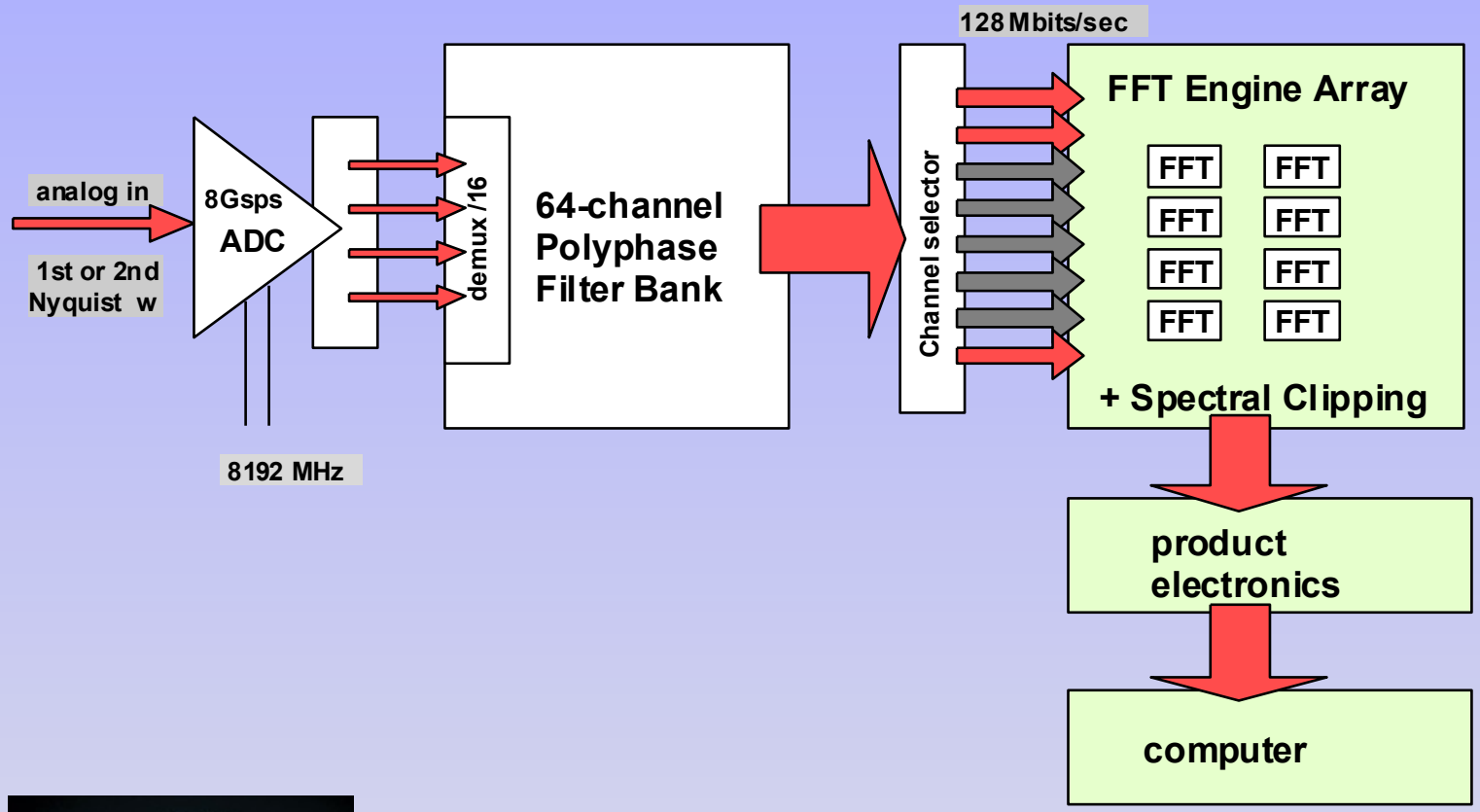
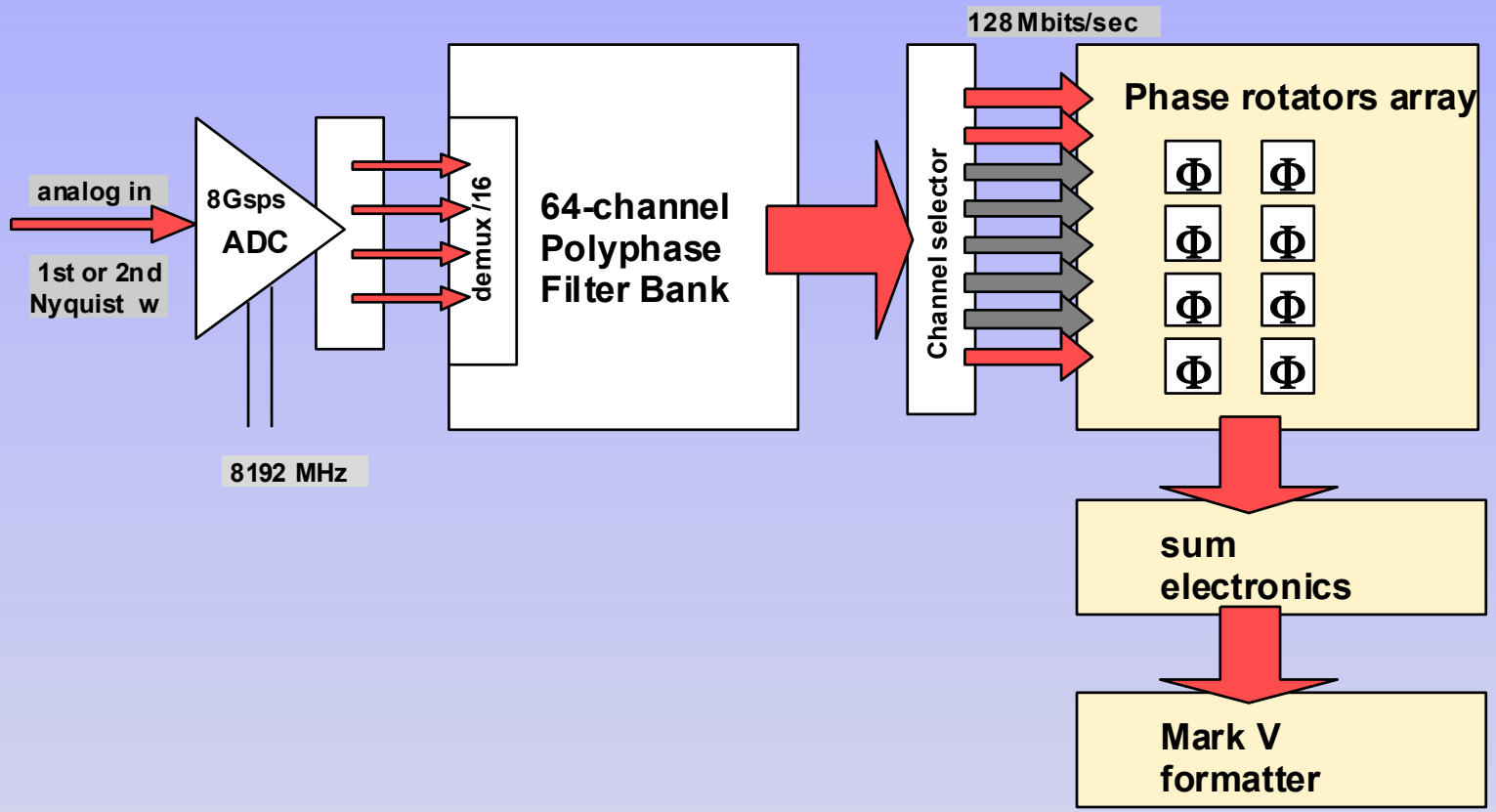


local interferometer configuration

One Channel is a digital stream of 16 bits@ 128 MHz (8 bits complex) representing a +/- 64 MHz chunk of IF frequency . The PFB delivers 64 such channels.



VLBI phased array configuration

Some merits of channelization

Merit 1: Only the selected channels are transmitted to the product electronics, which work at a low frequency.

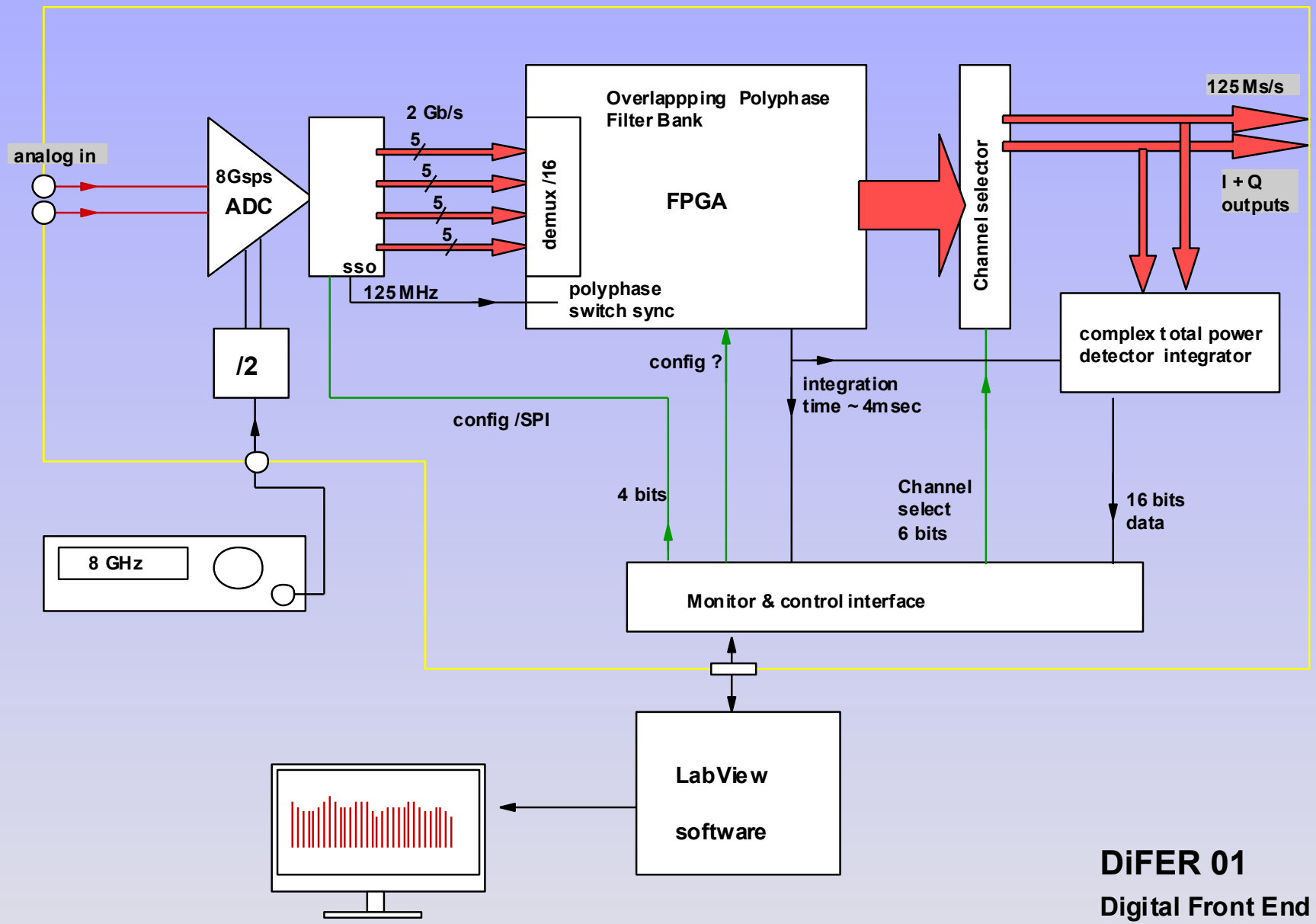
Merit 2: A 1-sample digital delay behaves as a fractional sample delay for the channel .

Merit 3: The additions for VLBI phased array mode are performed over a single channel , where the receiver group delays are assumed to be constant.

Bonus : Each channel can have a Total Power Detector to determine the receiver Temperature profile across the whole IF (64 points)

Design of a test PCB is in progress, based on :

- A 5-bit, 20Gsps ADC prototype chip, from a « famous manufacturer based in Grenoble »
- An ALTERA Stratix IV 230 GX, including 24 8 GBps transceivers
- An initial design clock speed of 8 GHz, to be increased as high as possible.



DiFER 01

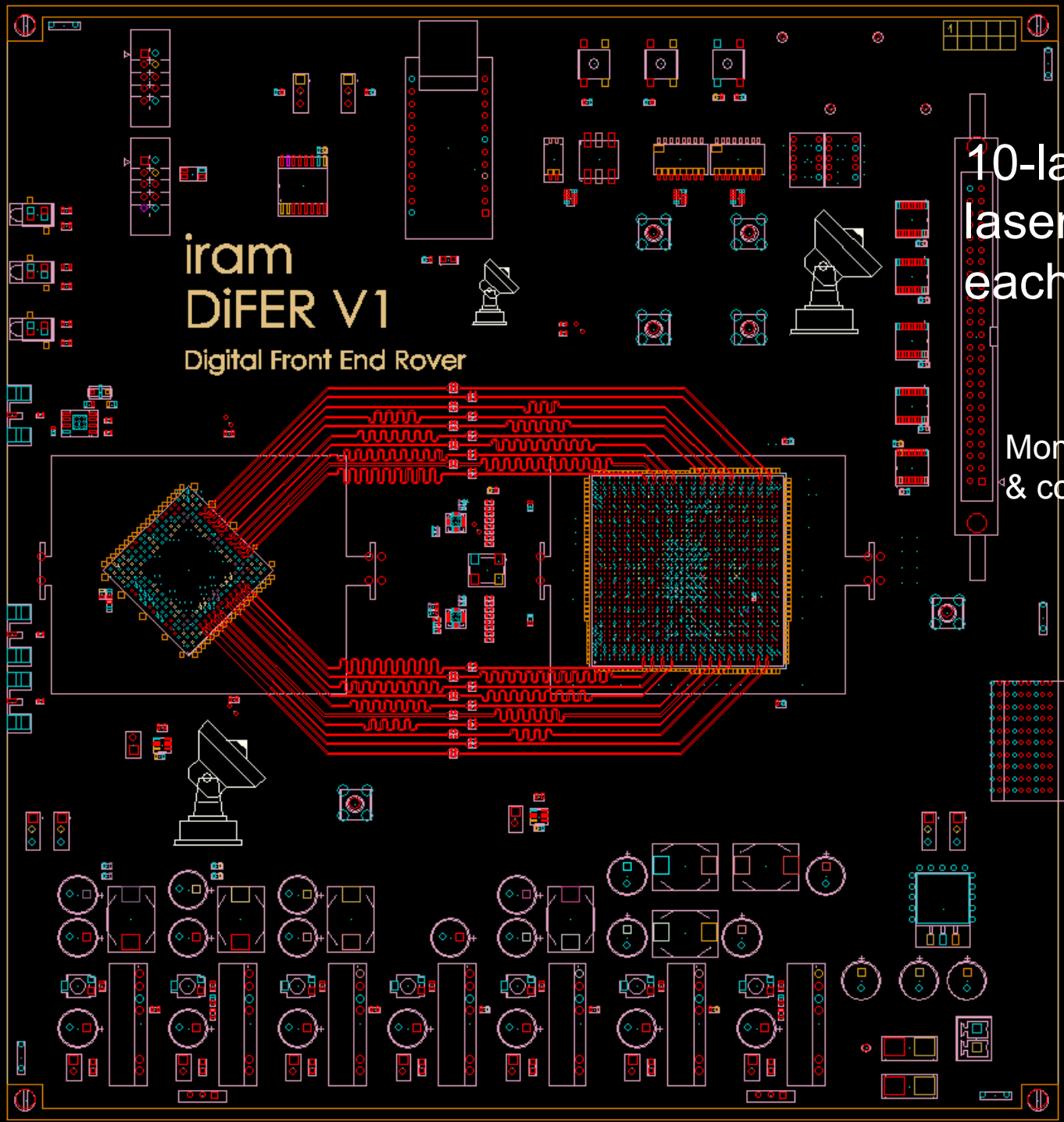
Digital Front End development setup
Stage 1 MT Aug 2009 rev Jan2010

Issues to be experimented :

- Synchronization of the 20 high speed data lines with the ALTERA transceivers (AC-coupled)

- Data de-scrambling from the Sonet $1+X^6+X^7$ sequence

- Synchronization of the polyphase switch to the ADC built-in /64 clock divider



10-layer PCB, laser via level each side

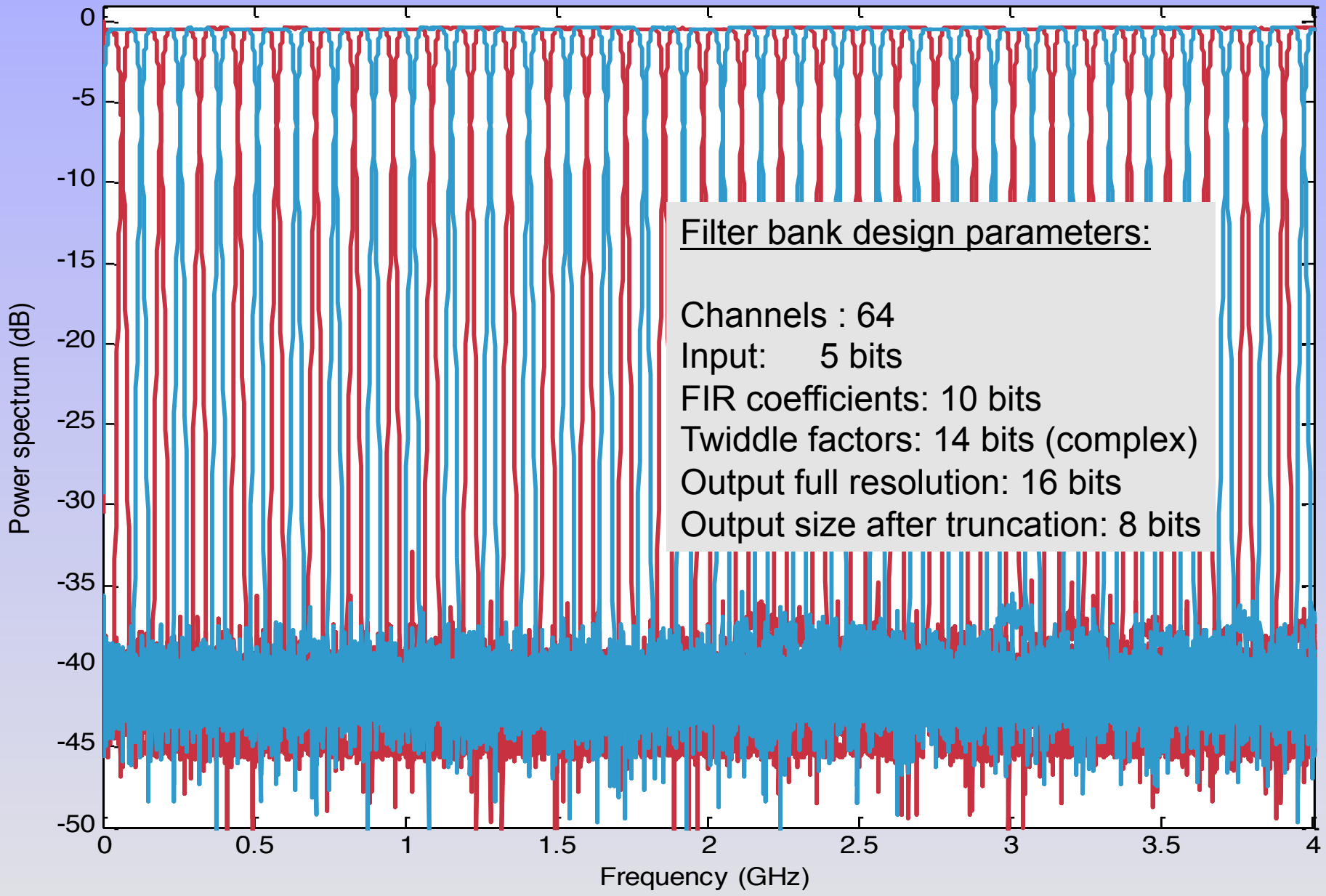
8 GHz Clock in

0-4 GHz Analog in

Monitor & control

Complex Channel Outputs

Overlapping Polyphase Filter Bank



Filter bank design parameters:

Channels : 64
Input: 5 bits
FIR coefficients: 10 bits
Twiddle factors: 14 bits (complex)
Output full resolution: 16 bits
Output size after truncation: 8 bits

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(simulation by Roberto Garcia)

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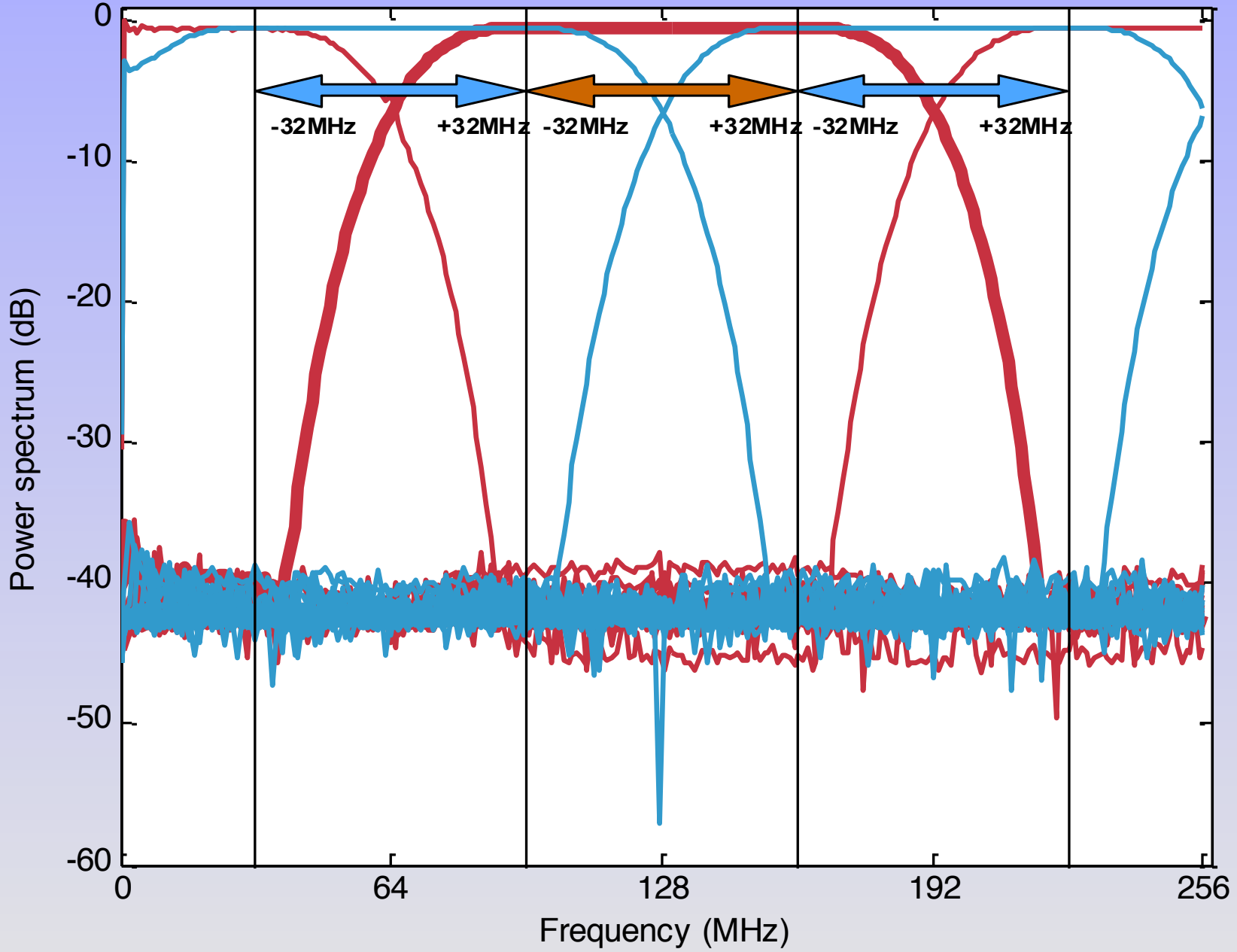
Spectral Clipping



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(simulation by Roberto Garcia)

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Some merits of the « half overlap and clip » channelization method

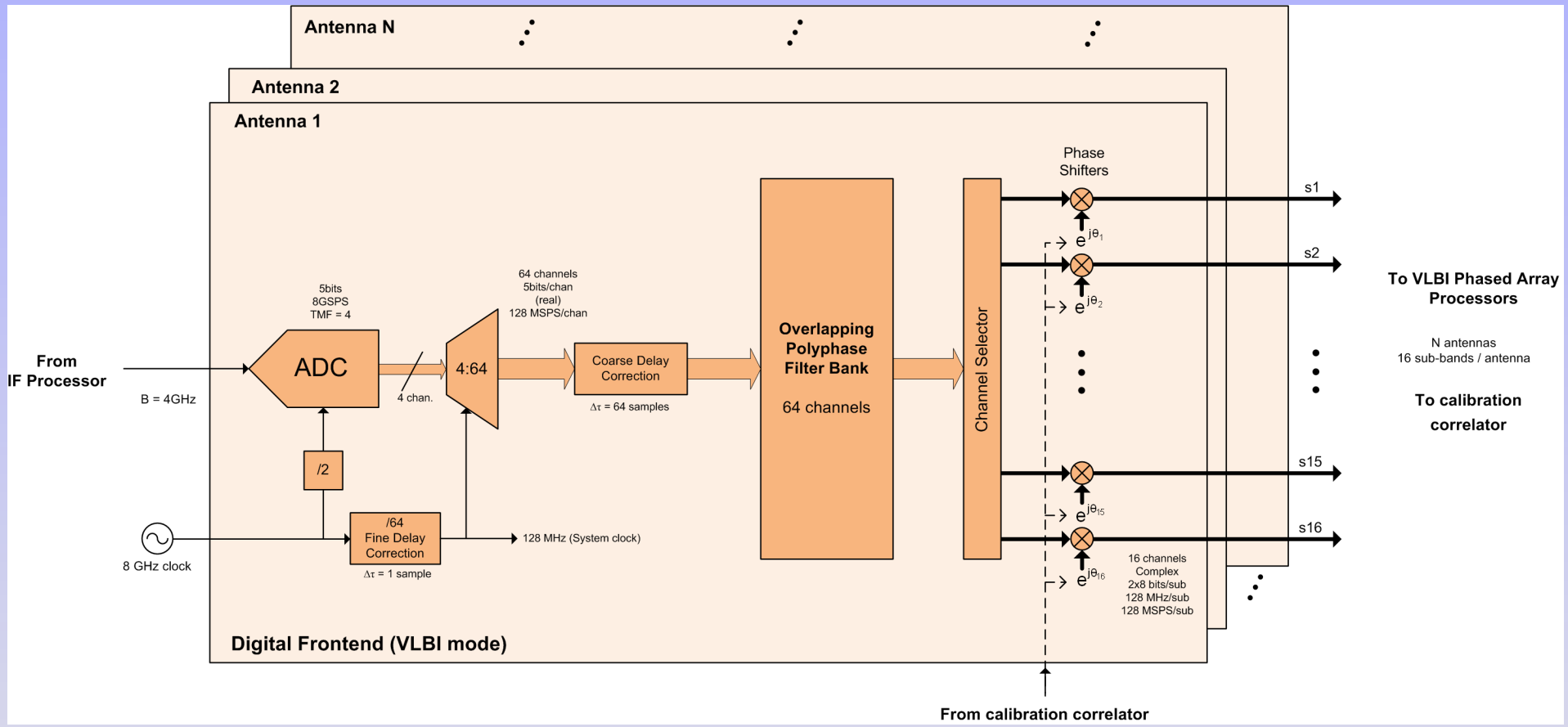
- Seamless stitching of the spectra.
- Naturally lends itself to polyphase implementation
- Prototype filter has few coefficients
- Backplane traffic is reduced by 2 if spectral clipping is performed in the signal electronics.

- The product electronics work on 100% useful data.
- The computers and archive work on 100% useful data

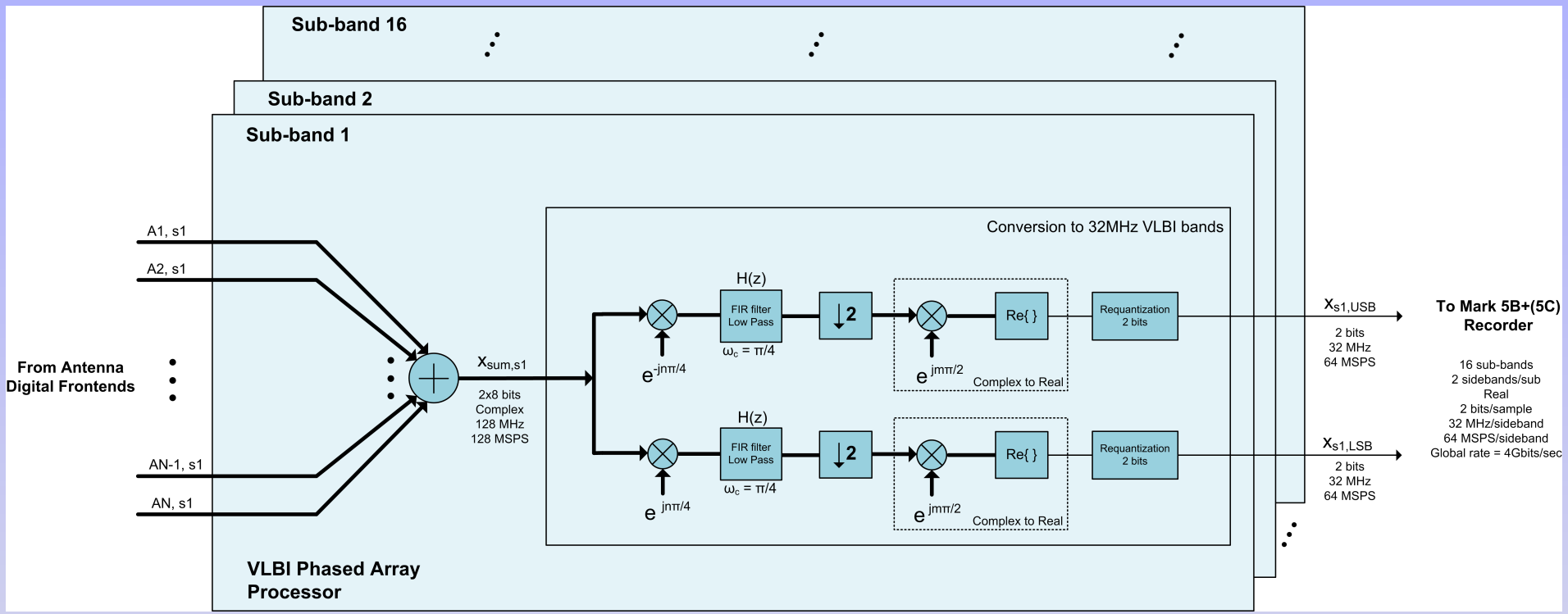
These savings largely pay off the sacrifice of 50% of the channels at the FFT level.

(note that doubling the number of points of an FFT engine requires little additional resource)

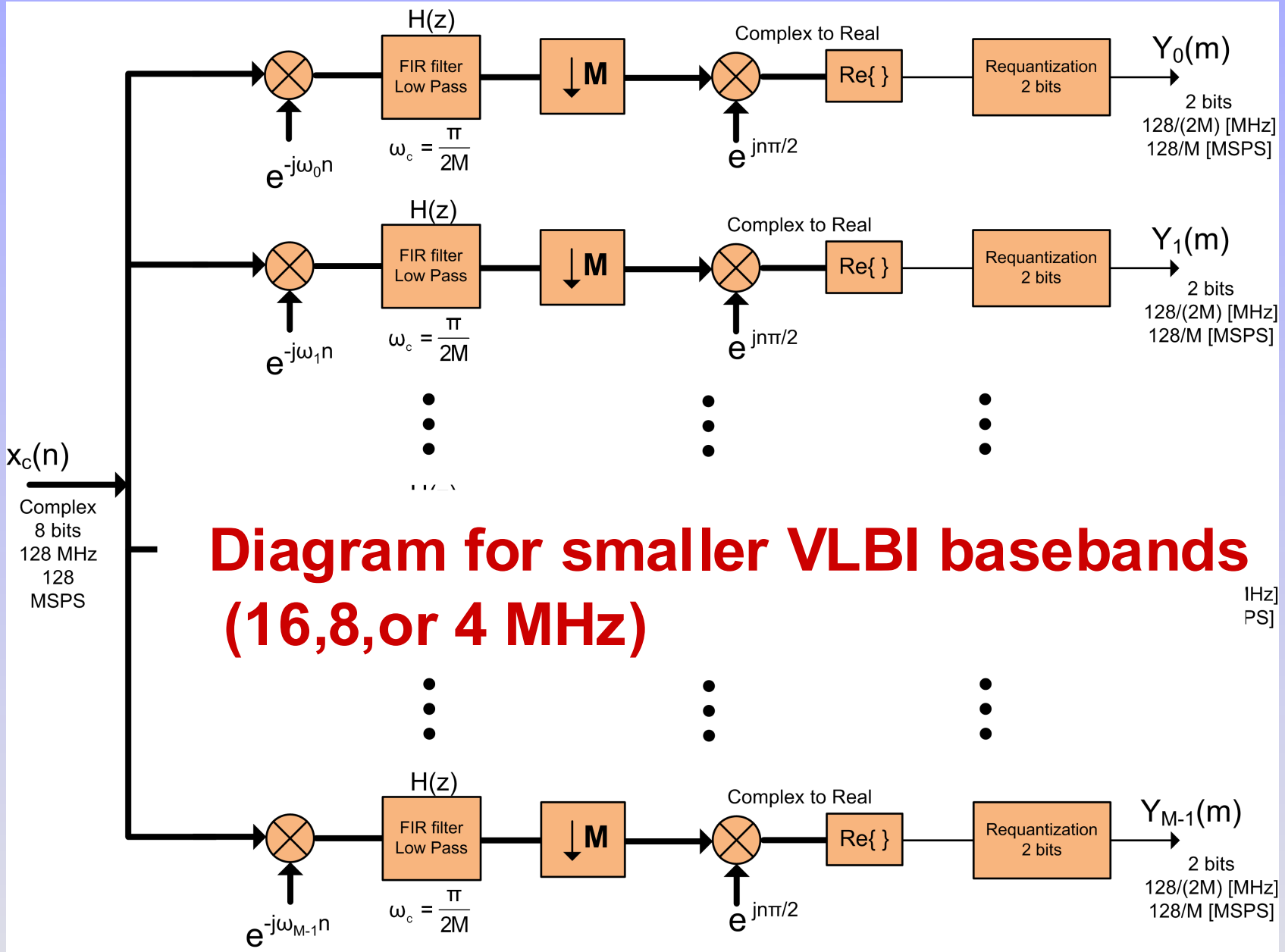
Digital front End for VLBI mode



For VLBI , the phase of every antenna is aligned on the reference antenna prior to summation.
This is performed for every BBC channel



Summation is performed on Complex Data then converted to Real 32 MHz USB and LSB basebands, later truncated to 2-bit for Mark 5 formatting and recording.



$$\omega_k = \frac{\pi}{2M}(2k - M + 1); \qquad k = 0,1,\ldots,M-1$$

Practical results expected 2010 Q4

To be followed by a 2nd version, targeted at interferometry :

- *Synchronization of two ADC's*
- *Fine delay system test*

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