The Digital Data Acquisition System for New Russian VLBI-network

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Introduction

Institute of Applied Astronomy currently develops a new VLBI-network based on small diameter antennas in Russia. It is intended for regular determination of Universal Time (UT) and Earth Orientation Parameters (EOP). For achievement of required sensitivity the data acquisition system should have wide recorded bandwidth. This poster reflects the development of this system.

The structure of the Digital Data Acquisition System

The basic structure of the Digital Data Acquisition System (DDAS) consists of four analog RF/IF downconverters and the Digital Backend (DBE). The basic DDAS could work in X and S frequency ranges in two polarizations. There are two X-downconverters that have input frequency range of 7.5-10.5 GHz and two S-downconverters of 2.2-2.7 GHz frequency range. The bandwidth of the DDAS channels could be 512 MHz or 1024 MHz in depends of the required mode. This structure will be implemented in the first stage of project. Then it will be extended in accordance with presented feeds by appropriate RF/IF converters.

The variant of extended DDAS with additional C- and Ku-downconverters is presented on Fig.1. For translation from Ku to IF frequency range double conversion is used. Ku-downconverter translates input signal to frequency range of X-downconverter which translate the signal to IF range. This method could be used for Ka frequency range (28-33 GHz) as well.

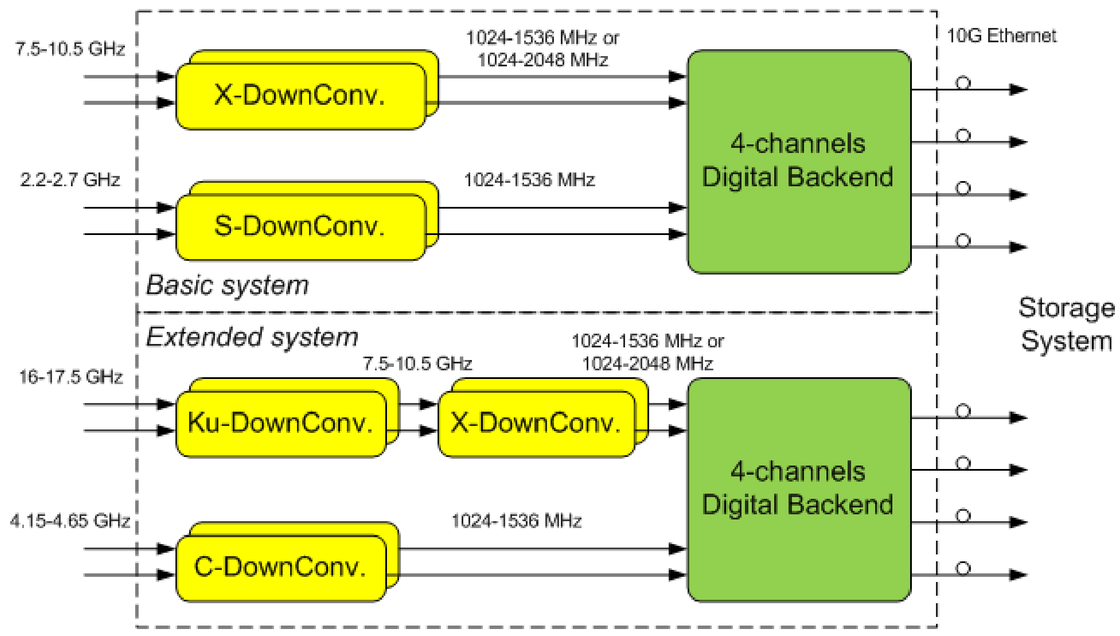

Fig. 1. Structure of the Digital Data Acquisition System

RF/IF downconverters

The RF/IF downconverters are set of microassembles located in thermally stabilized units situated on the moving part of antenna. Input and output frequencies of the downconverters are presented in Table 1. In X- and Ka-downconverters the frequency of translation could be set by means of tunable local oscillators.

Table 1. Input and output frequencies of RF/IF downconverters

Input frequency range	S	C	X	Ku	Ka
	2.2-2.7	4.15-4.65	7.5-10.5	16-17.5	28-33
Bandwidth, MHz	512	512	512/1024	512/1024	512/1024
LO	fixed	fixed	tunable	fixed	tunable

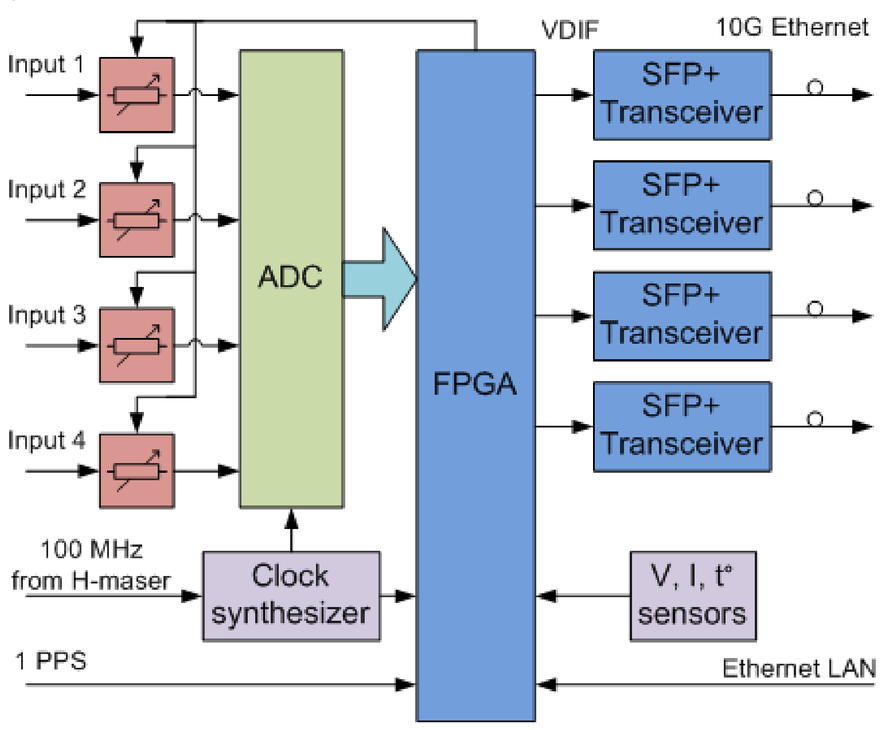

Fig. 2. 4-channels DBE unit

Digital Backend

The IF signals from downconverters are digitized by analog-to-digital converters (ADC) and processed by FPGA in the Digital Backend (Fig.2). The DBE unit is able to process four 512 MHz bandwidth channels or two 1024 MHz bandwidth channels. Depending on chosen bandwidth input signals are located in either third or second Nyquist zone. Corresponding signal spectrum inversion is compensated by FPGA.

FPGA quantizes input signals to 2-bits using RMS value as a threshold. It forms quantized data to VDIF frames and transmits it through 10G Ethernet optical interface to storage system. As well it is possible to transmit 8-bits samples from ADC for subsequent processing. Besides that the FPGA extracts multi-tone phase calibration signal (PCAL) and estimates distribution of quantized signal.

The DBE is implemented as single multilayer PCB and intended to be locate directly on the moving part of antenna.

Current state

The single channel prototype of DBE unit (Fig.3, left) was produced and has been tested. Currently firmware and software of the DBE prototype (Fig.3, right) is close to completion.

Developing and manufacturing of the 4-channels DBE and S, X-downconverters will be done by 2013. The entire DDAS will be created by 2014.

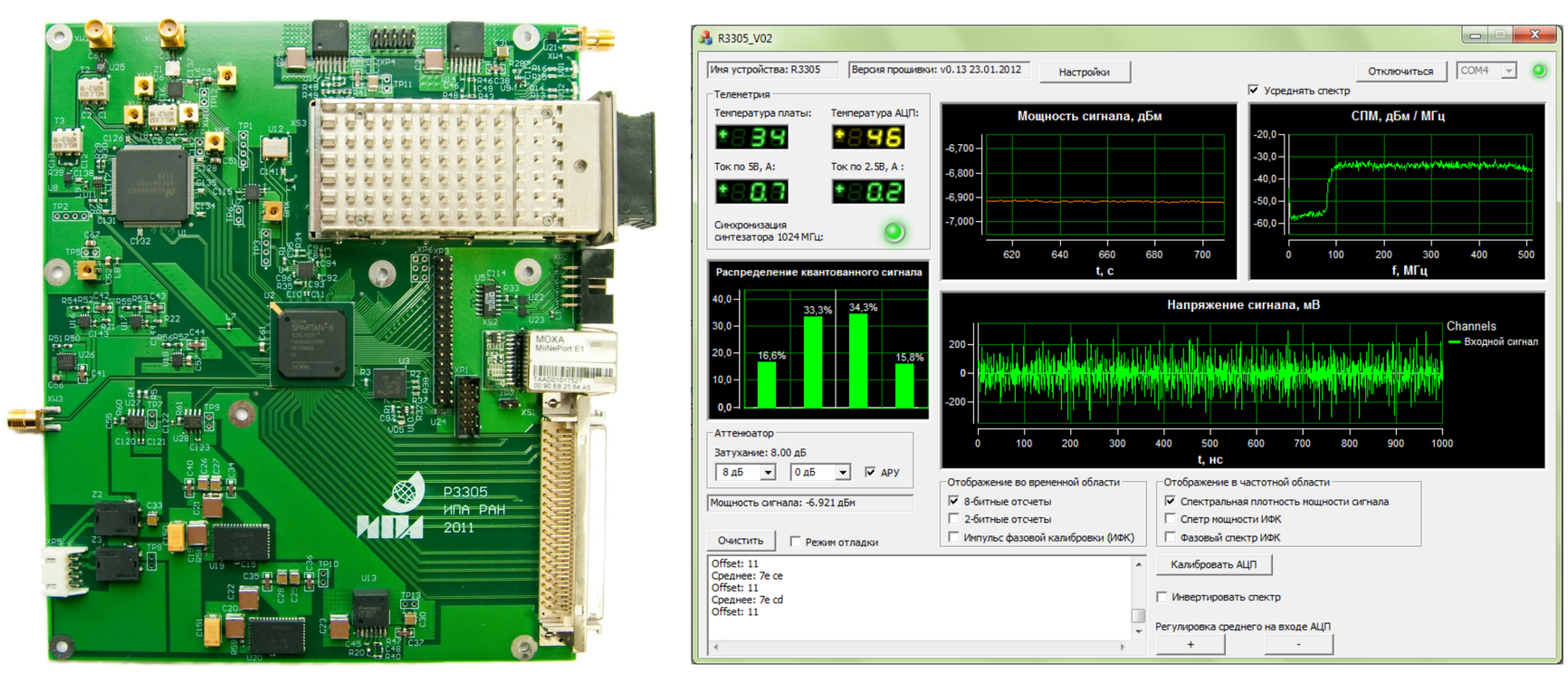

Fig. 3. The single channel prototype of DBE (left) and interface of control software (right)

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