FX-i-FILA10G - A FX Complex Cross-Correlator in FILA10G

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The FILA10G board is a FPGA based board mainly devoted to the Ethernet network data transfer for VLBI data acquisition purposes. A data transfer of 2x10 Gbps XFP bi-directional optical functionality is possible together with additionally 2 x 1-2-4 Gbps SFX connections for general purpose applications.

Input/output source could be selected either between four different VSI-H connections or dedicated DBBC HSI (High Speed Input bus) for pure sampled data as coming from a ADB2 board for connecting a digital RF/IF from the output of a receiver to a destination point, like a digital backend, VLBI correlator, etc. trough a standard 10G network connection.

Due to the general structure of the interface board is possible to implement other functionalities to build instruments or to perform general debug functionalities. In particular has been felt useful to have available the possibility to perform zero baseline correlation tests in order to be able to evaluate proper VLBI observation conditions. This could be performed as intra-VSI channels belonging to the same system, but coming from different IFs/ADB so as between different VSI-H channels belonging to different back-ends. Both this options are useful because the first is related to the possibility to evaluate proper functionality in different sections of the same system, while the second is additionally able to evaluate different reference clock and timing behaviours.

It needs to implement a complex cross-correlator to perform the needed functionality, and in particular it seems to be worth to take into consideration the FX architecture to fully implement the operations inside the FPGA. The FILA10G disposes of a Virtex4 FPGA with 2 hardware PowerPC for possible mixed hardware/software functionality integrated in the same device.

The general operations to be performed are:

1) Selection of the two input source data stream to be correlated
2) Delay in both the sources in case of needs for difference time adjust
3) Complex Fast Fourier transform
4) Complex multiplication
5) Integration
6) Data output for a numerical and visual inspection

A generic schematic diagram is shown, with the data flow to be implemented. Additional architectures are possible, but the proposed solution adopted is supported by the standard library of IP Cores available from Xilinx.

Number of channels to be implemented in parallel (1 to 16) should be evaluated during the development depending on the FPGA used resources.

It could be worth before implementing in the FPGA to develop a simple simulation run based on standard math tools like IDL or Mathcad.