Max-Planck-Institut für Radioastronomie

DBBC3 Testing for APEX and Pico Veleta

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DBBC3 EHT Design Review History

2018 Aug+Sep:

Tests on APEX DBBC3 in lab in Bonn
System characterization, zero-baseline test, comparison to R2DBE, etc

2018 Sep 13 Engineering Review Telecon

J Weintroub (chair) et al.
Generated 45 ORA's (Observation, Response & Action)

2018 Sep 14-24

39 ORA's addressed,
6 ORA's remain open (primarily improve the efficiency measurement)
Designed improved analogue noise source combiner network / ordered components

2018 Sep 25-Oct 24 (No activity - EHT 345 GHz fringe test, Alan in APEX)

2018 Oct 25-Nov 5 Components arrive, assembled improved combiner network
Addressing ORA #27 (excess PN in 2048 MHz sampler clock)
Addressing ORA #21 (better efficiency measurement)

2018 Nov 6 This meeting (EHT Collaboration Meeting Nijmegen)

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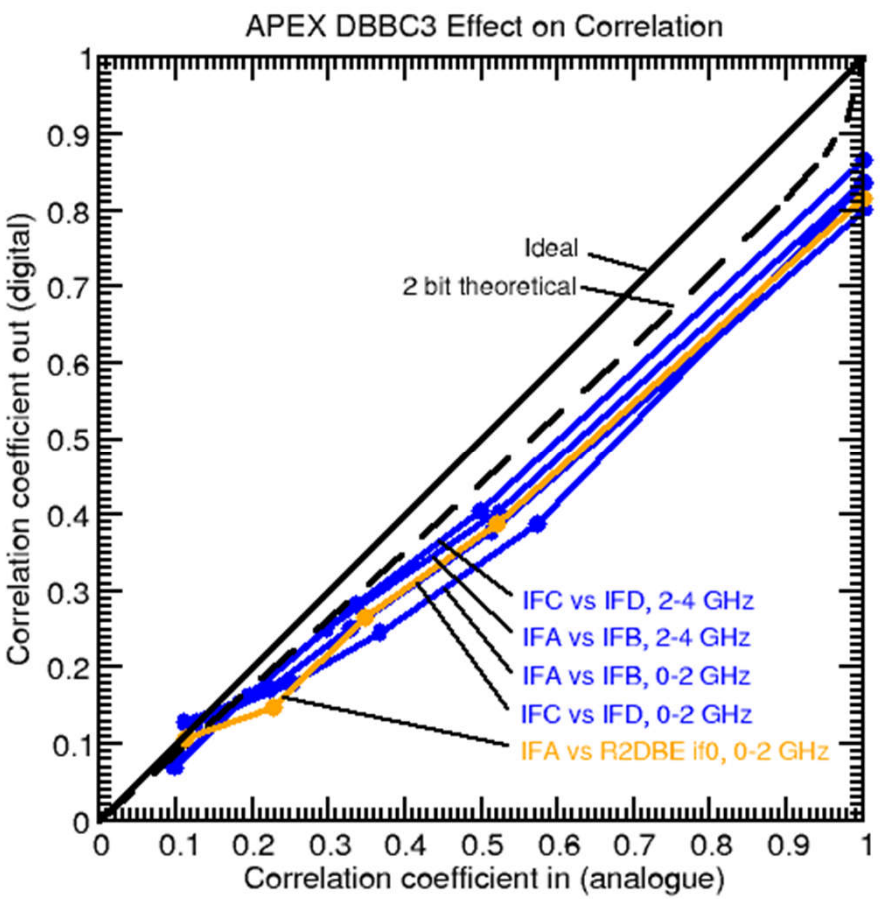
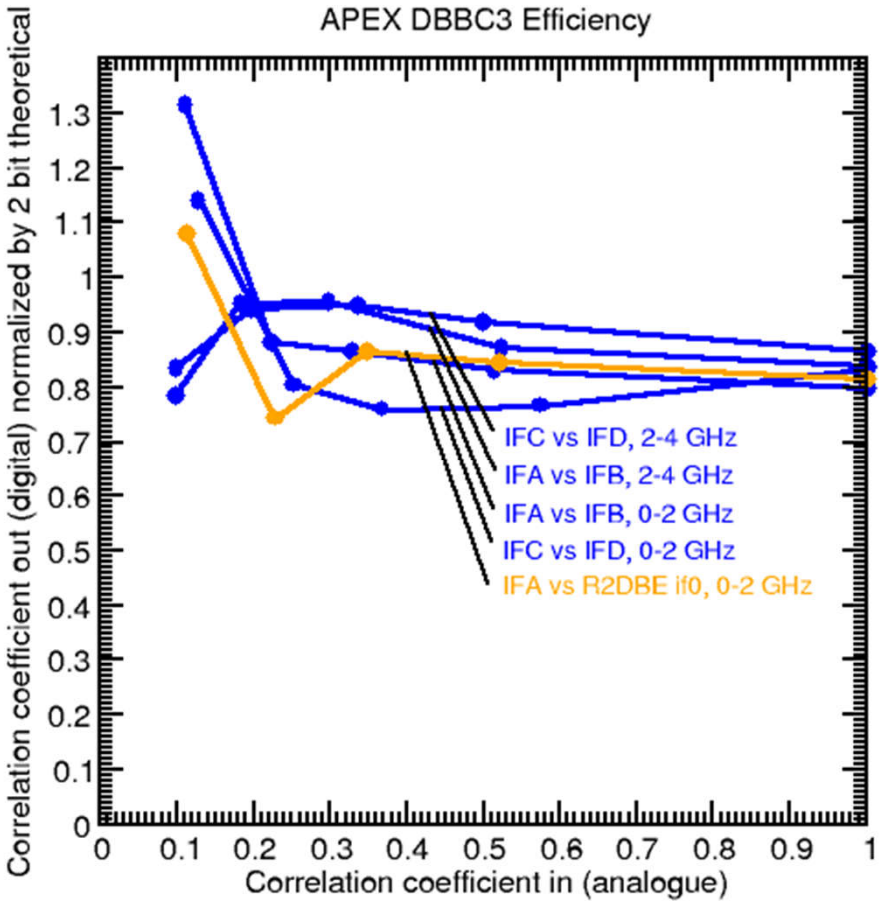
Zero Baseline Test: zerocorr analysis example for $\rho_0 = 0.336$





Efficiency of each backend: 90 % to 93 %

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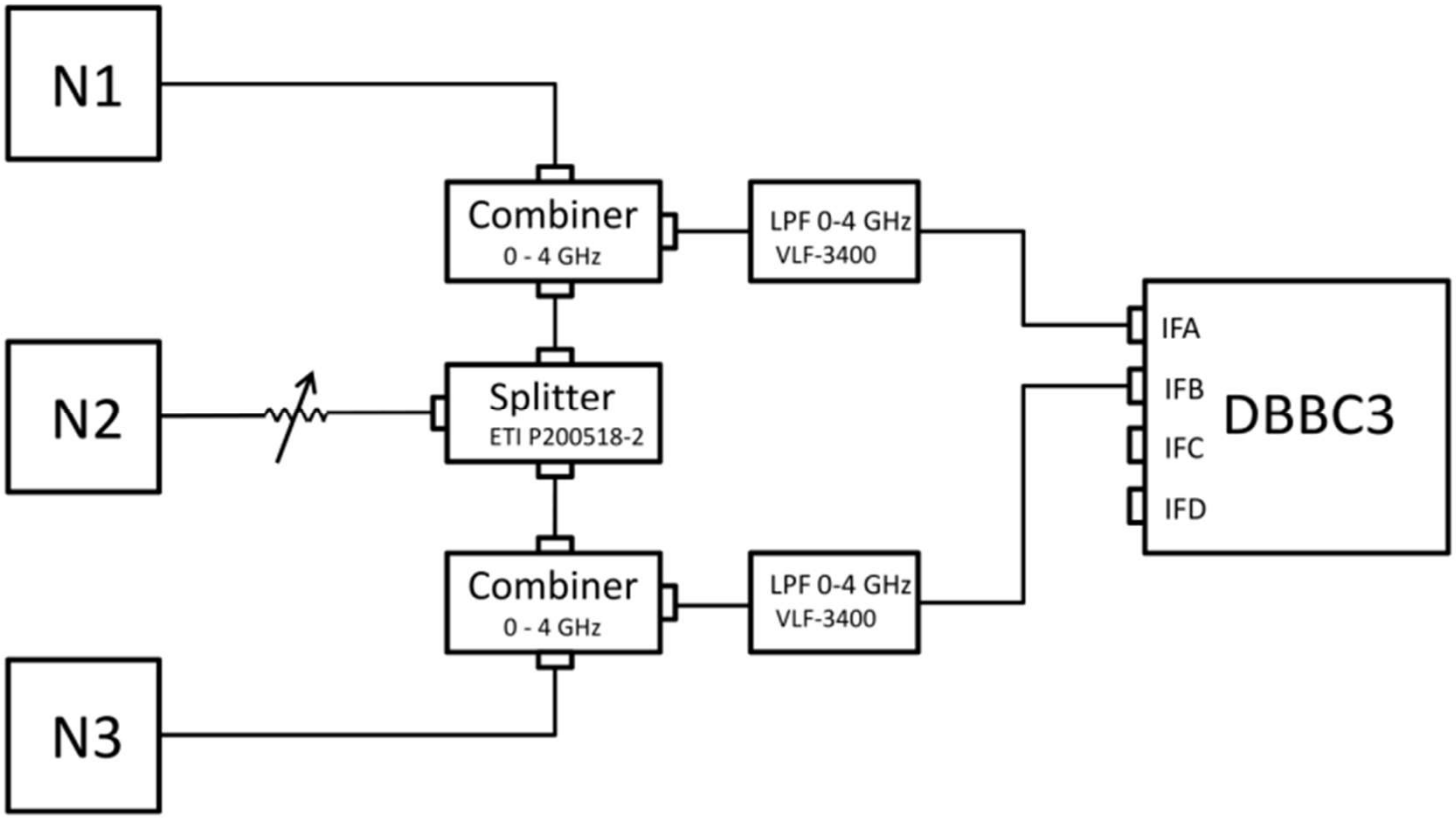
Analogue Signal Preparation: 2018 Aug-Sep



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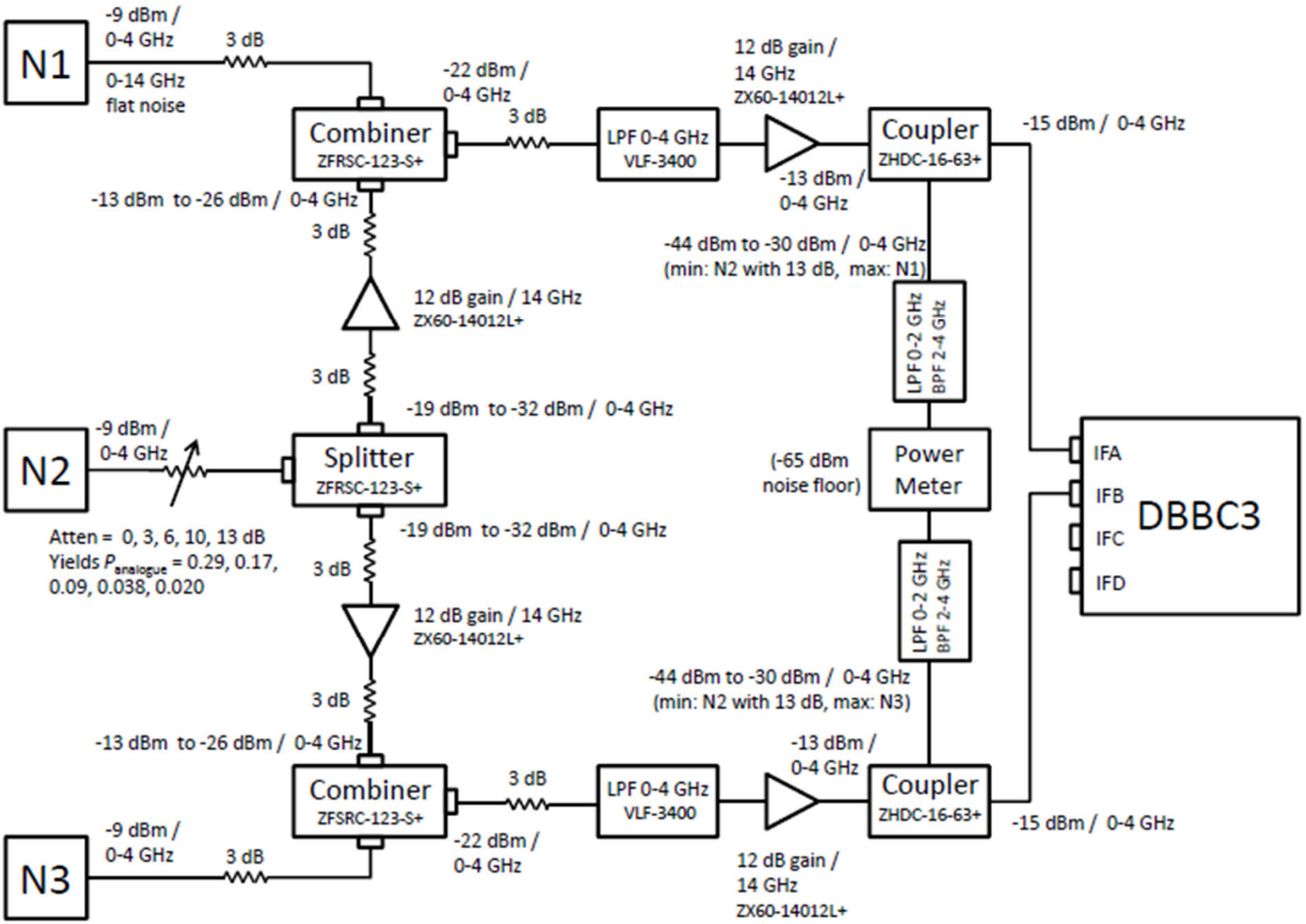
Analogue Signal Preparation: 2018 Oct-Nov



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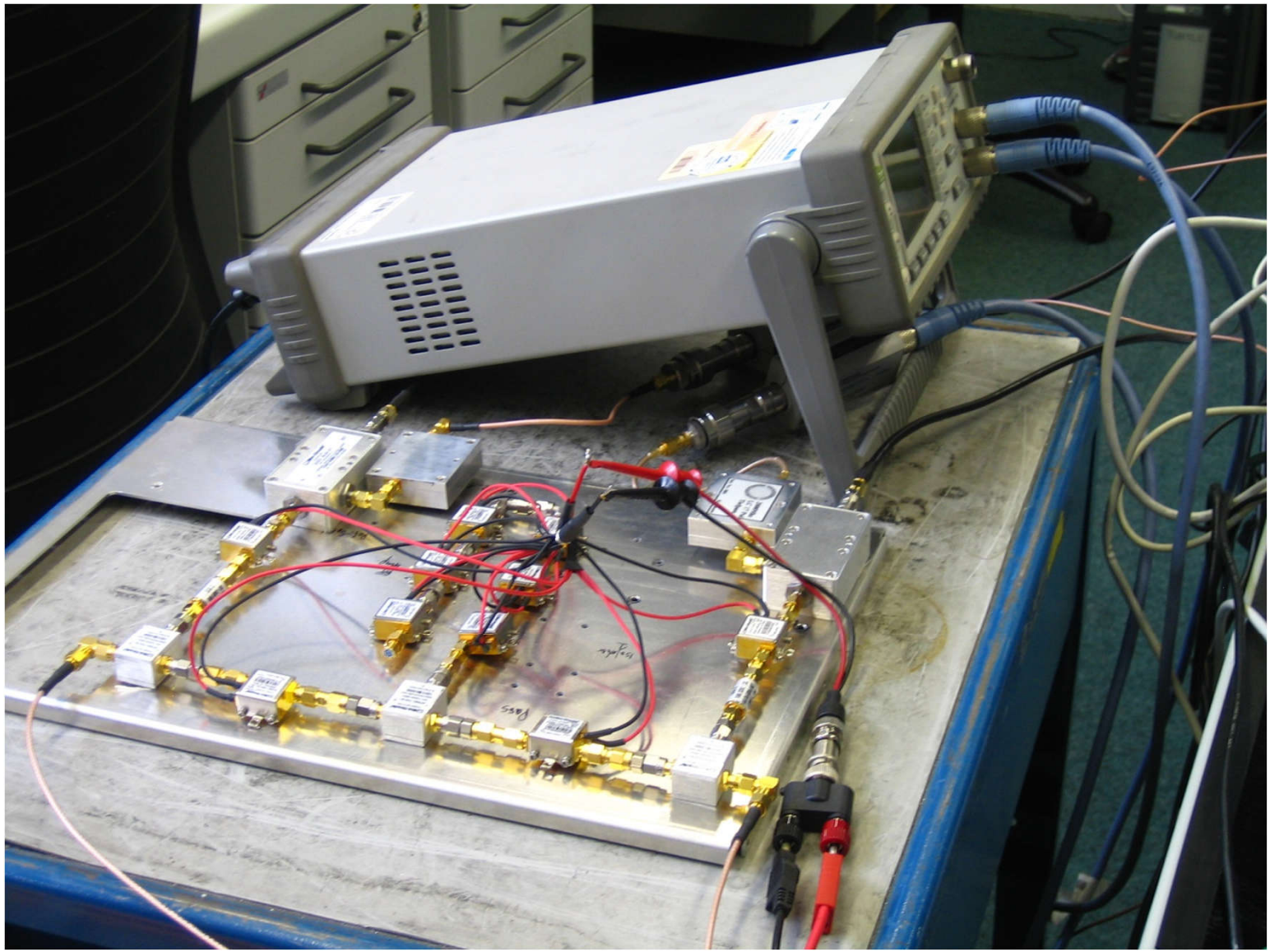
Analogue Signal Preparation: 2018 Oct-Nov



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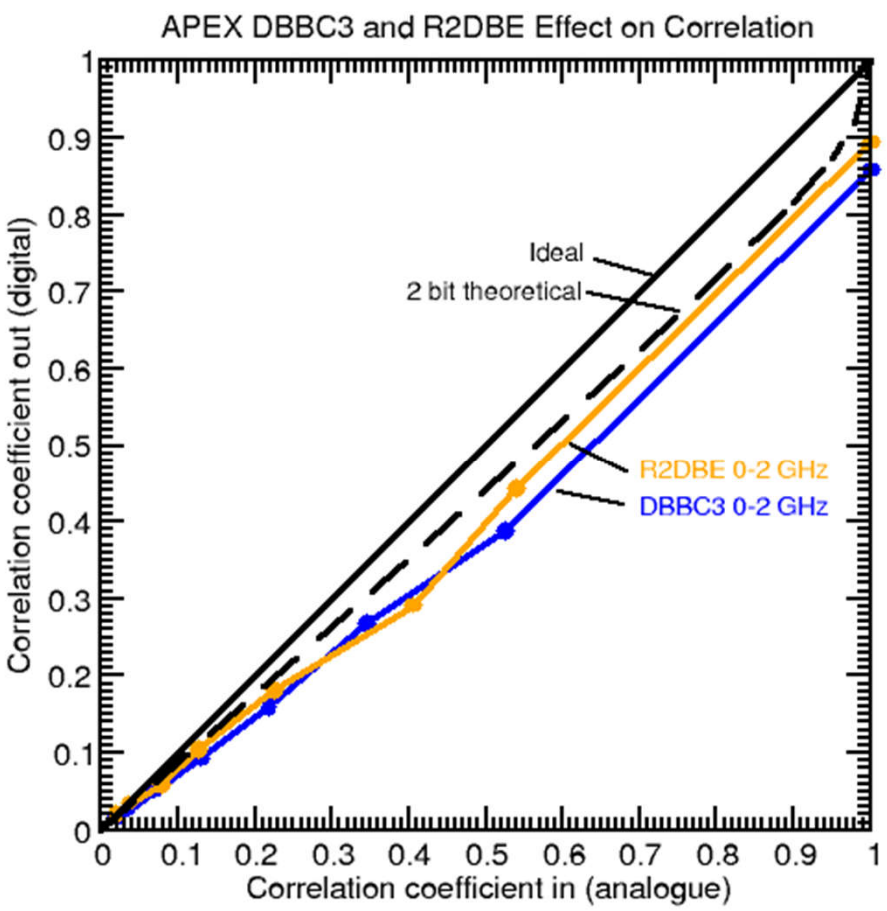
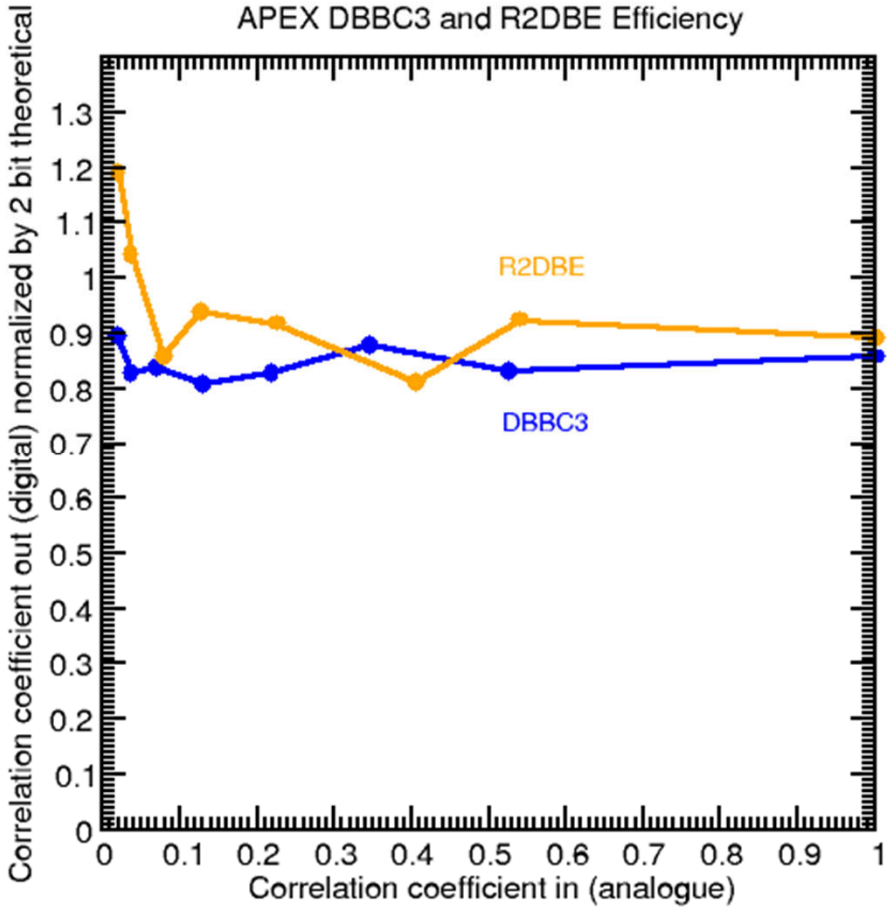
Zero Baseline Test





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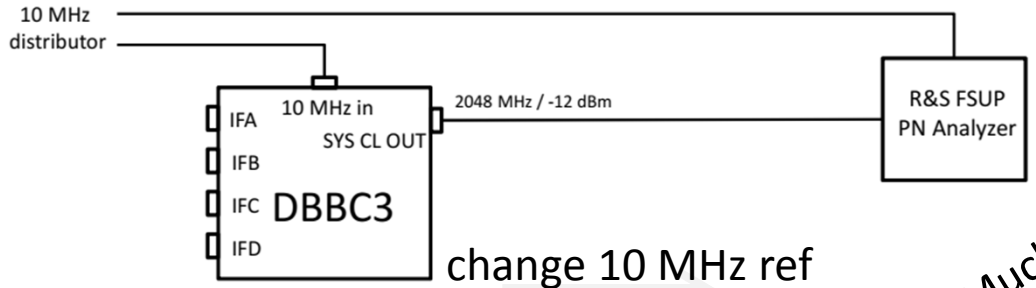
ORA#27 Timing Stability: Sampler Clock

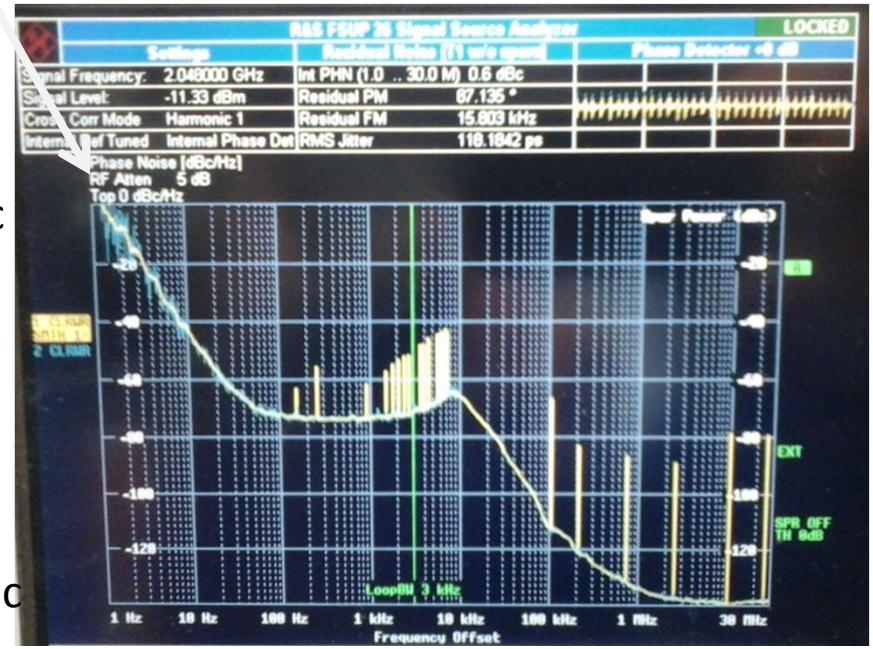


Excess close-in PN

Much less close-in PN

change 10 MHz ref

2048 MHz Clock using Lab 10 MHz Ref



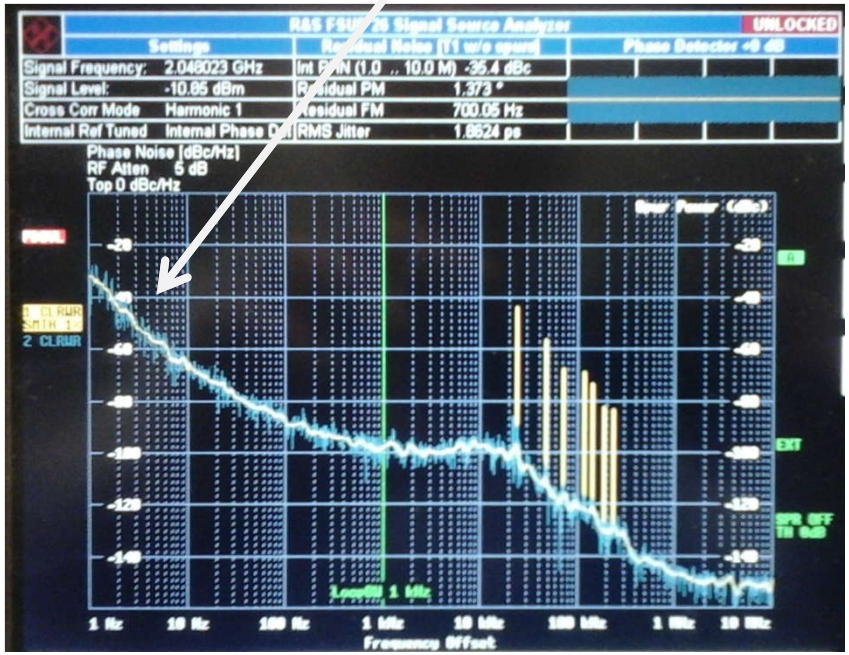
0 dBc

-140 dBc

1 Hz 30 MHz

87° RMS random phase jitter(!!!)

2048 MHz Clock using Wiltron 10 MHz Ref



1 Hz 30 MHz

1.9° RMS random phase jitter

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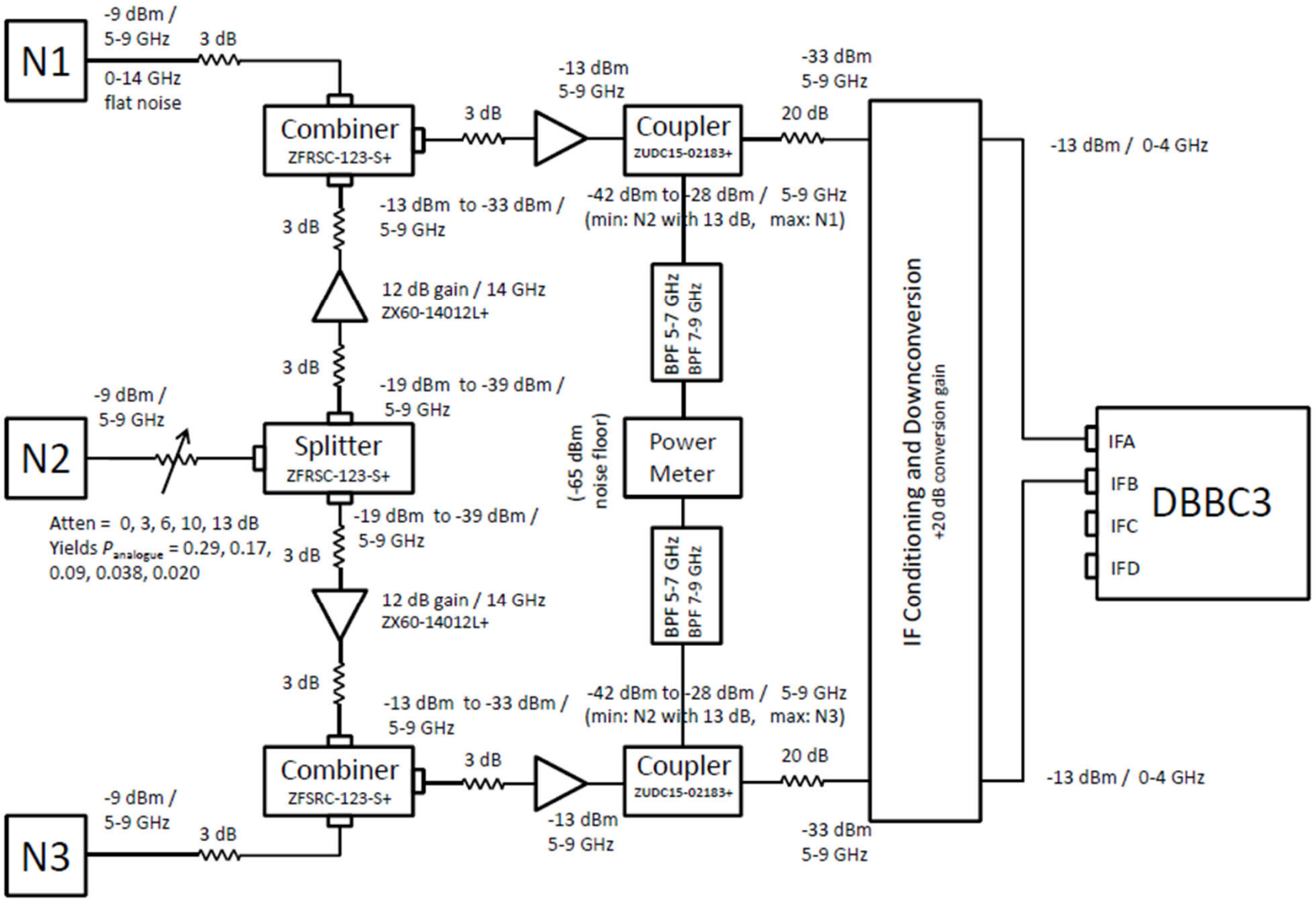
Analogue Signal Preparation: 2018 Oct-Nov



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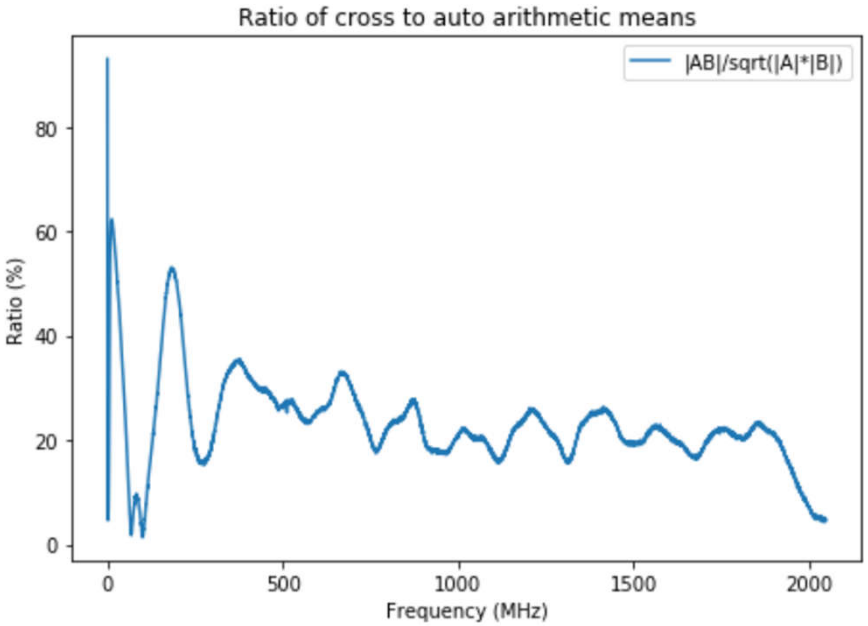
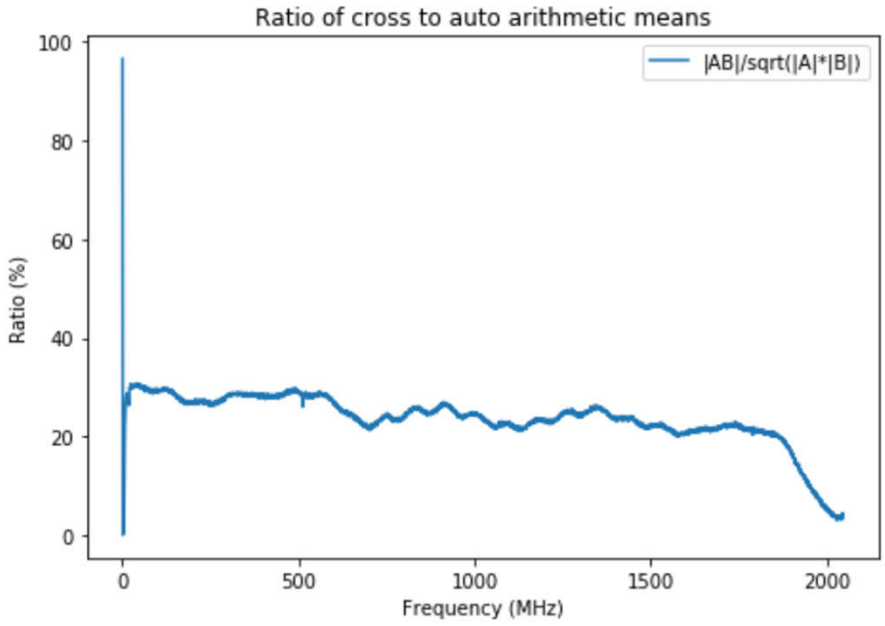
ORA#(35) Bandpass Ripple

- Improved component selection in analogue combiner



2018 Sep



2018 Nov 05

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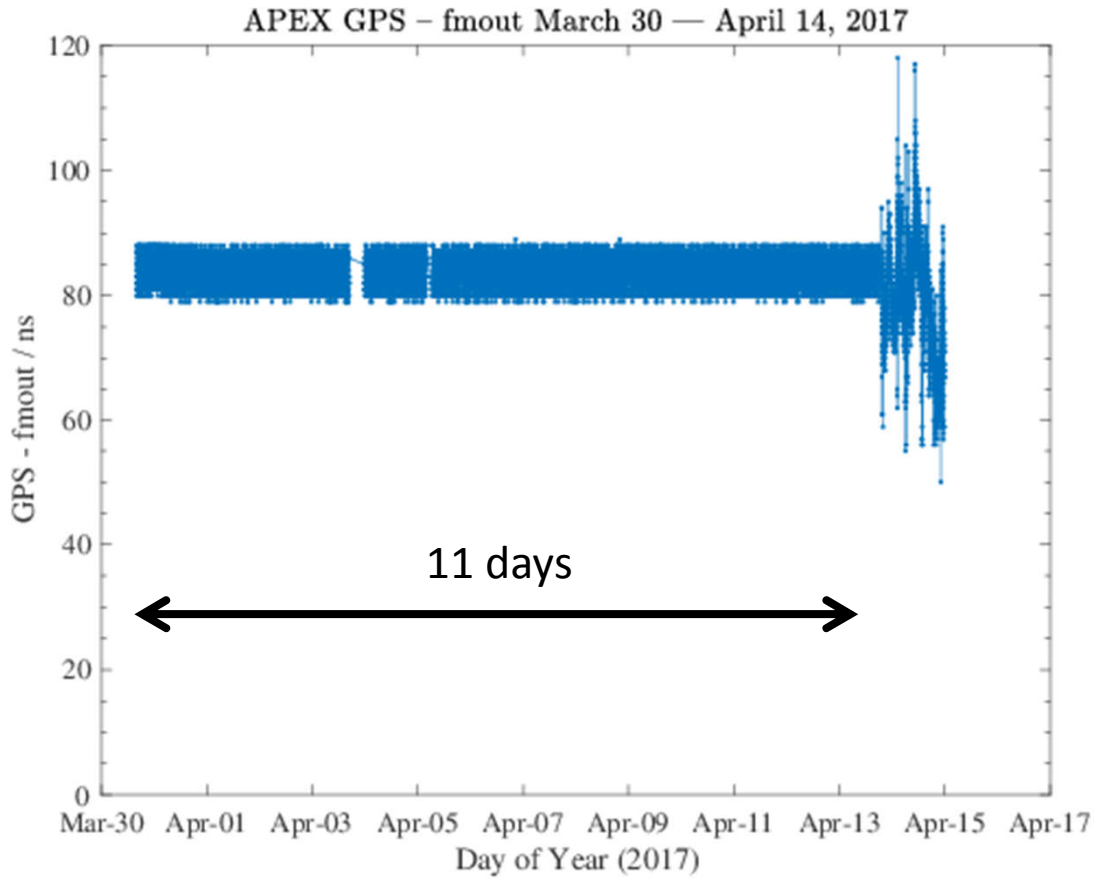
ORA#1 Too-Stable 1 PPS GPS-FMOUT



- Cause: firmware performs re-sync each second on 1 PPS input
- Fix: 2-line change in firmware, recompilation not stable (Xilinx ISE issue; need PlanAhead)

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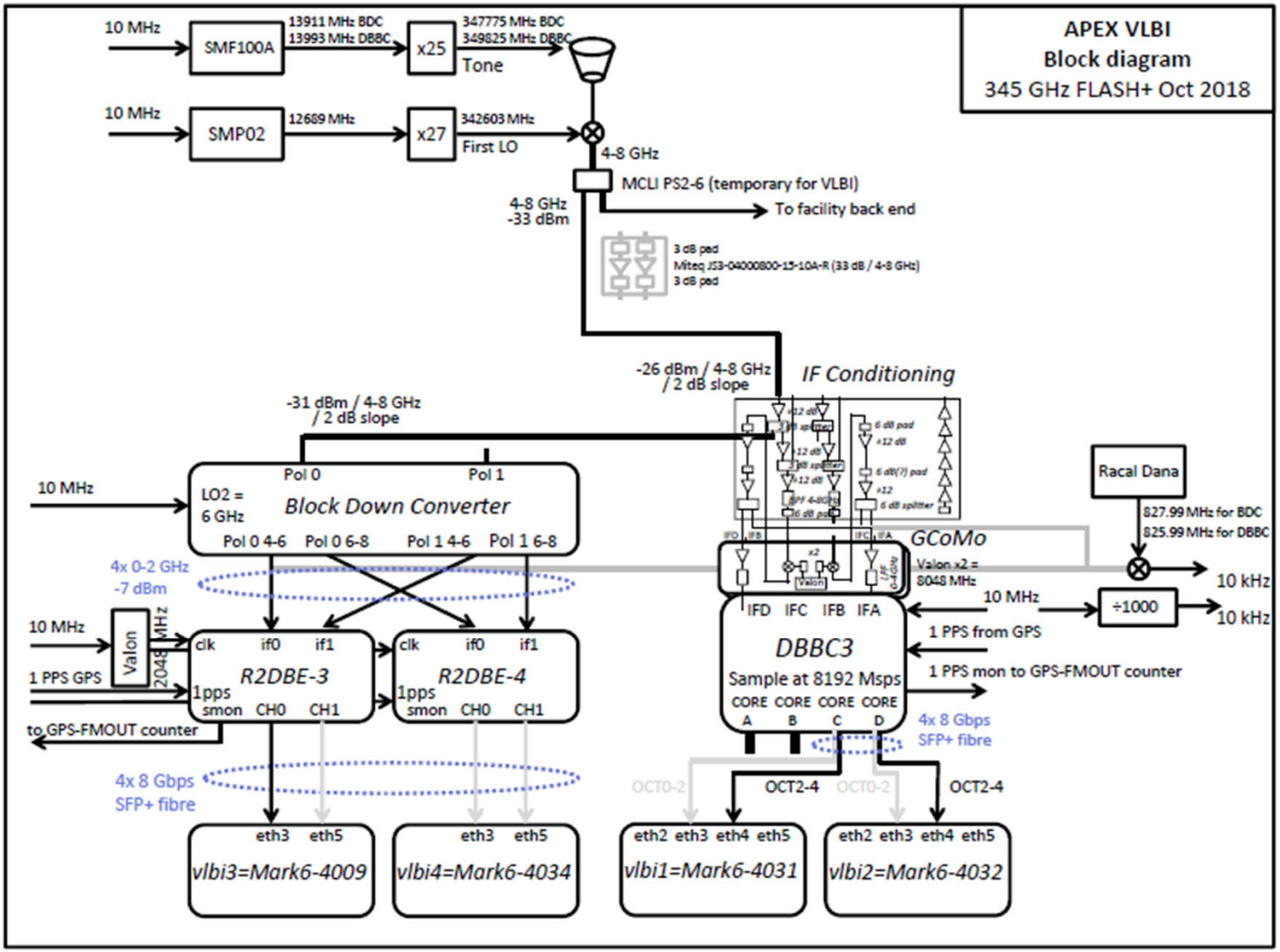
On-Sky Fringe Test EHT Oct 345 GHz

Parallel DBBC + R2DBE



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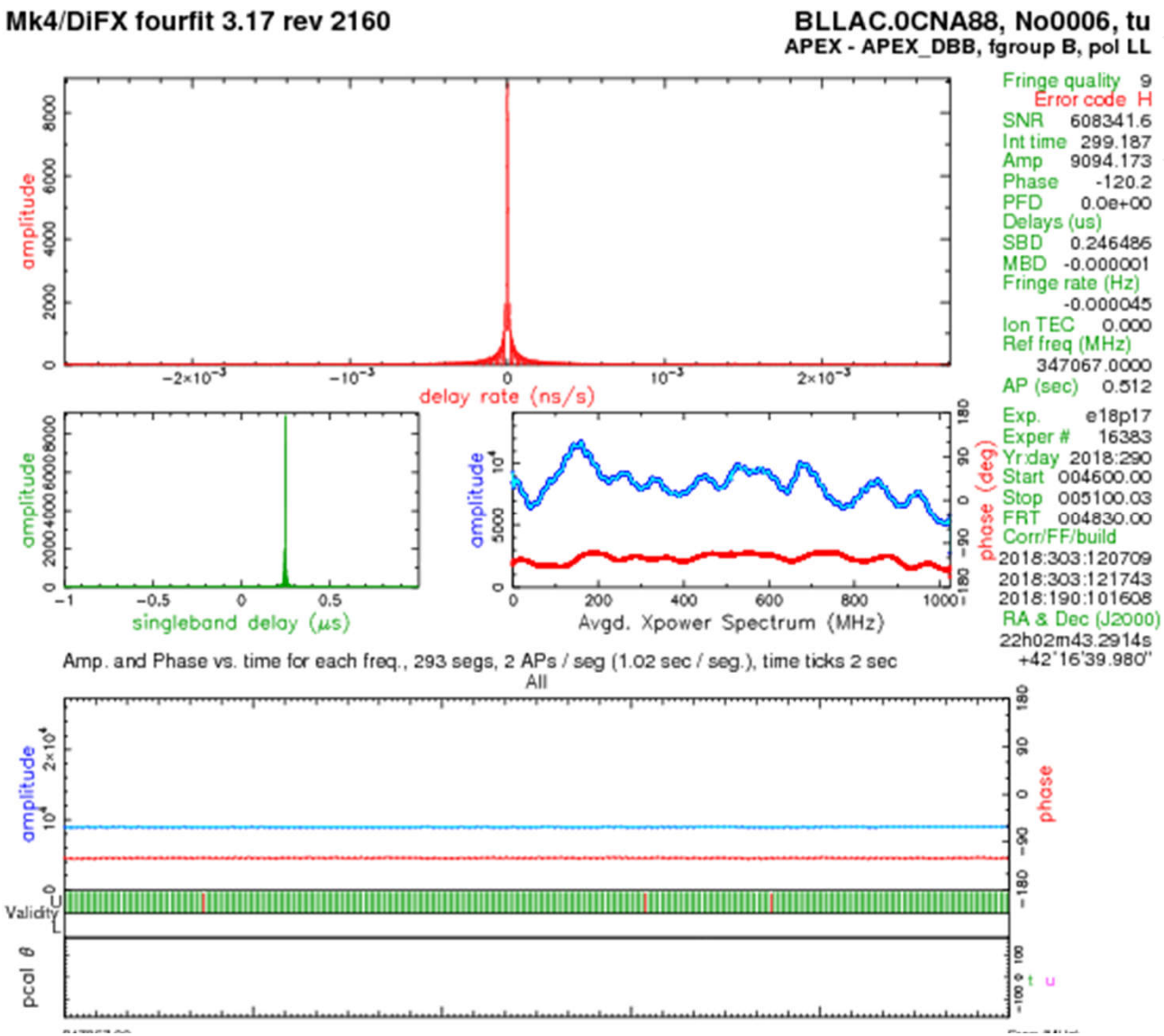
On-Sky Fringe Test EHT Oct 345 GHz



R2DBE – DBBC3 zero-baseline

Amp = 9094 whitneys = 90.94 %

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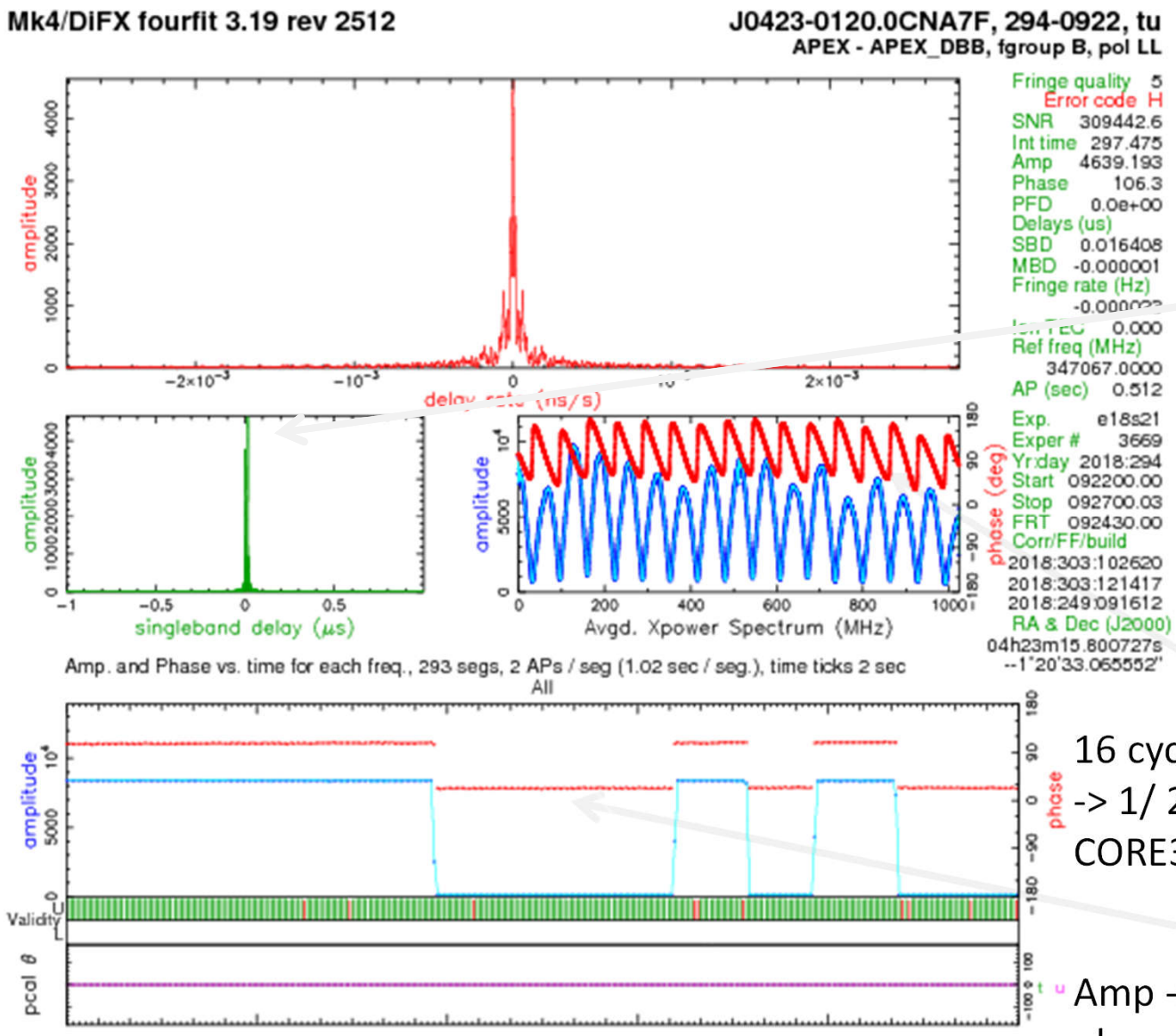
On-Sky Fringe Test EHT Oct 345 GHz



R2DBE – DBBC3 zero-baseline

SBD twin peaks

16 cycles beating at 4096 MSps
-> 1/ 256 MHz delay slip
CORE3 clock = 256 MHz

Amp -> zero intermittently, phase jump

Cause: Re-syncing on 1 PPS, firmware fixed, not yet stable