DBBC3 status and deployment

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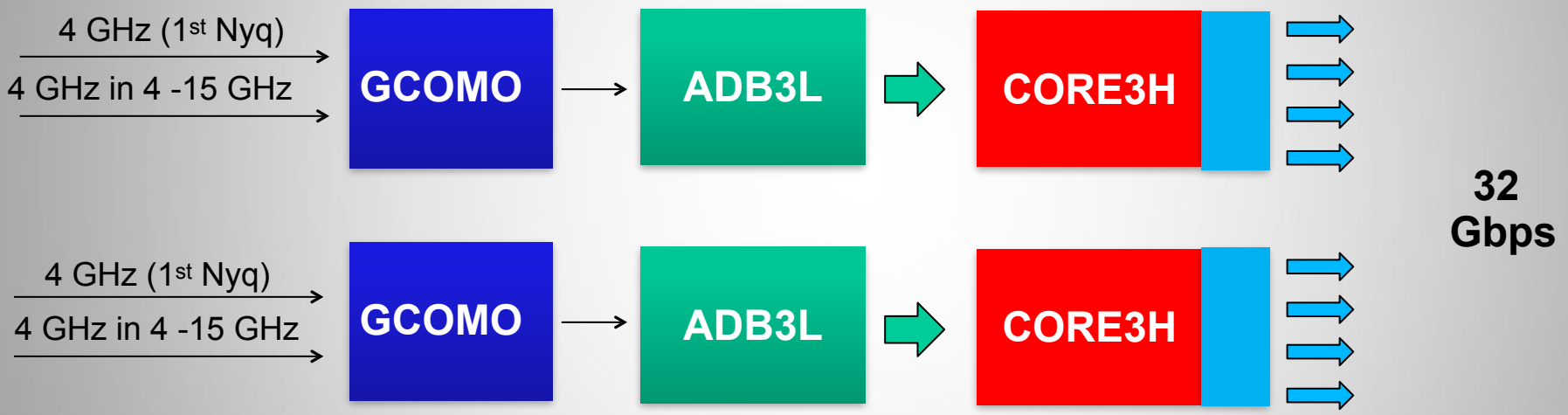
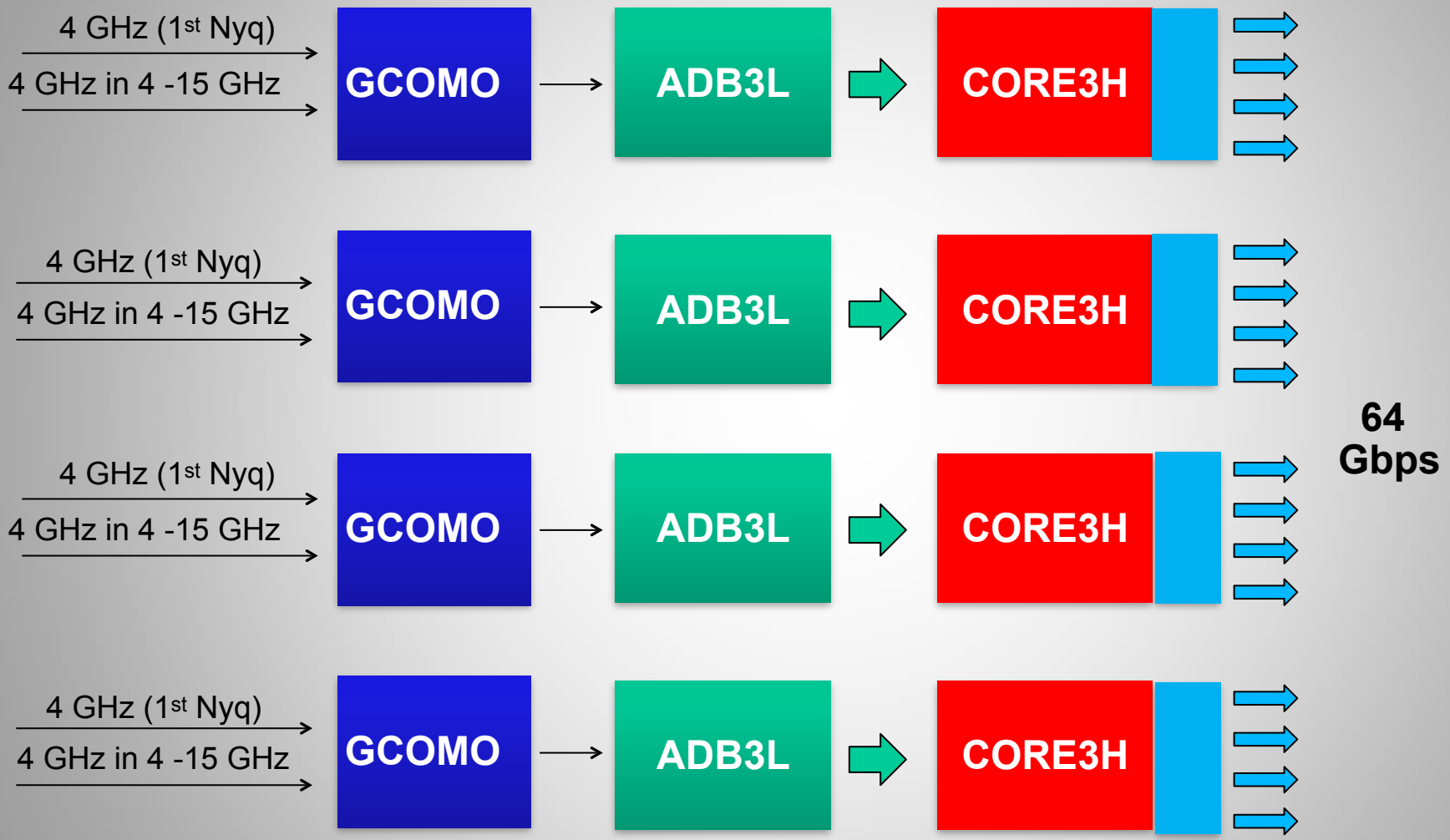
DBBC 3
EUROPEAN
NETWORK
HAT Lab

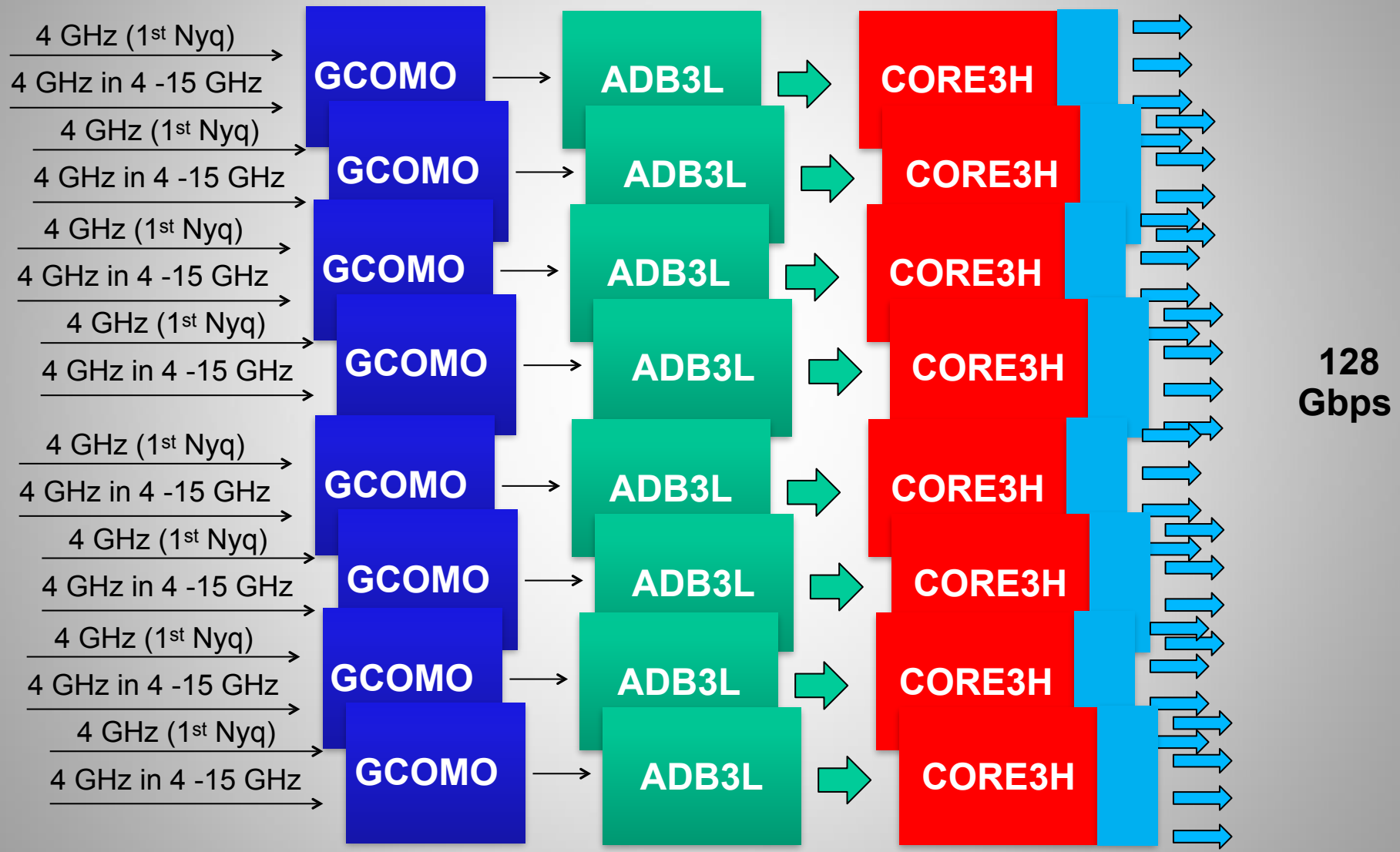
DBBC3L-2L2H Architecture



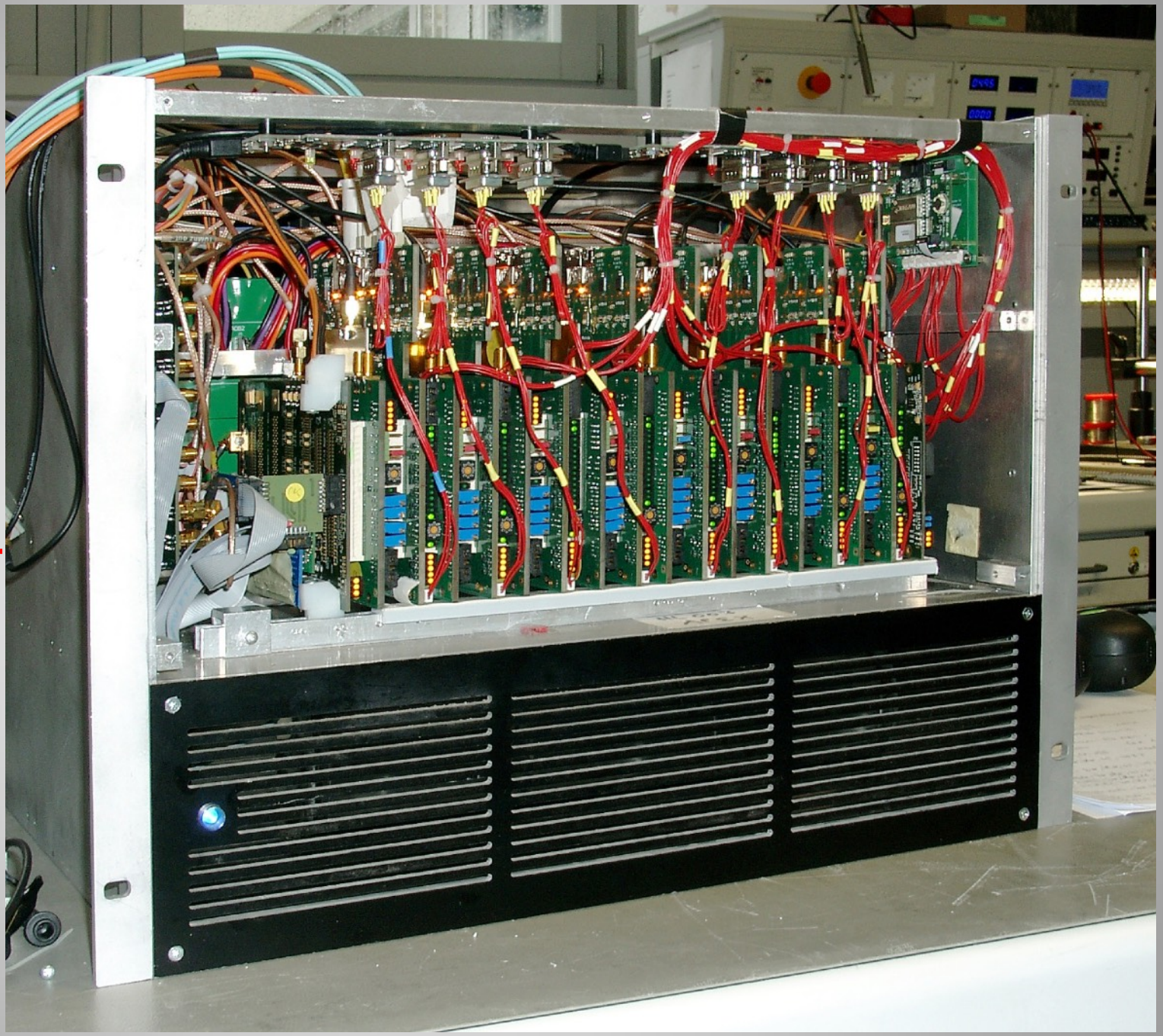
DBBC3L-4L4H Architecture



DBBC3L-8L8H Architecture

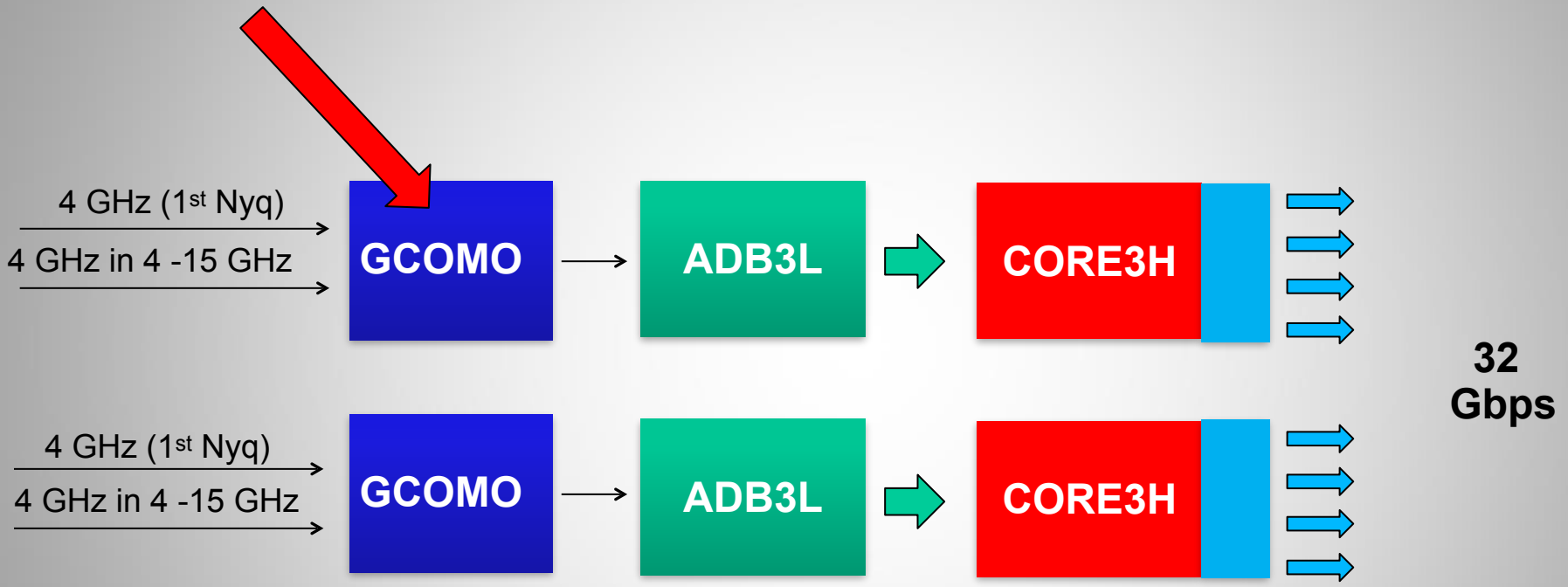


VGOS
DBBC3L-8L8H

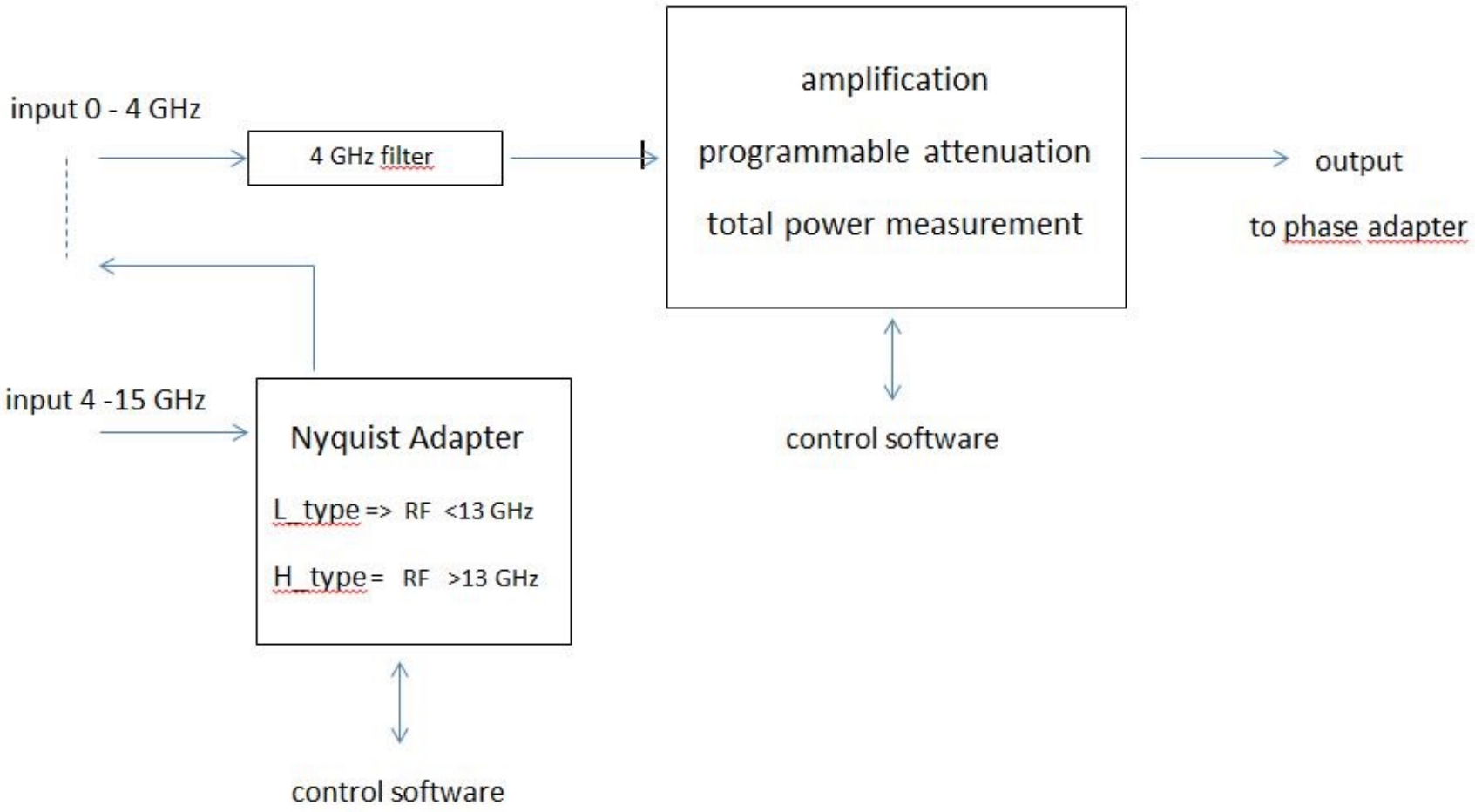


GCoMo

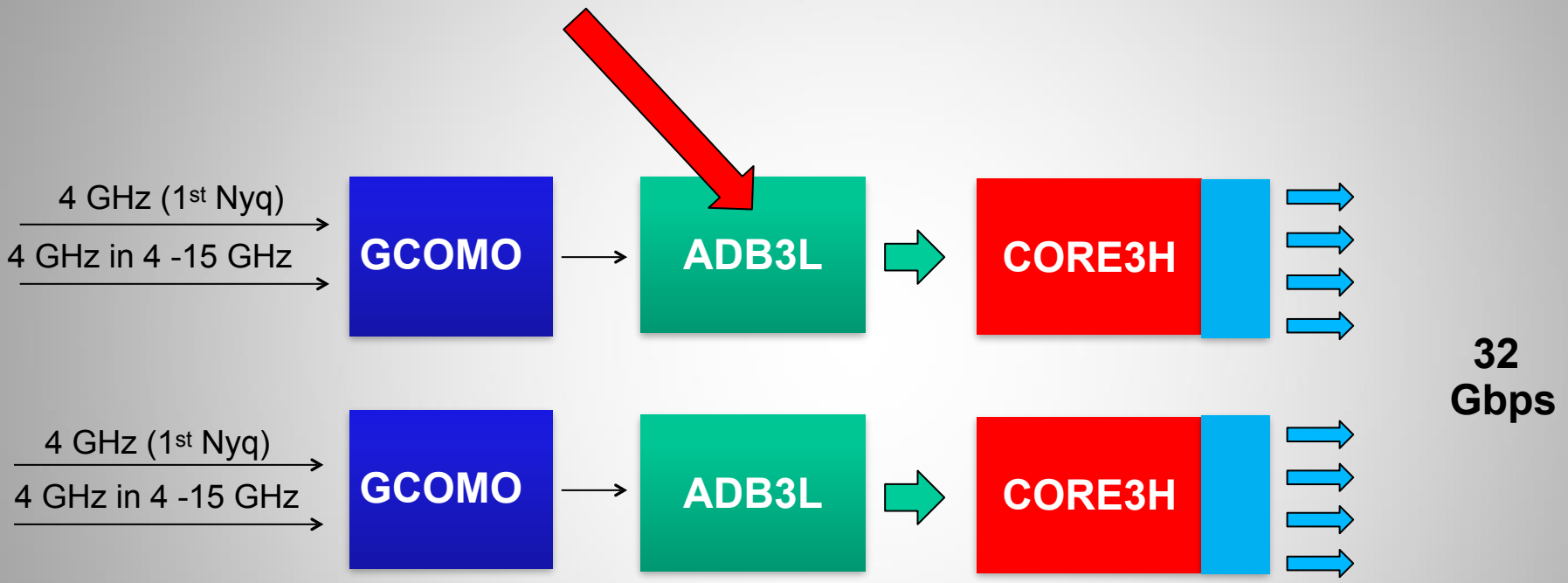
DBBC3L-2L2H Architecture



GCoMo std. (4GHz)

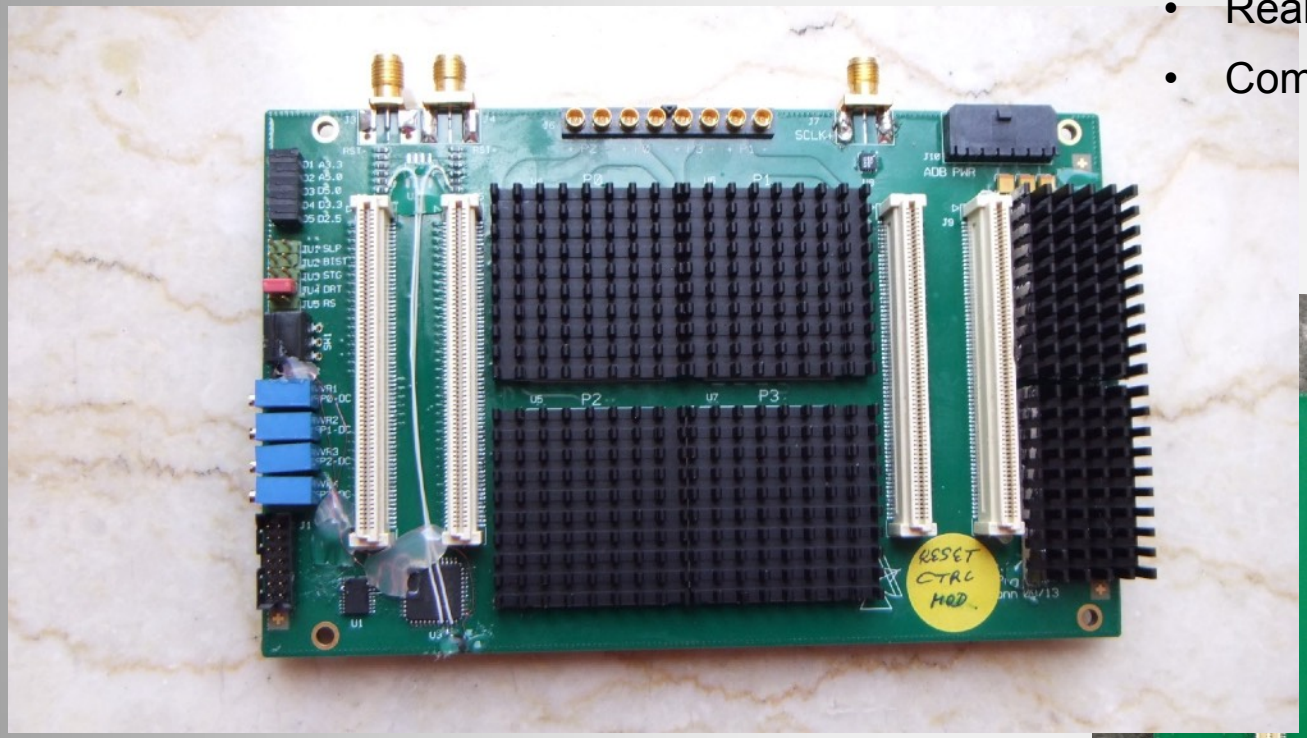


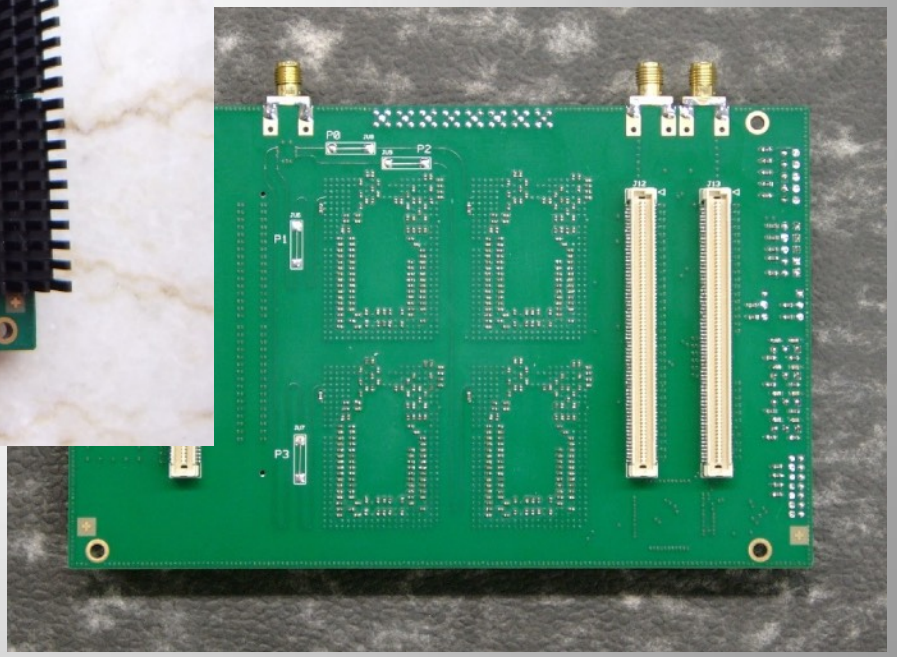
DBBC3L-2L2H Architecture



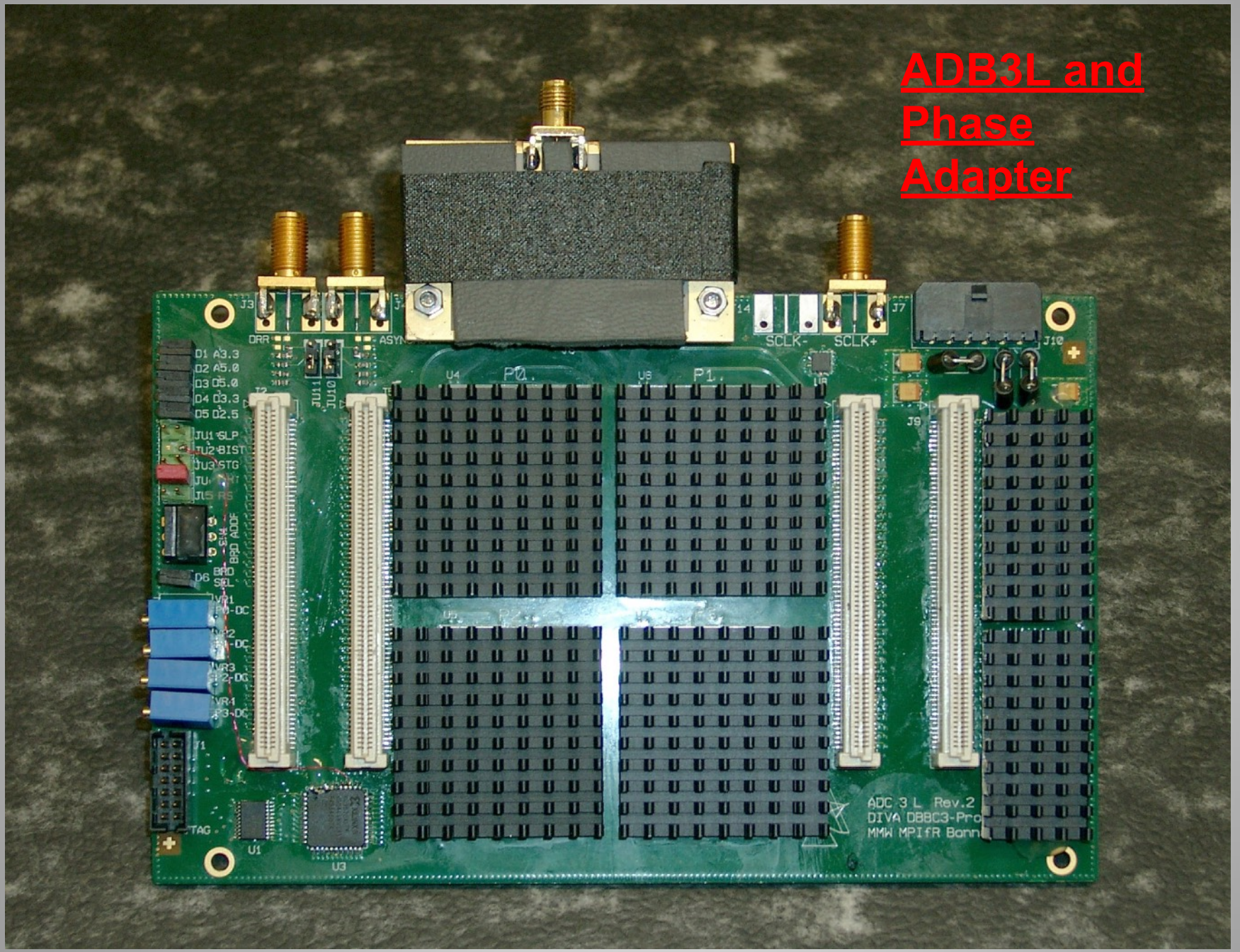
ADB3L

- Number of IFs: **1 - 4**
- Equivalent Sample Rate IF: **8 GSps**
- Instantaneous bandwidth: **4 GHz**
- Sampling representation: **10 bit**
- Real/Complex Sampling
- Compatibility with existing DBBC

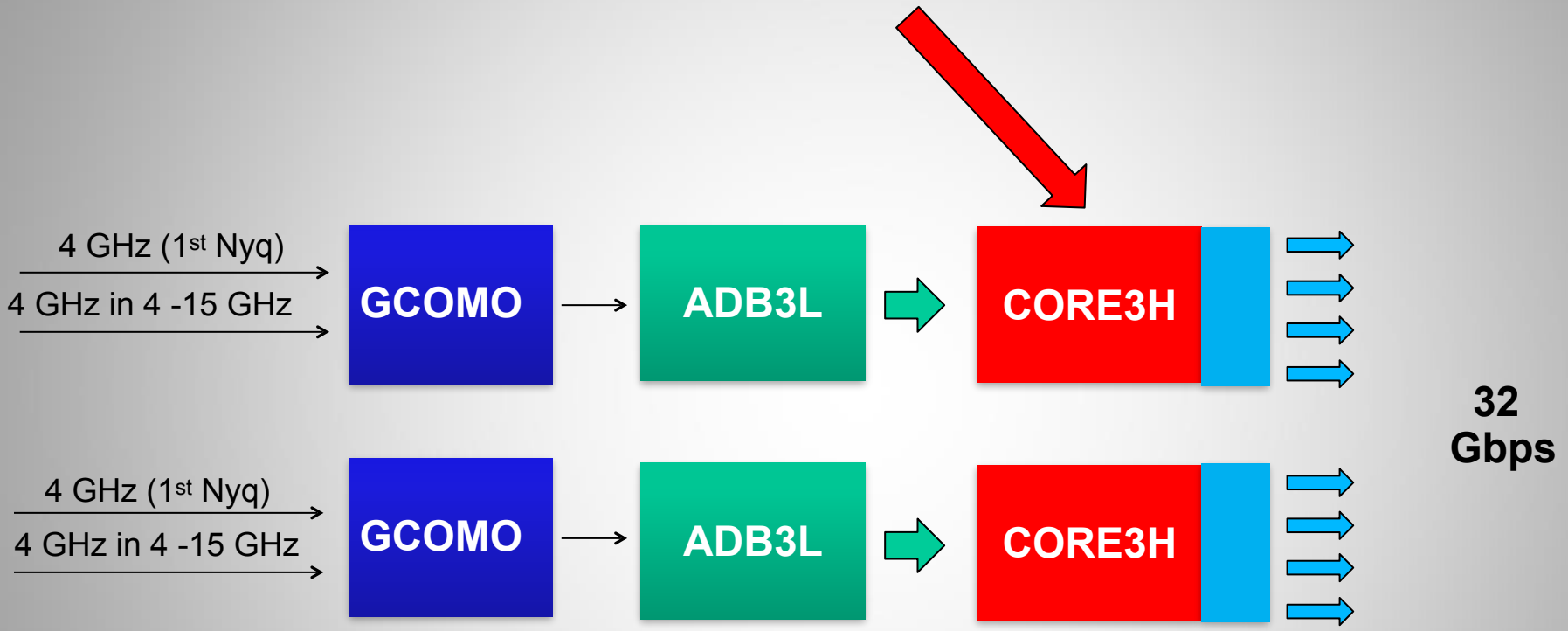




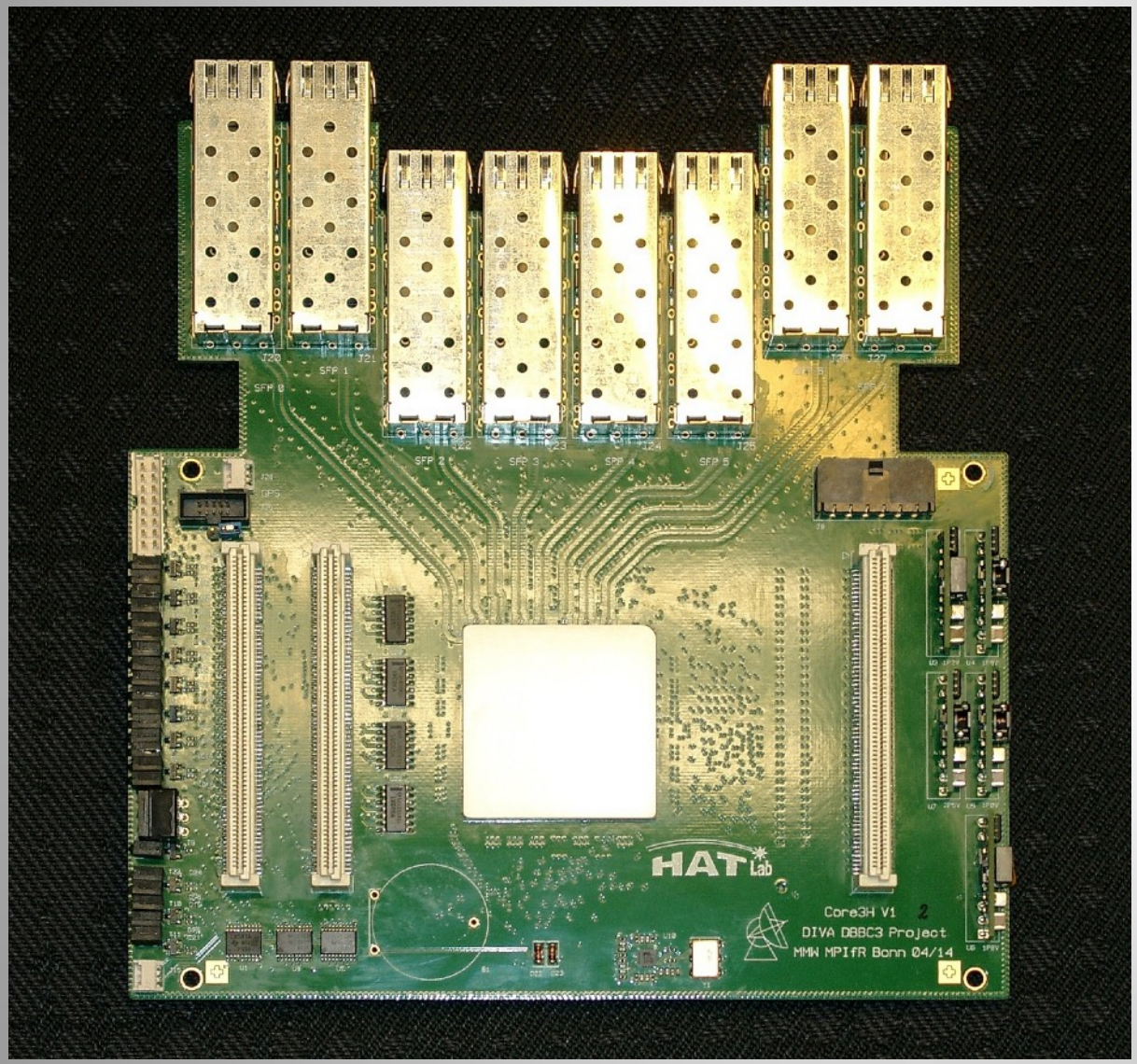
ADB3L and Phase Adapter



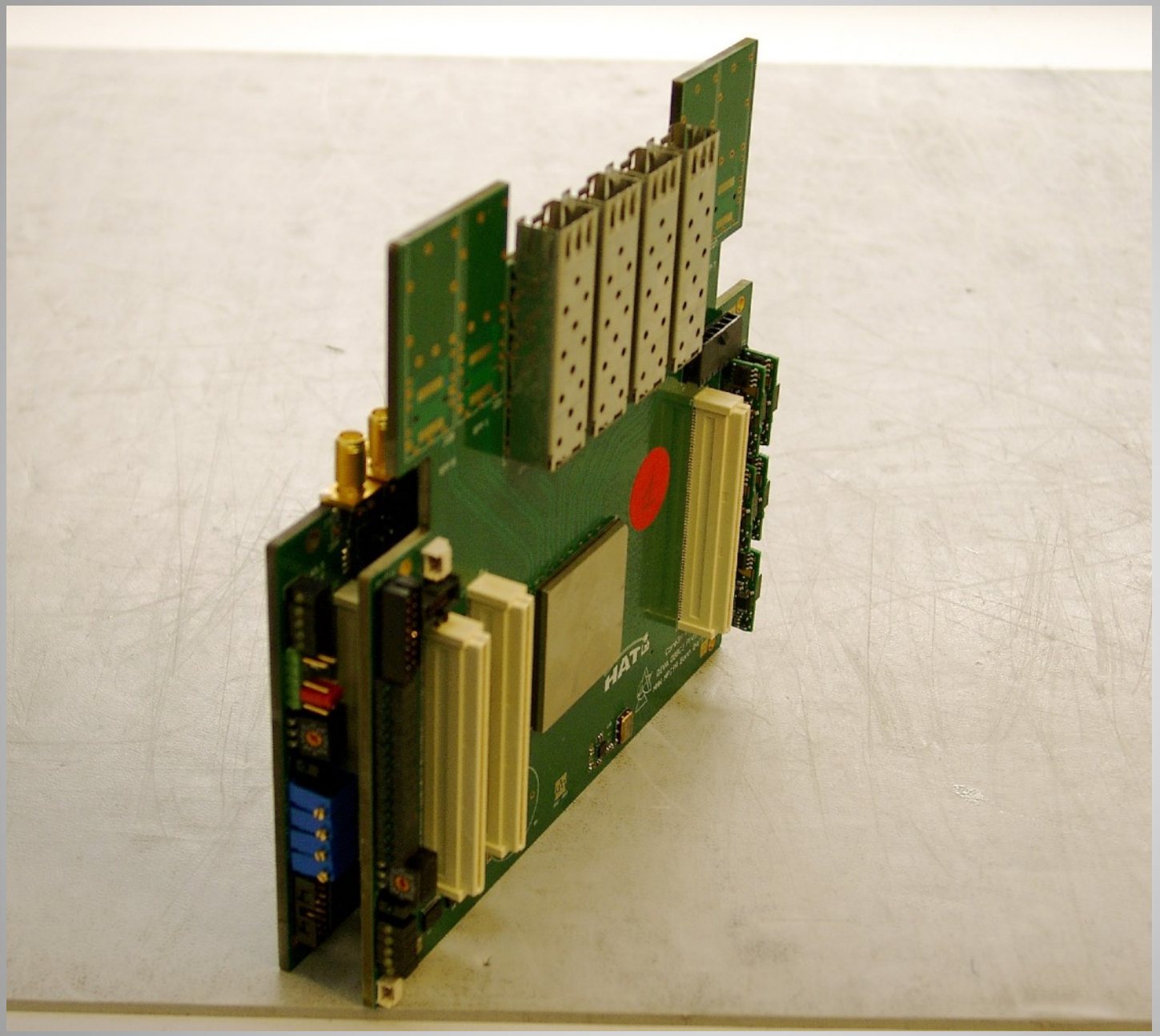
DBBC3L-2L2H Architecture



CORE3H

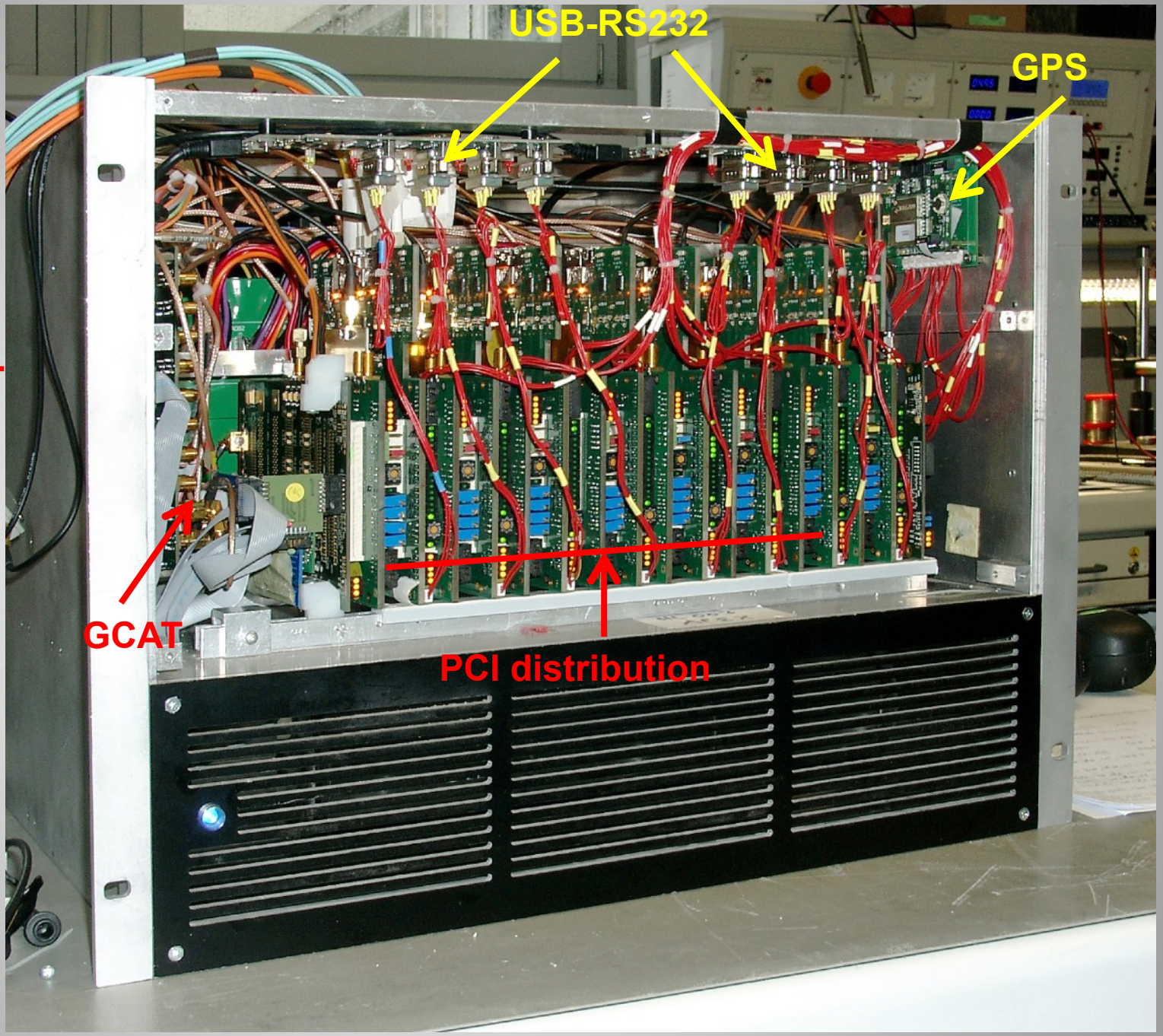


- Input bus: **HSI & HSI2**
- Input sampling representation: **8-10 bit**
- Input bandwidth : **1 x 4GHz,** 2 x 2GHz, 4 x 1GHz
- Processing capability: **DCS, DDC/PFB**
- Max Output: **8 x 10GE SFP+**
- Inter-board bus: **8 Input 10GE SFP+**
- Compatibility with existing DBBC environment



ADB3L + CORE3H

VGOS DBBC3L-8L8H



DBBC3 Calibration

- Necessary for good operations with interleaved sampling without artifacts
- Values for delay, offset and gain need to be determined
- Needs to be done after assembly of DBBC3 or after any hardware modifications

Control-Software and config-Files

- Control software: DBBC3 Control.exe
- Client: DBBC client v4.exe
- 3 types of config-files

– Main config file: dbbc3_config_file_300.txt

– Sampler settings: config_adb3l.txt

– Core3H settings: dsc_core3H_1.fila10g

Main config file: dbbc3_config_file_300.txt

```
config_adb3l.txt
3 dscv3_100217.bit dsc_core3H_1.fila10g COM12
3 dscv3_100217.bit dsc_core3H_2.fila10g COM13
30 dscv3_100217.bit dsc_core3H_3.fila10g COM14
30 dscv3_100217.bit dsc_core3H_4.fila10g COM15
0 dscv3_100217.bit dsc_core3H_5.fila10g COM8
0 dscv3_100217.bit dsc_core3H_6.fila10g COM9
0 dscv3_100217.bit dsc_core3H_7.fila10g COM10
0 dscv3_100217.bit dsc_core3H_8.fila10g COM11
3 4096 5 34000 COM3
3 4096 5 34000
3 4096 5 34000 COM4
3 4096 5 34000
0 34000
0 34000
0 34000
0 34000
GCAT 2048 10 COM5
```

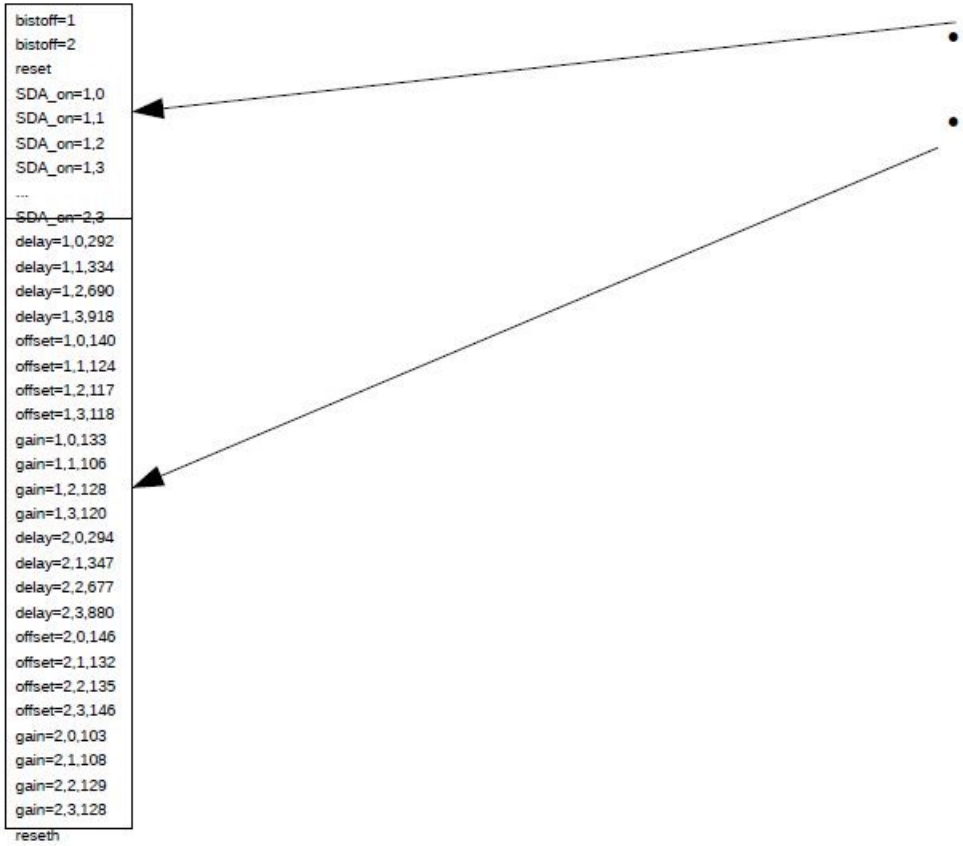
- Config-file for sampler settings
- Configuration for Core3H-Boards
  - 3 dscv3_100217.bit dsc_core3H_1.fila10g COM12
    - 3 – Board present and signal connected
    - 30 – Board present but no signal connected
    - 0 – No Board present
  - 3 dscv3_100217.bit dsc_core3H_1.fila10g COM12
    - Firmware for Core3H
  - 3 dscv3_100217.bit dsc_core3H_1.fila10g COM12
    - Config-File for this Core3H
  - 3 dscv3_100217.bit dsc_core3H_1.fila10g COM12
    - COM-Port for serial communication

Main config-file: dbbc3_config_file_300.txt

```
config_adb3l.txt
3 dscv3_100217.bit dsc_core3H_1.fila10g COM12
3 dscv3_100217.bit dsc_core3H_2.fila10g COM13
30 dscv3_100217.bit dsc_core3H_3.fila10g COM14
30 dscv3_100217.bit dsc_core3H_4.fila10g COM15
0 dscv3_100217.bit dsc_core3H_5.fila10g COM8
0 dscv3_100217.bit dsc_core3H_6.fila10g COM9
0 dscv3_100217.bit dsc_core3H_7.fila10g COM10
0 dscv3_100217.bit dsc_core3H_8.fila10g COM11
3 4096 5 34000 COM3
3 4096 5 34000
3 4096 5 34000 COM4
3 4096 5 34000
0 34000
0 34000
0 34000
0 34000
CAT3 2048
```

- Configuration for Conditioning Modules
  - 3 4096 5 34000 COM3
    - 3 – GCoMo with internal Valon Synthesizer
    - 2 – CoMo without internal synthesizer
    - 0 – No (G)CoMo present
  - 3 4096 5 34000 COM3
    - Valon Frequency (0.5 * LO-Frequency)
  - 3 4096 5 34000 COM3
    - Attenuation of Valon Frequency in dB
  - 3 4096 5 34000 COM3
    - AGC target value
  - 3 4096 5 34000 COM3
    - COM-Port for serial communication with Valon Synthesizer
- Configuration for Clock Generator

Sampler config-file: config_adb3l.txt



- Static part
- Calibration settings for each sampler
  - Format: command=board,sampler,value
  - Boards 1-8
  - Samplers 0-3
  - Valuerange depends on command:
    - Delay: 0-1023
    - Offset: 0-255
    - Gain: 0-255

Core3H config-file: dsc_core3H_1.fila10g

```
core3_init
core3_mode independent
regwrite core3 0 20
regwrite core3 1 0xBFBFBFBF
regwrite core3 2 20
regwrite core3 3 20
regwrite core3 9 1
reboot
inputselect vsi1-2-3-4-5-6-7-8
vsi_samplerate 64000000
splitmode on
reset
vdif_frame 2 1 8192 ct=off
tengbcfg eth0 ip=192.168.1.30 gateway=192.168.1.1 nm=27
tengbcfg eth1 ip=192.168.1.31 gateway=192.168.1.1 nm=27
tengbcfg eth2 ip=192.168.1.28 gateway=192.168.1.1 nm=27
tengbcfg eth3 ip=192.168.1.29 gateway=192.168.1.1 nm=27
tengbarp eth0 2 00:60:dd:44:0b:7a
tengbarp eth1 3 00:60:dd:44:0b:7b
tengbarp eth2 4 00:60:dd:44:0b:8a
tengbarp eth3 5 00:60:dd:44:0b:8b
destination 0 192.168.1.2
destination 1 192.168.1.3
destination 2 192.168.1.4
destination 3 192.168.1.5
timesync
start vdif
sysstat
```

- Command-set similar to FiLa10G, one file per Core3H:
- Vdif-settings
- Ethernet configuration

Calibrate offset

- Select high attenuation for IF to get a low power noise.
  - Power values between 1000 and 8000 are ok.
  - f.e.: dbbcifa=2,60
- Issue offset-calibration with command: cal_offset=1
  - The parameter is the board number
- After calibration the correct offset-values are set and should be copied in the ADB3L config-file

Calibrate gain

- Select an attenuation value for IF that is close to realistic values
  - 34000 is a good value
  - Command: dbbcifa=2,agc,1,34000
    - Wait until target is reached and then set agc off: dbbcifa=2,man
- Issue calibration with command cal_gain=1
  - Parameter is board number
- After calibration the correct gain-values are set and should be copied in the ADB3L config-file

Calibrate delay

- Should be done after offset and gain calibration
- Set CoMo settings identical to gain calibration, not necessary if directly calibrated after gain.
- Issue delay calibration with command cal_delay=1
  - The parameter is the board number
- After calibration the correct gain-values are set and should be copied in the ADB3L config-file

DBBC3 Firmware:

Different packages for the modes (.bit, .exe, .txt, .doc)

DSC: 0- 4 GHz —-> operational

OCT1: 0-2, 2-4 GHz —-> operational

0-1, 1-2, 2-3, 3-4 GHz —-> operational

0.5-1.0, 1.0-1.5, ……, 3.5-4.0 GHz —-> operational

OCT2: 2 filters as above at the same time per IF —-> operational

DDC-L: 16 bbc (U&L) 2-4-8-16 MHz tunable in 4GHz —-> operational
(legacy) 32 bands tunable PFB 2-4-8-16 MHz block in 4GHz —-> operational

DDC-V: 12 bbc (U&L) full 32MHz tunable in 4GHz —-> operational
(VGOS) 24 bands 32 MHz PFB block tunable in 4GHz —-> operational

16 bbc (U&L) tunable full 32MHz in 4GHz —-> *in progress*
32 bands tunable 32 MHz PFB block in 4GHz —-> *in progress*

DBBC3 New hardware under development:

A new class of samplers to be coupled by optical fibers to the CORE3H

- **ADB3H1: Double polarizations, 0 - 16 GHz, 8-bit**
- **ADB3H2: Double polarizations, 0 - 24 GHz, 8-bit**
- **ADB3H3: Double polarizations, 0 - 28 GHz, 8-bit**

DBBC3 systems delivered and under construction:

APEX, DBBC3-4L4H

PICO VELETA, DBBC3-4L4H

HOBART, DBBC3-6L6H

YEBES, DBBC3-2L2H, GCoMO/CoMo

ONSALA1, DBBC3-8L8H

ONSALA2, DBBC3-8L8H

NyALESUND1, DBBC3-8L8H

NyALESUND2, DBBC3-8L8H

EFFELBERG, DBBC3-2L2H

KOREA (NGII), DBBC3-2L2H

KATHERINE, DBBC3-6L6H

YARRAGDEE, DBBC3-6L6H

WETTZELL, DBBC3-8L8H

SHESHAN, DBBC3-8L8H

METSAHOVI(FGRI), DBBC3-8L8H