Max-Planck-Institut für Radioastronomie

DBBC3 Testing for APEX and Pico Veleta

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Test Procedures

1 Timing Stability

Monitor 1 PPS output from firmware vs 1 PPS input to detect cycle slips
Clock synthesizer stability
Measure system phase stability end-to-end
Verify UTC timestamp in VDIF header
Check for delay jumps in recording

2 Analogue Input Components

IF conditioning module characteristics
Headroom
Mixer LO power requirement for downconversion
Total system bandpass characterization
Noise figure

3 Digital Transmission Integrity and Processing Correctness

Examine state counts of 8 bits from sampler
Examine state counts of 2 bits after thresholding
Examine 1 PPS rise time
Verify total power spectrum clean of artifacts
Verify 8 Gbps correct transmission
Verify OCT-D filter shape
Verify VDIF packet stream correctly formatted, no gaps, in time order, no stream mixing

4 Reliability

Cooling
Sustained recording test for infrequent errors.

5 Zero-Baseline Test

Check analogue correlation coefficient from noise source splitting
DBBC3 – DBBC3 Digital Correlation Coefficient for Partially Correlated Noise
DBBC3 – R2DBE Digital Correlation Coefficient for 100 % Correlated Noise

6 On-Sky Fringe Test

Kashima – Onsala Test

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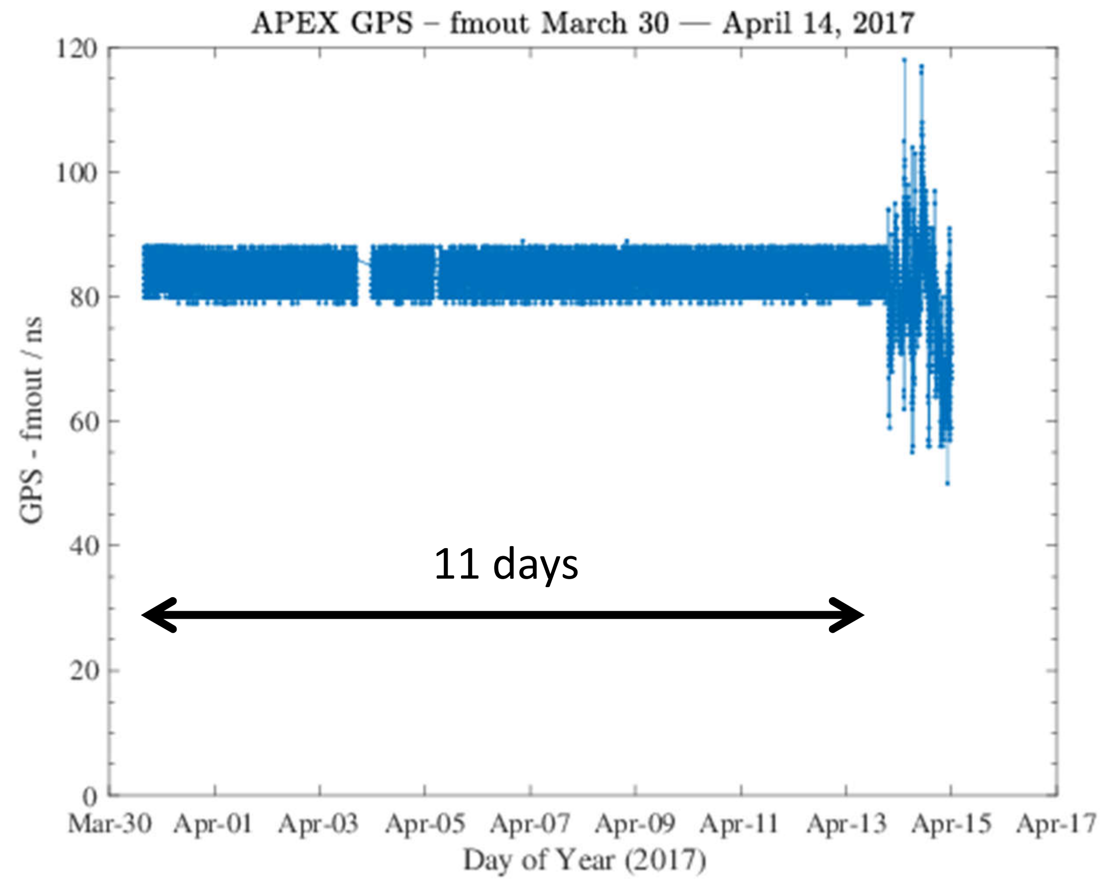
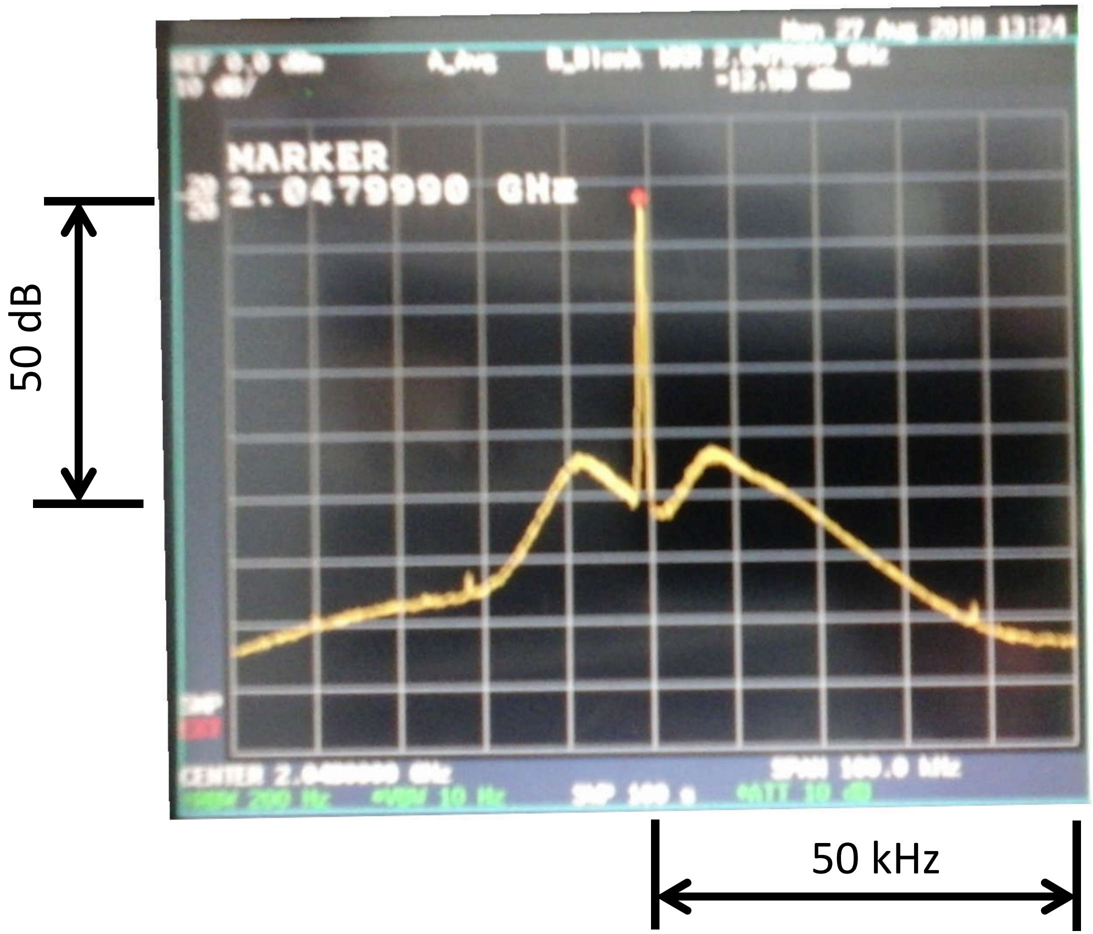
Timing Stability

Monitor 1 PPS Output from Firmware vs 1 PPS Input to Detect Cycle Slips



- GPS-FMOUT for APEX DBBC3 during EHT 2017 run
- No cycle slips over 11 days; a 10 MHz slip would make 100 ns step.
- The counter was recabled to the R2DBE FMOUT on April 13

Timing Stability: Sampler Clock on Spectrum Analyzer



- SSB phase noise integrated 1 kHz to 100 kHz offset → 3.9° RMS random phase jitter
- Minimal loss but anywal seems a bit high since doesn't include noise < 1 kHz offset
- Next use FFT analyzer to examine closer offsets from carrier

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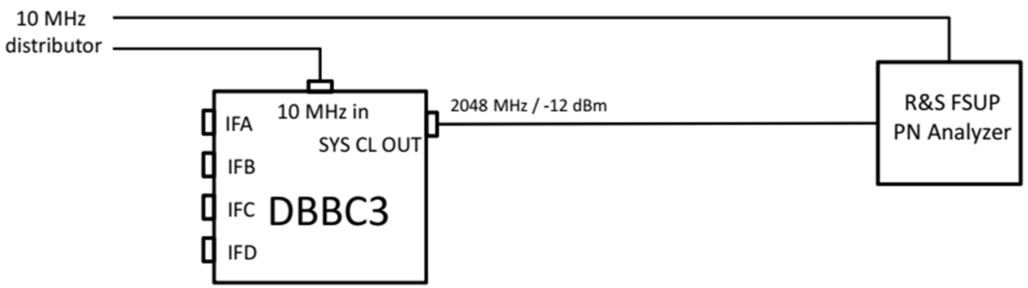
Timing Stability: Sampler Clock on FFT Analyzer



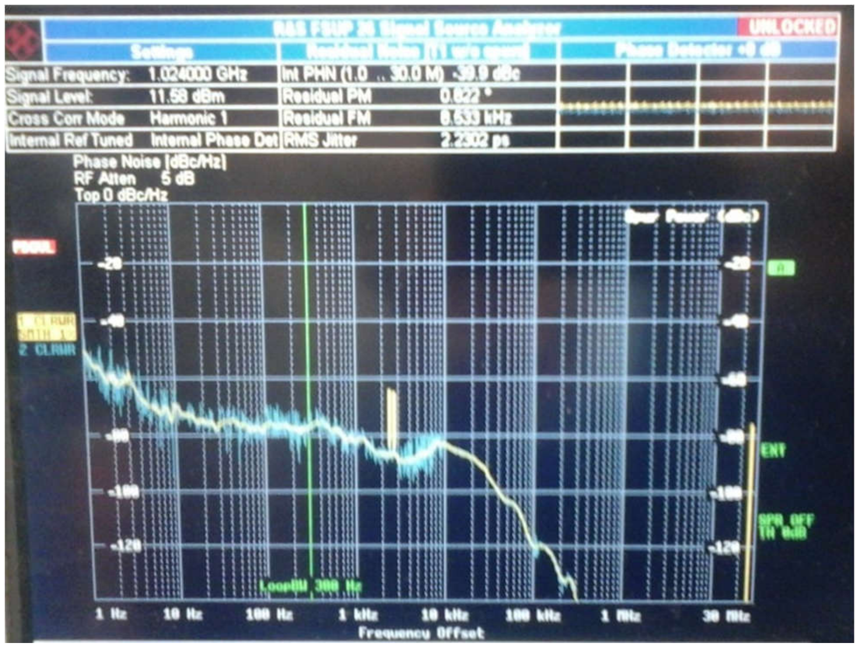
Excess close-in PN

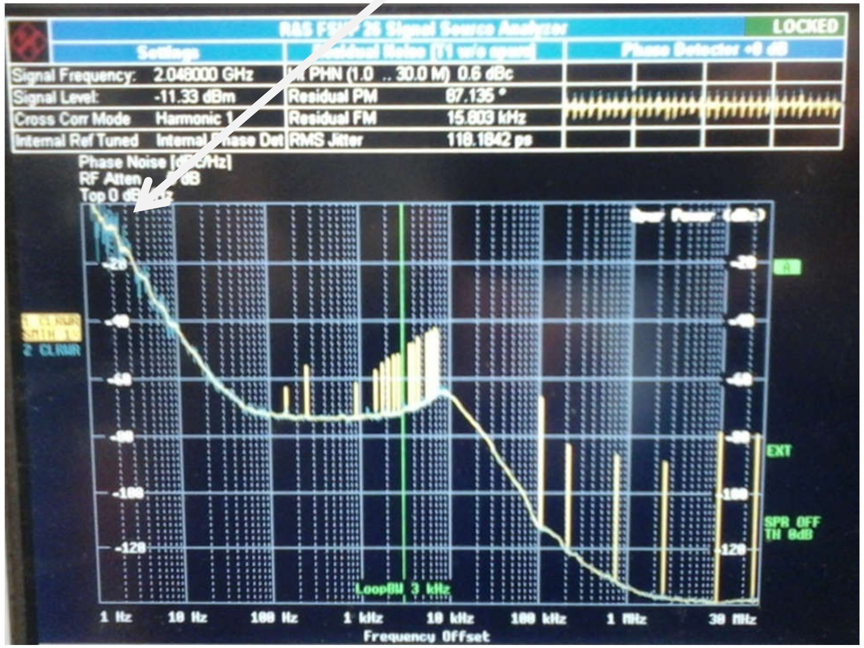
Clock set to 1024 MHz

Clock set to 2048 MHz (EHT setting)

0 dBc

-140 dBc





1 Hz 30 MHz

1 Hz 30 MHz

0.8° RMS random phase jitter

87° RMS random phase jitter(!!!)

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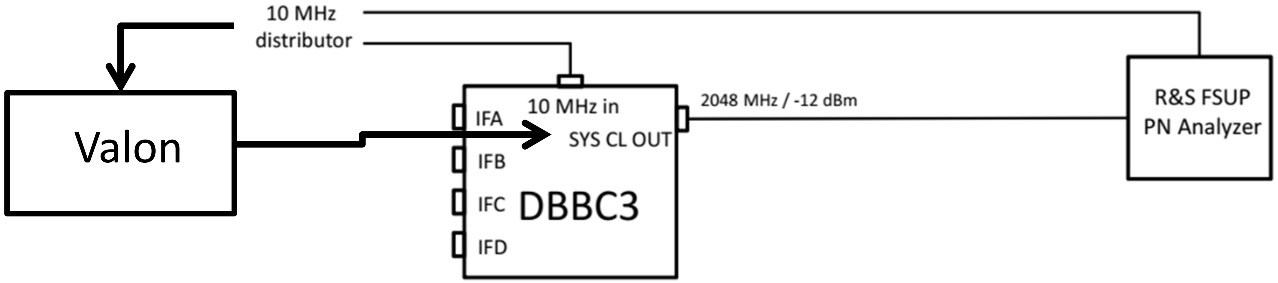
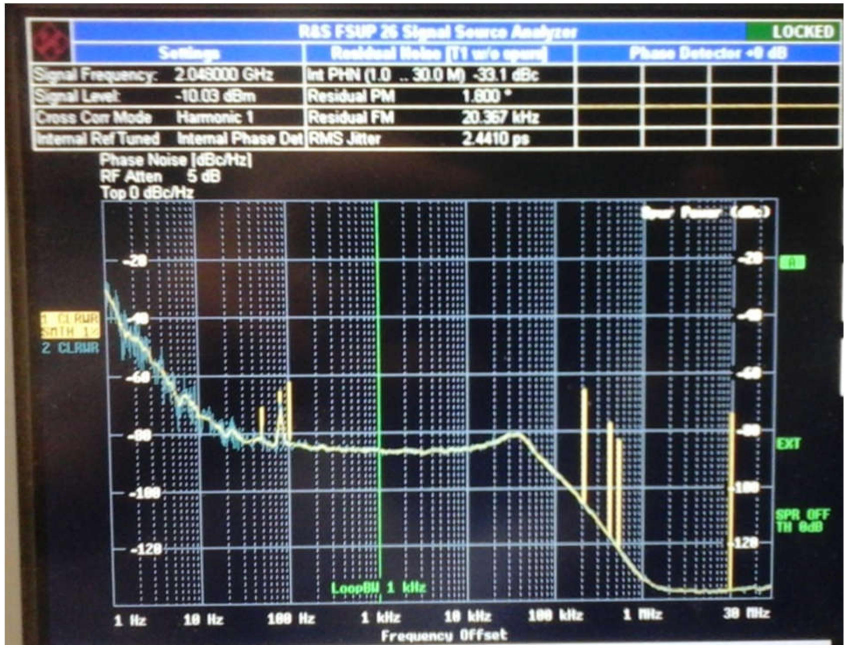
Timing Stability: Sampler Clock on FFT Analyzer



Valon comparison set to 2048 MHz

0 dBc

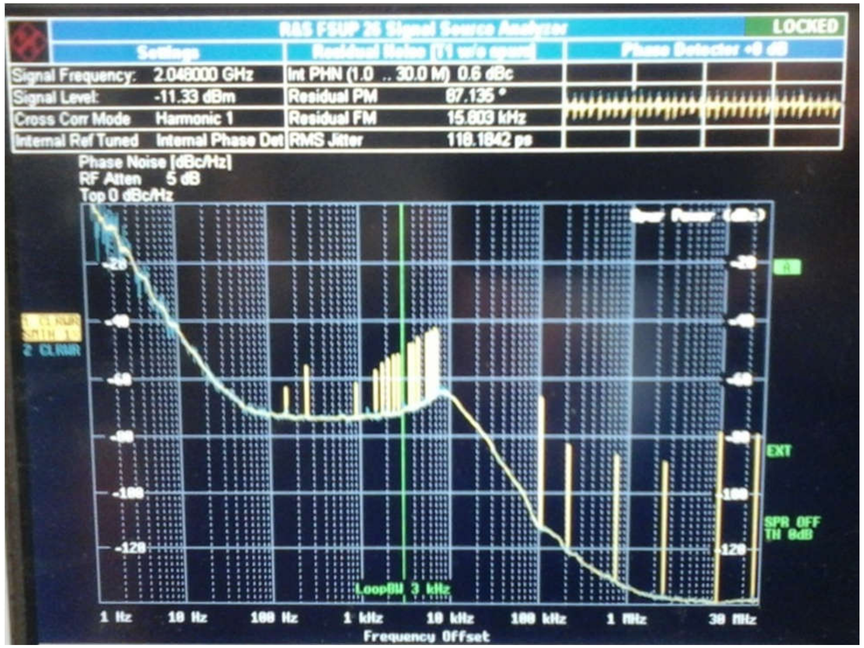
-140 dBc



1 Hz 30 MHz

1.8° RMS random phase jitter

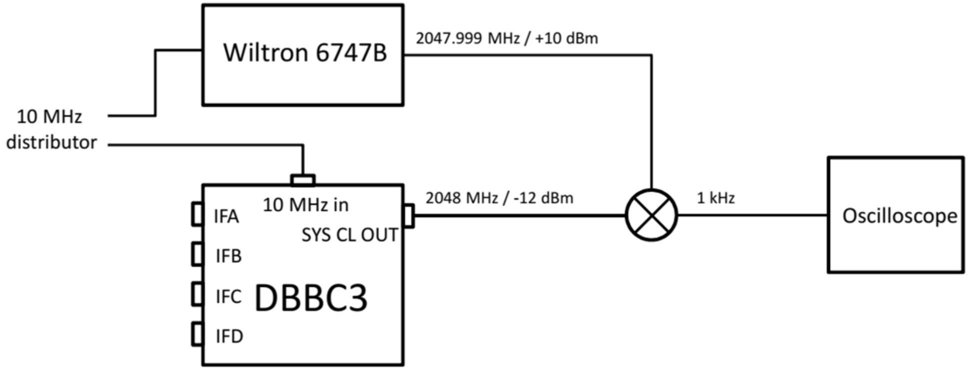
Internal clock set to 2048 MHz



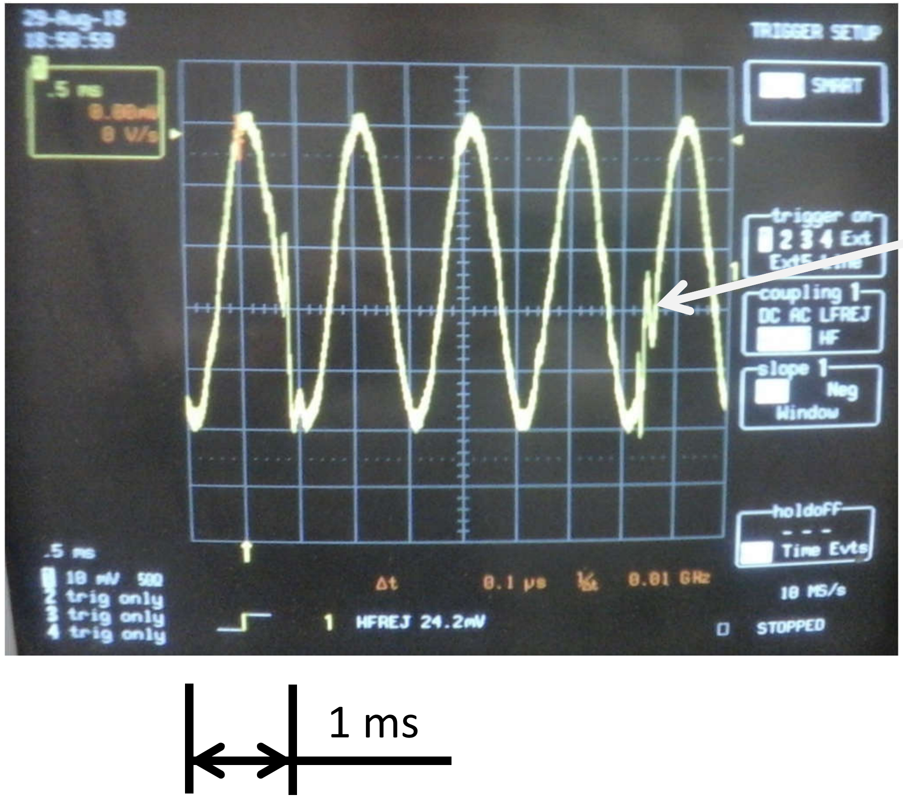
1 Hz 30 MHz

87° RMS random phase jitter(!!!)

Timing Stability: Sampler Clock on Oscilloscope

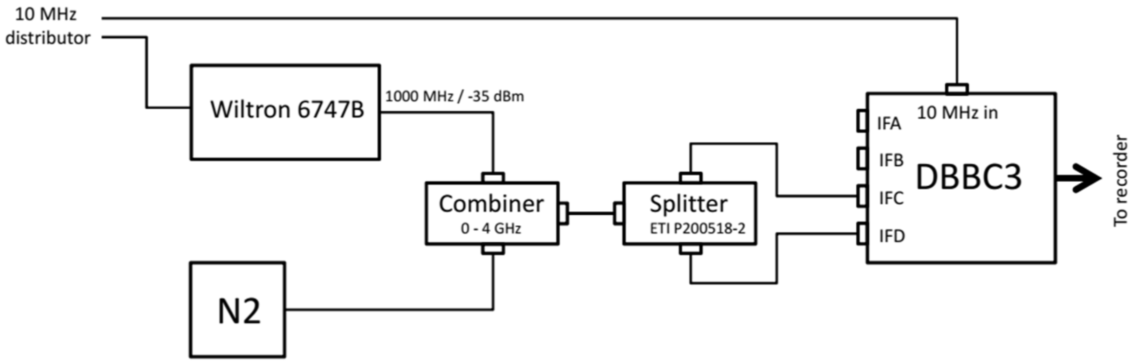


Internal clock set to 2048 MHz

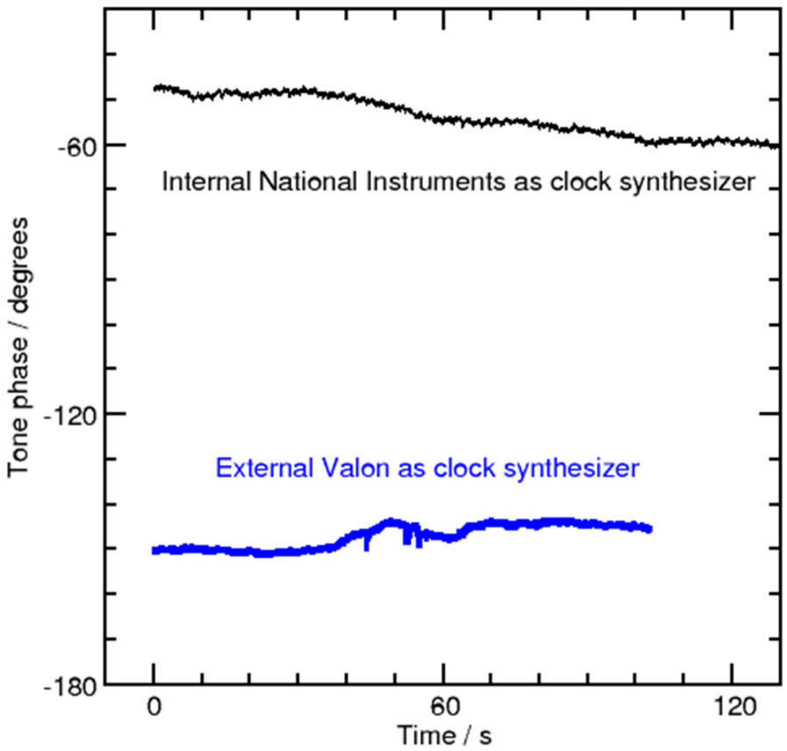


- Solid stable phase
- Much less than 87° RMS
- Occasional wobbles but returns to correct phase
- Valon also wobbles in same way → wobble in Wiltron?
- Looks like FFT analyzer issue

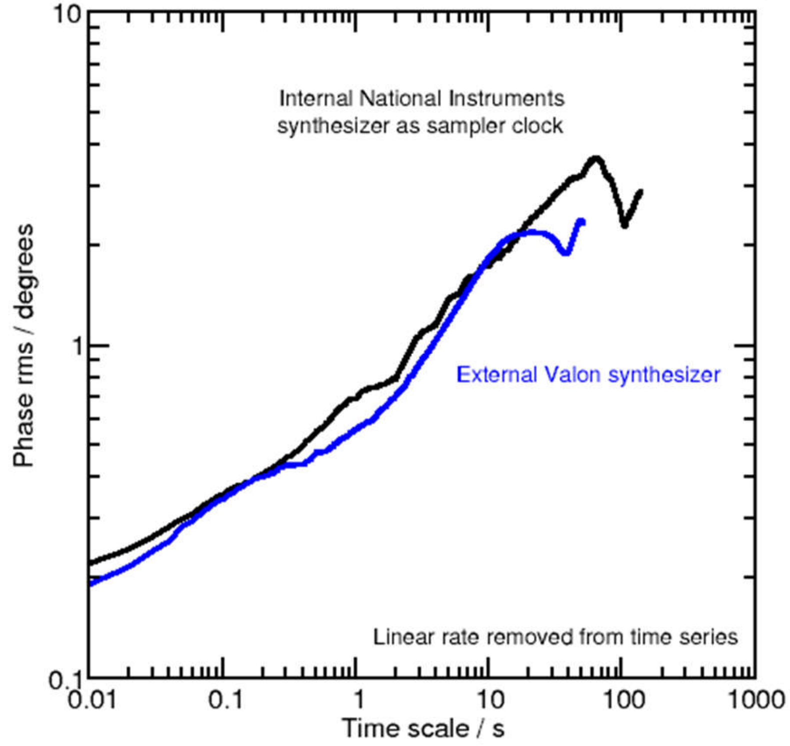
Timing Stability: Phase Stability End-to-End



1 GHz tone phase, APEX DBBC3, Valon vs Internal GCaT Synthesizer



1 GHz tone phase structure function from DBBC3 recording



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Timing Stability: Timestamp Correctness

***`vdiftimecheckUDP`*:**

- VDIF header timestamps are correctly decoded
- Agreement with system time on the Mark 6 from NTP
- Differences typically milliseconds.

Check for Delay Jumps in Recording:

Long history of recordings over many experiments → no delay jumps

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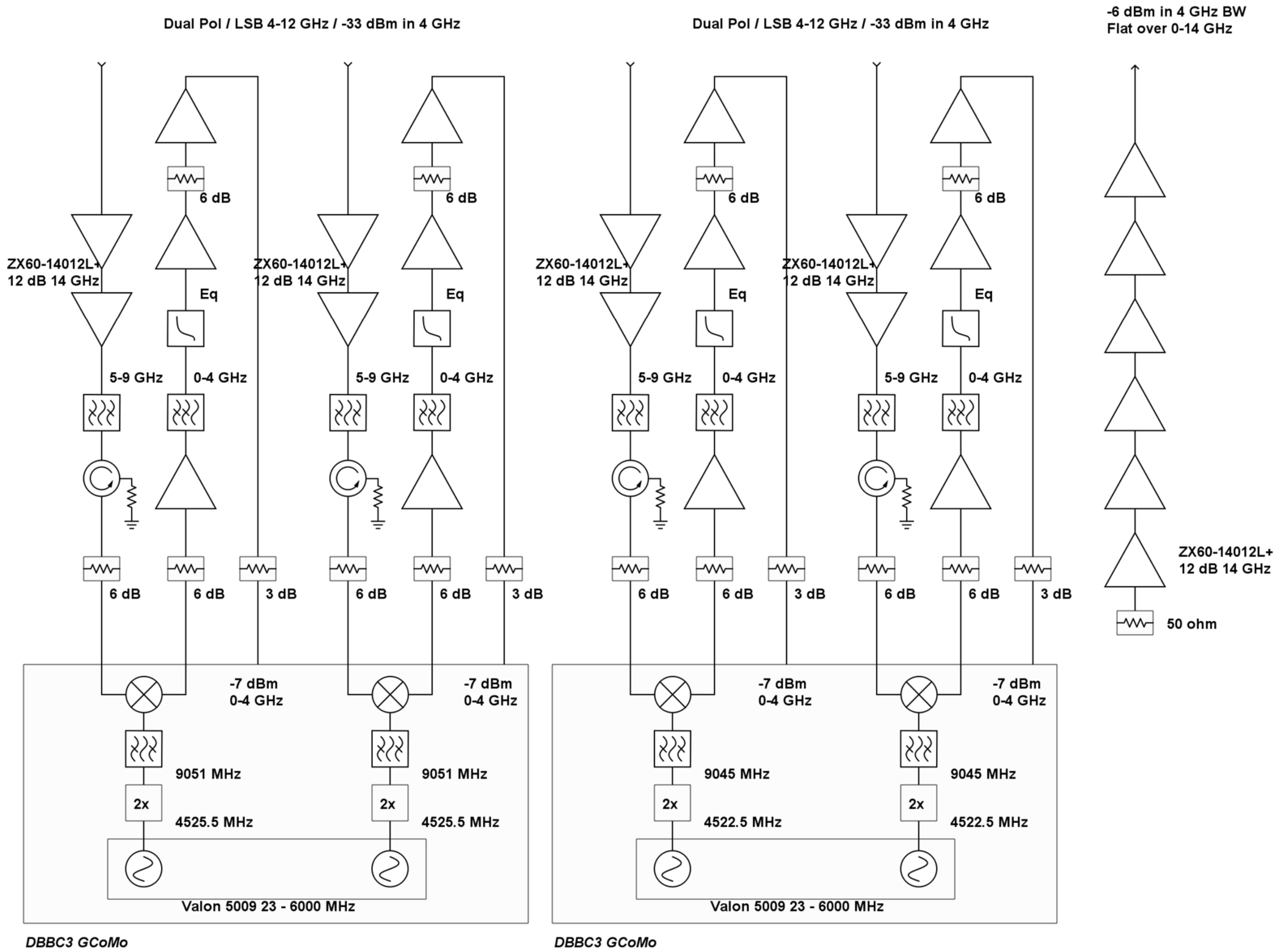
Analogue Conditioning



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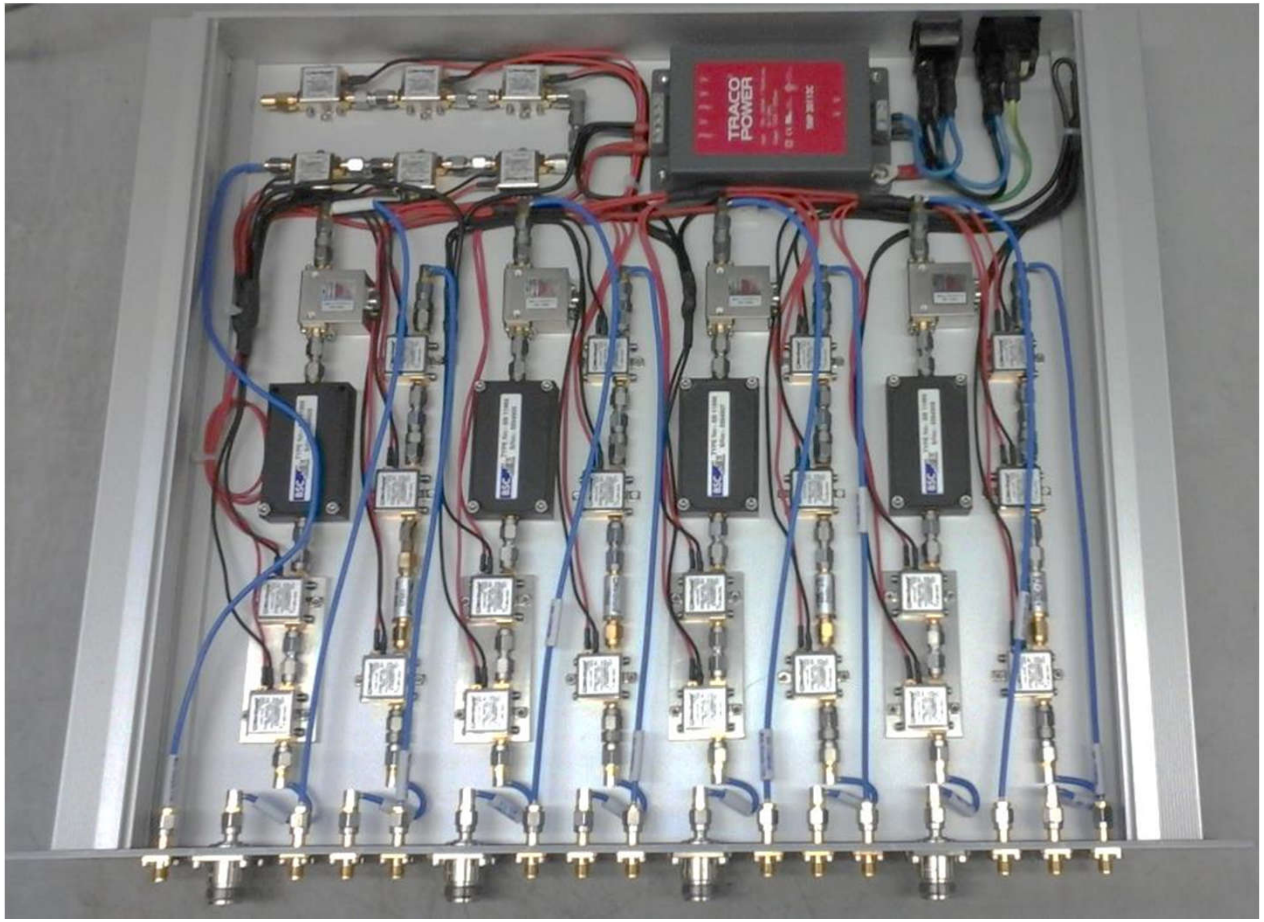
Analogue Conditioning:



Analogue Conditioning Module for DBBC3 at APEX:

4-12 GHz IF in from receiver

Gain, 5-9 GHz BPF, impedance matching, downconversion (in GCoMo)

0-4 GHz gain, baseband out to DBBC3 GCoMo

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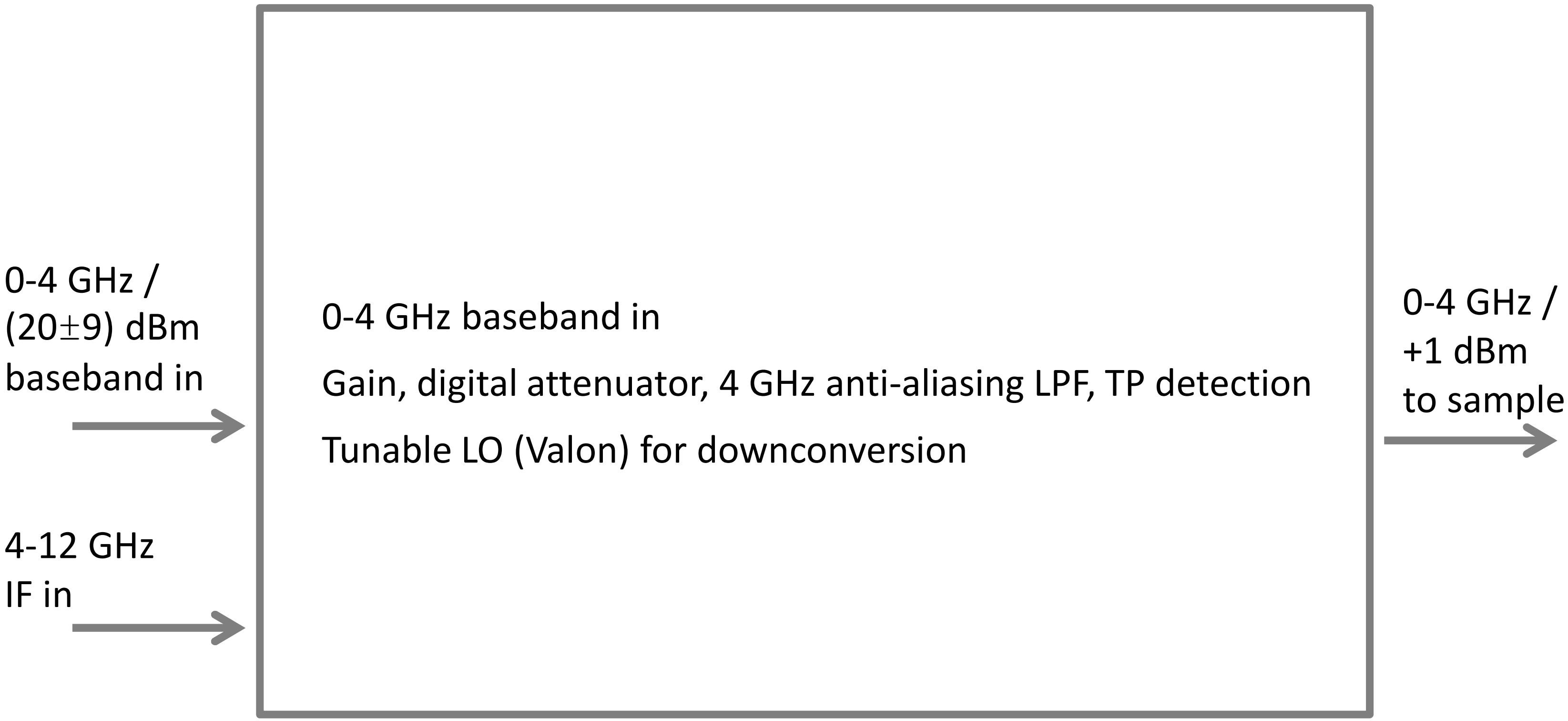
Analogue Conditioning: GCoMo



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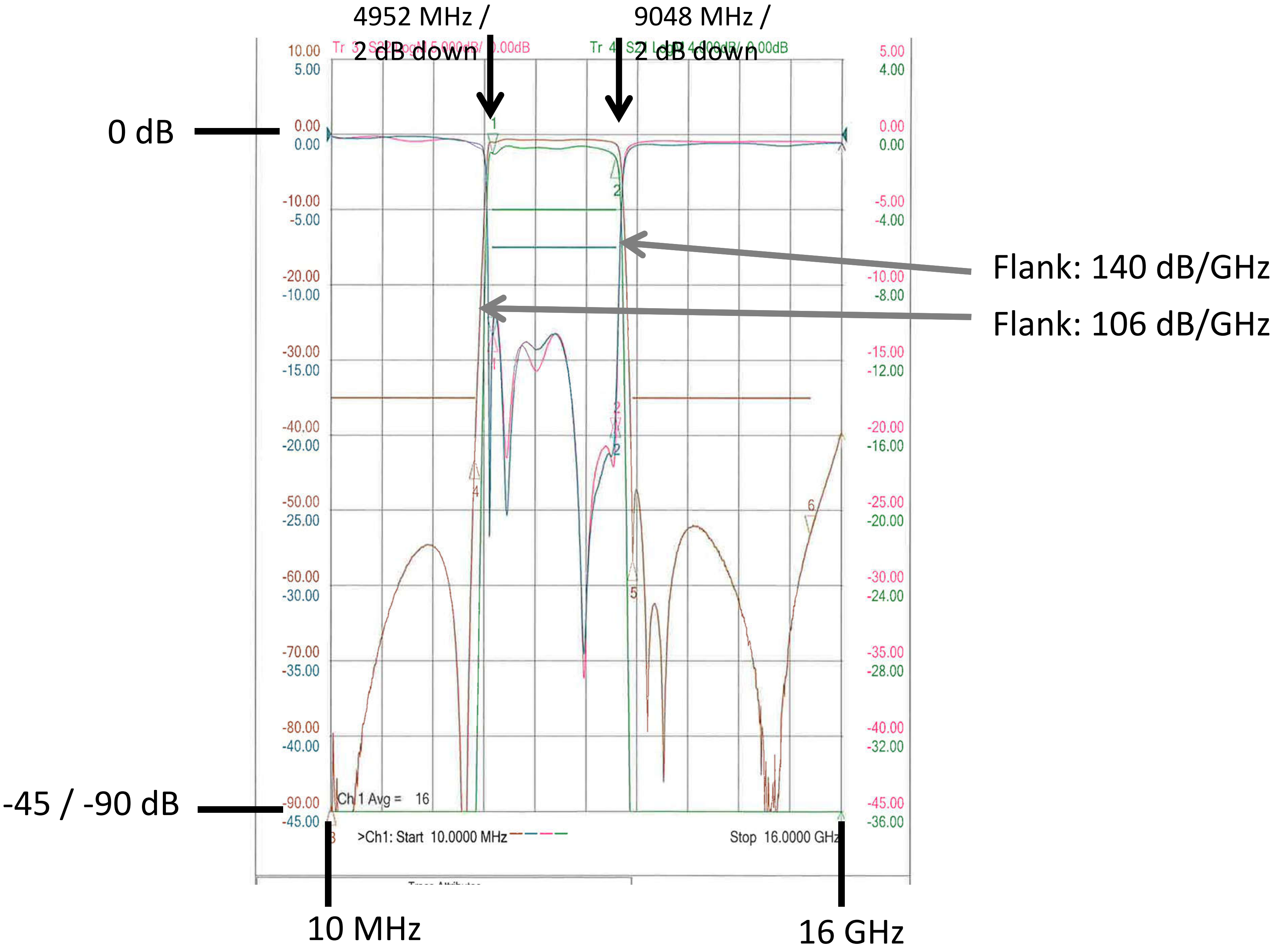
Analogue Conditioning: 5-9 GHz BP filter (BSC)



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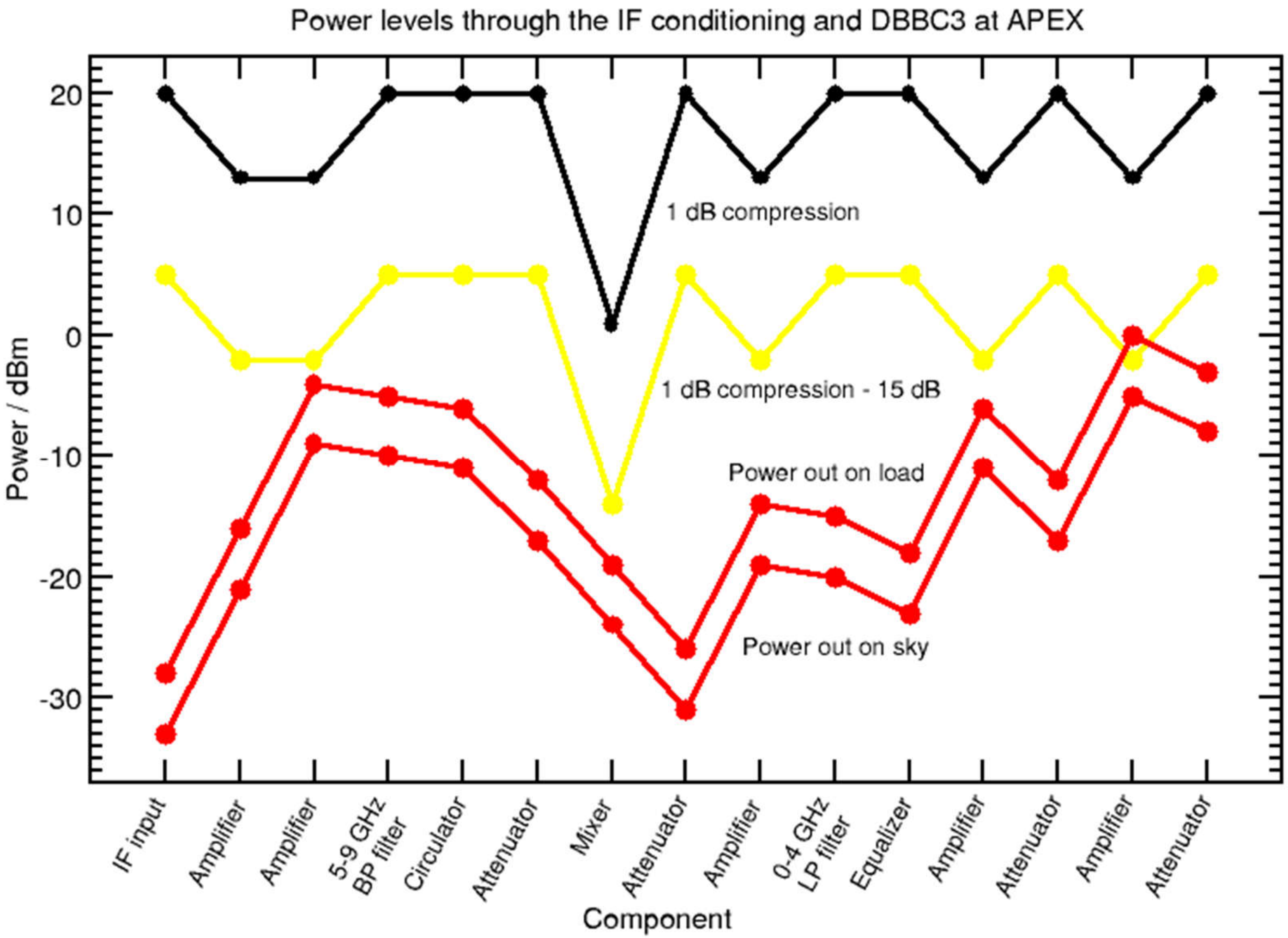
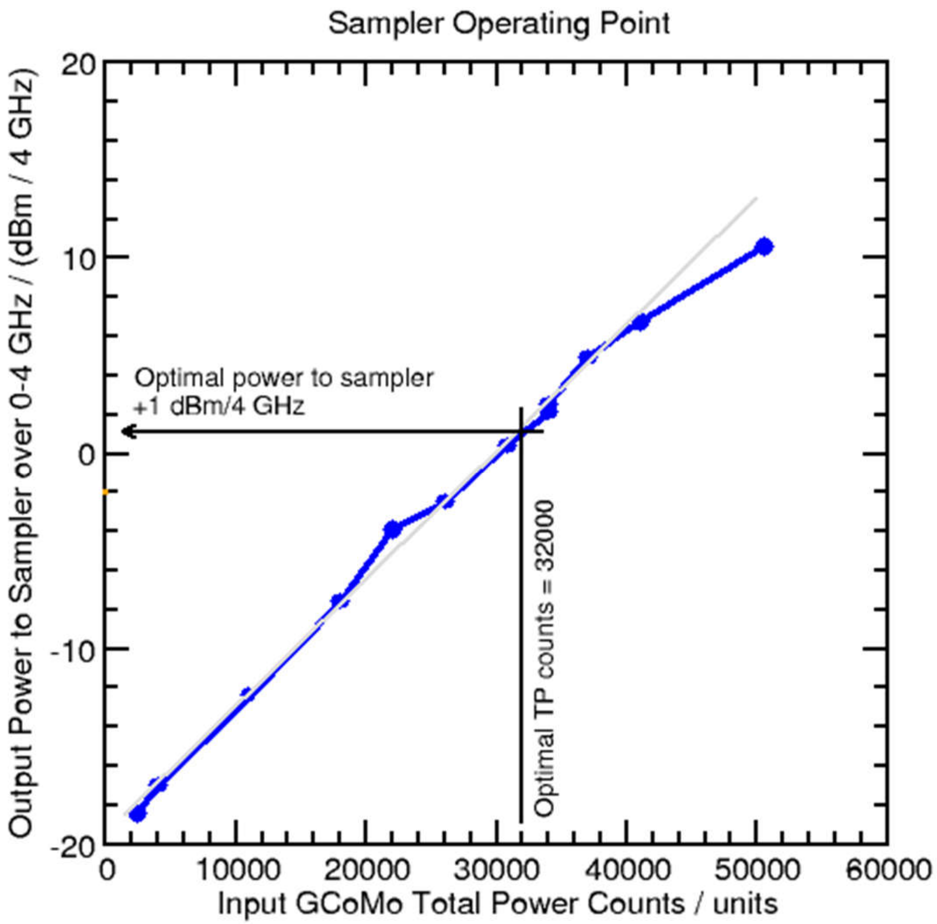
Analogue Conditioning: Headroom Design



Design rule: Stay ≥ 15 dB below 1 dB compression point

Analogue Conditioning: Linearity and Operating Point



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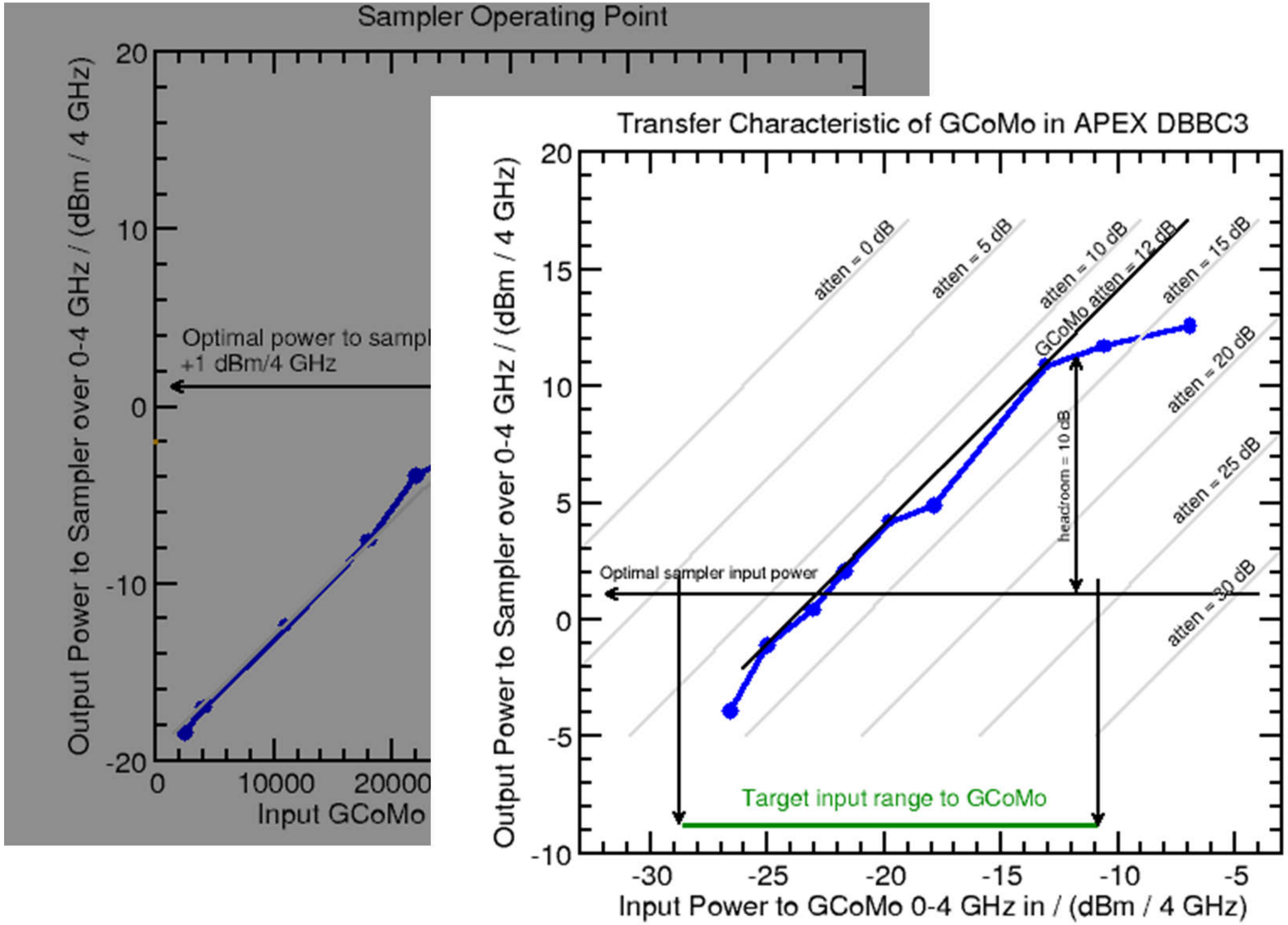
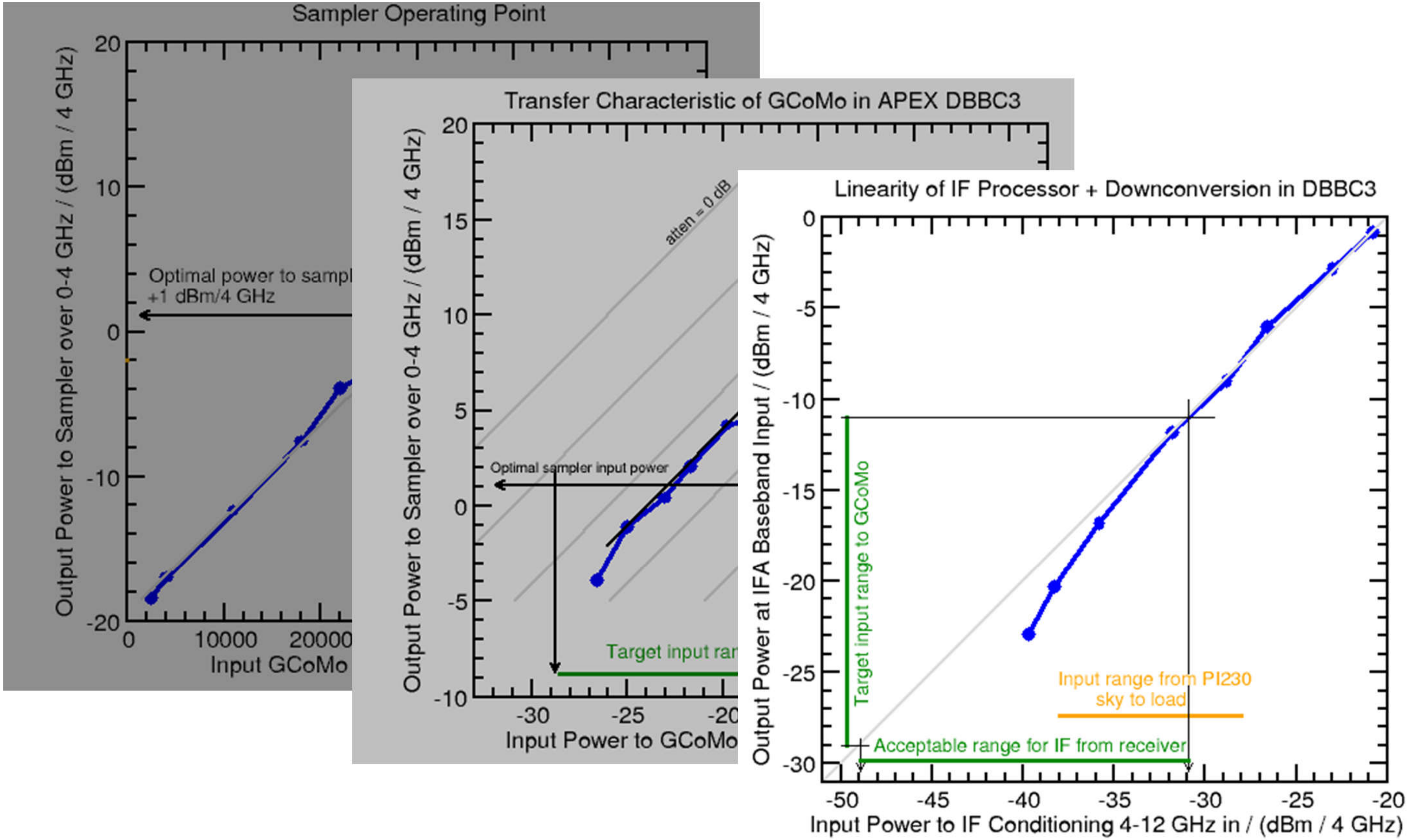
Analogue Conditioning: Linearity and Operating Point



Analogue Conditioning: Linearity and Operating Point



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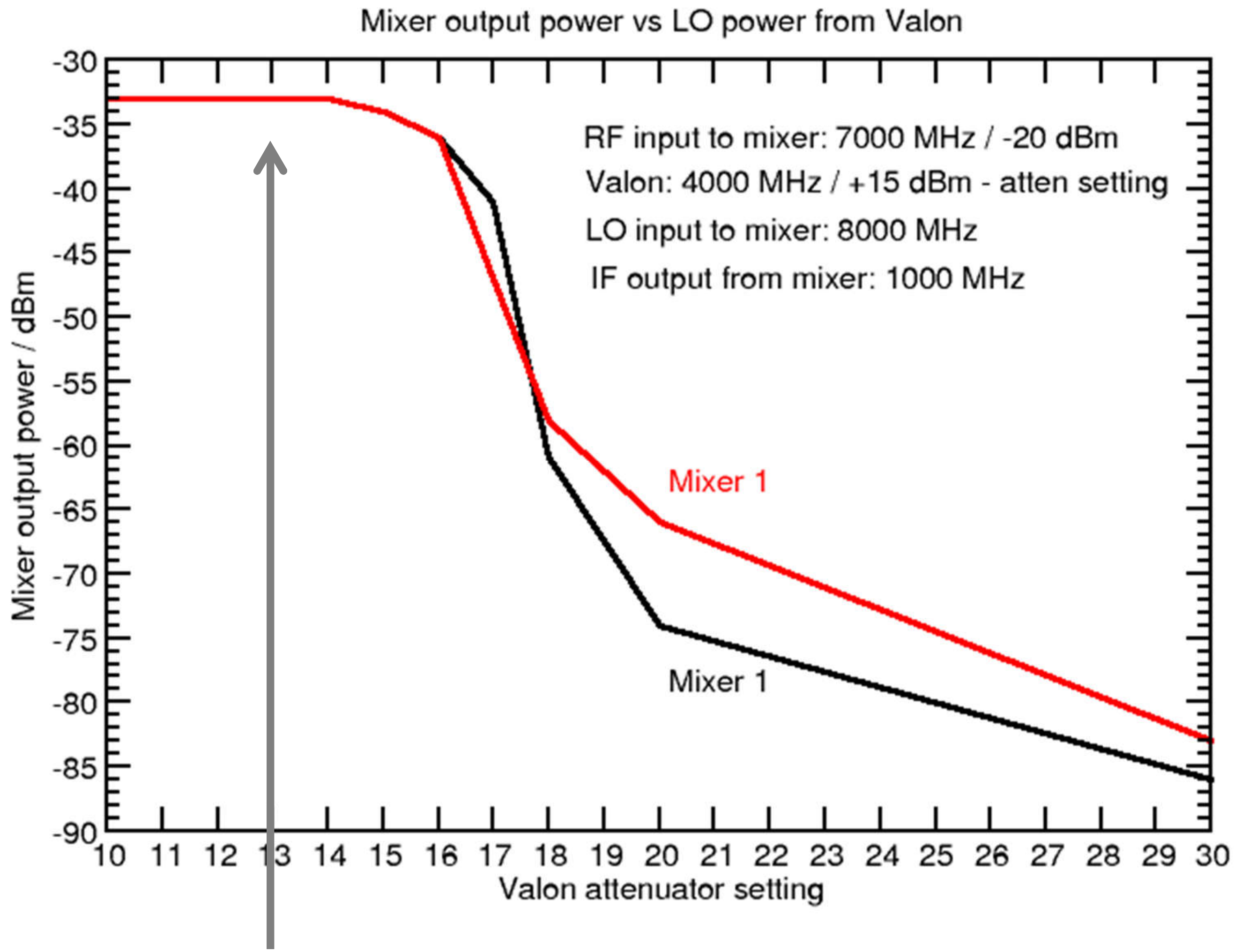
Analogue Conditioning: Mixer LO Power Requirement



Operating point for LO power, mixer in saturation

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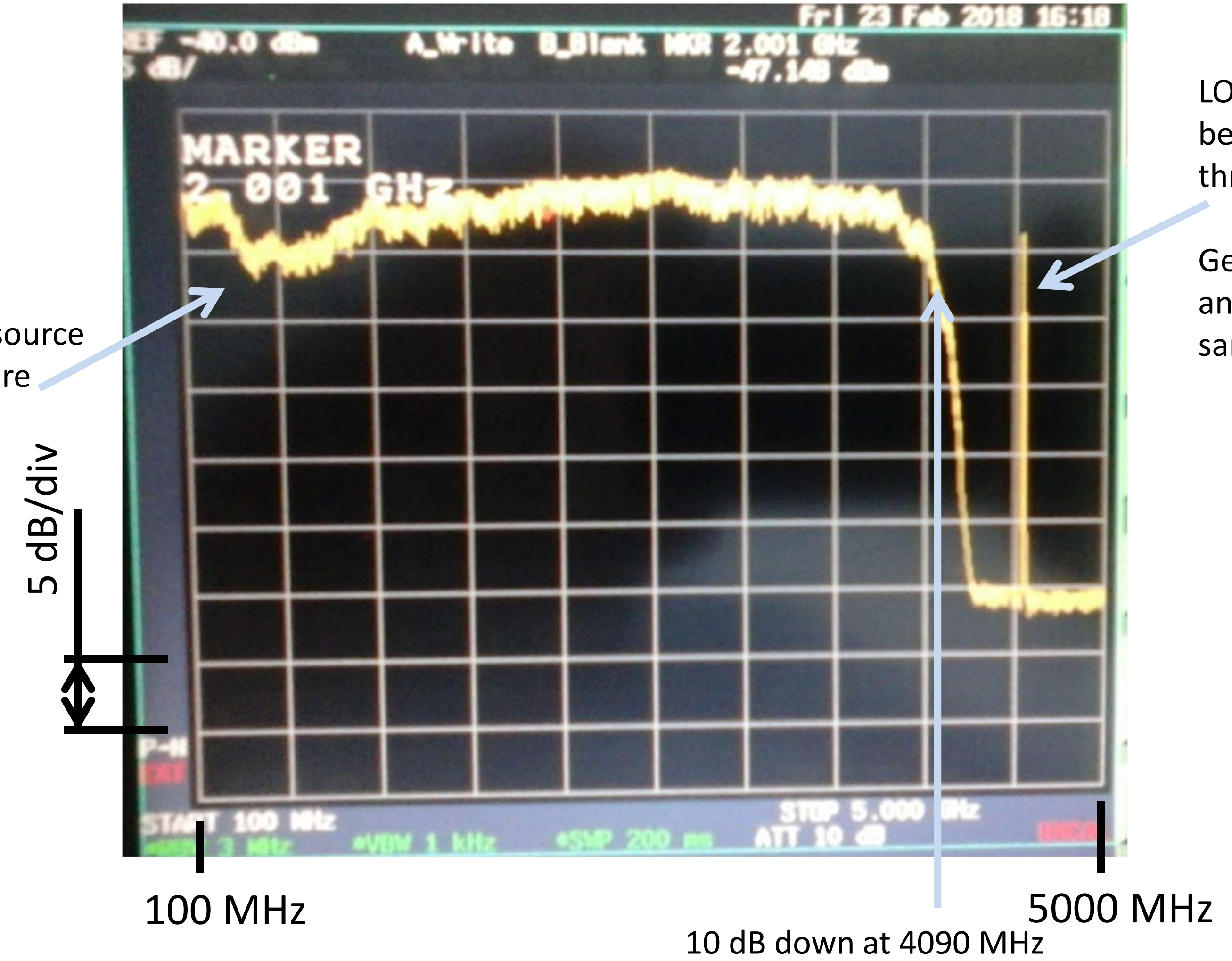
Analogue Conditioning: Analogue Passband Shape

Passband at 0-4 GHz GCoMo Input
after downconversion from 5-9 GHz
IF source: nearly flat noise 0-14 GHz



Noise source structure

LO fundamental at 4524 MHz before doubler breaking through mixer to IF

Gets removed by 0-4 GHz anti-aliasing LPF before sampler

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Digital Data Integrity

8 bit state counts:	All lines active, none tied high or low
2 bit state counts:	Values after thresholding typically 16 % 34 % 34 % 16 %
Total power spectrum:	Clean of artifacts
Analysis of recorded VDIF:	No missing packets, No out of order packets, ADC thread re-interleaving done correctly, Data validity is high on DiFX/fourfit

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Reliability: Sustained recording test

- Many weeks of run time on the APEX DBBC3:
  No firmware instability (eg no loss of sync, no delay jumps, no hangs).
  Ten DBBC3's in field operations: not much support requested from HAT-Lab

- Many hours of analysis of the output 10 GE data streams on protocol analyzer:
  no errors, no packets out of order.

- 2 % frame loss on Mark 6 recordings fixed with Mark 6 tuning

- Cooling: FPGA die temperatures 49 °C to 57 °C for ambient temp 23 °C to 29 °C.
  Max spec 120 °C. Comfortably low.

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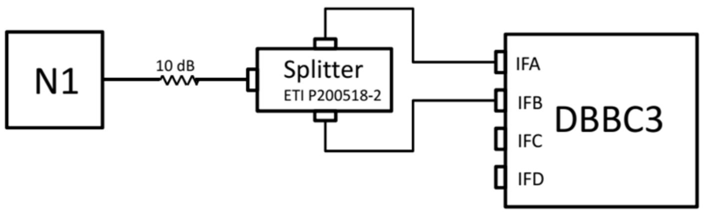
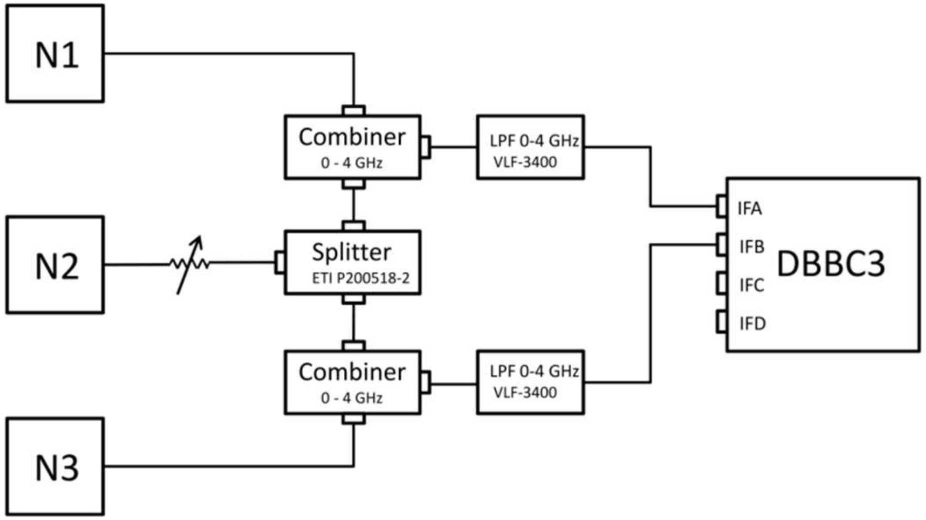
Zero Baseline Test: DBBC3-DBBC3 Setup

For 100 % correlated noise:



For partially correlated noise:



$$\rho_0 = \varepsilon \sqrt{\frac{T_{A1} T_{A2}}{(T_{S1} + T_{A1})(T_{S2} + T_{A2})}}$$

where T_A = antenna temperatures

T_S = system temperatures

ε = efficiency, typical systems ~ 0.5 allow for quantization and processing losses.

Use ε = 1 here to give analogue input correlation coefficient.

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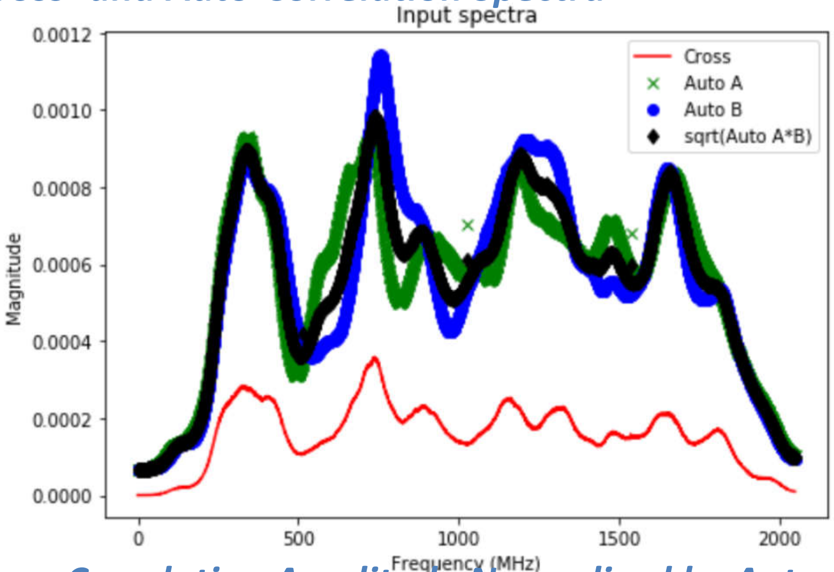
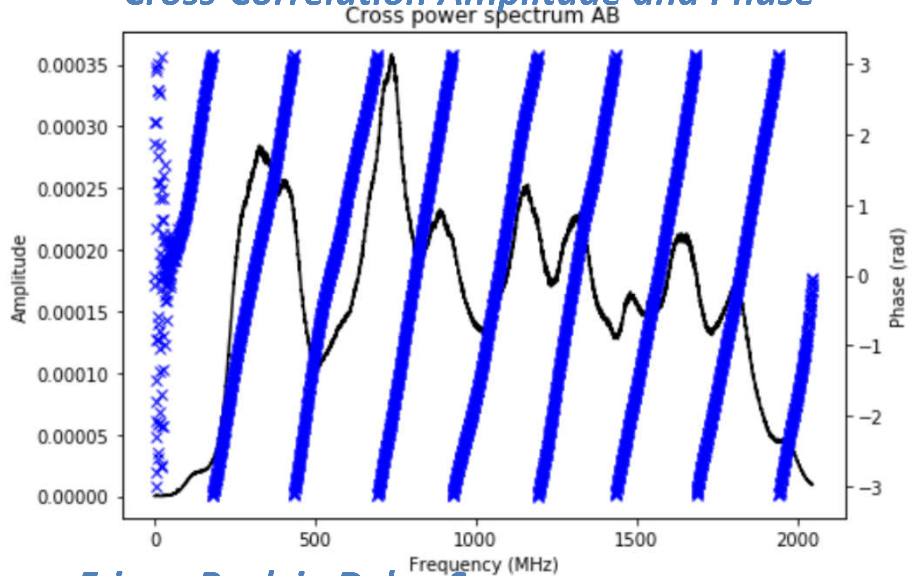
Zero Baseline Test: zerocorr analysis example for ρ_0 = 0.336

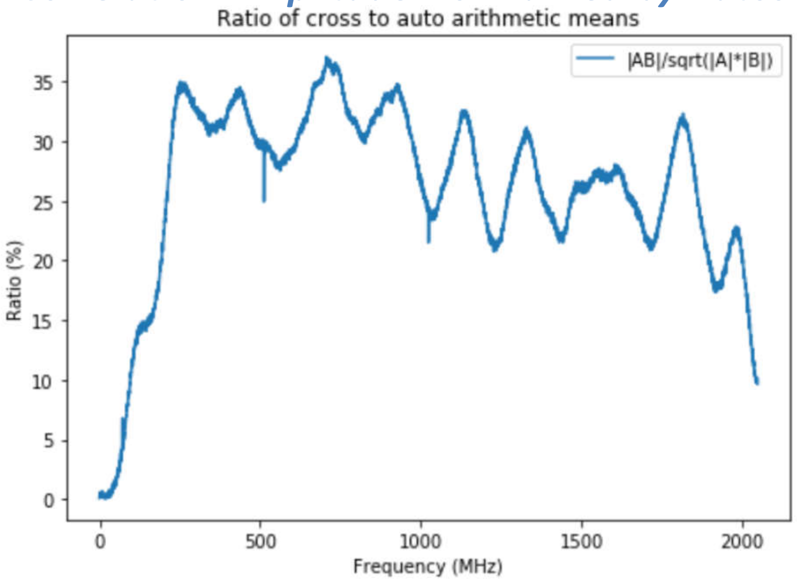
Cross- and Auto-Correlation Spectra



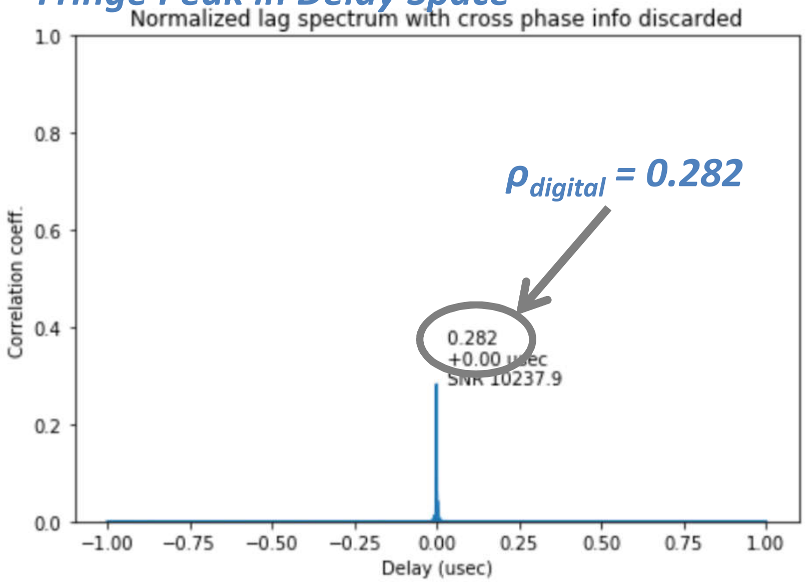
Cross-Correlation Amplitude and Phase



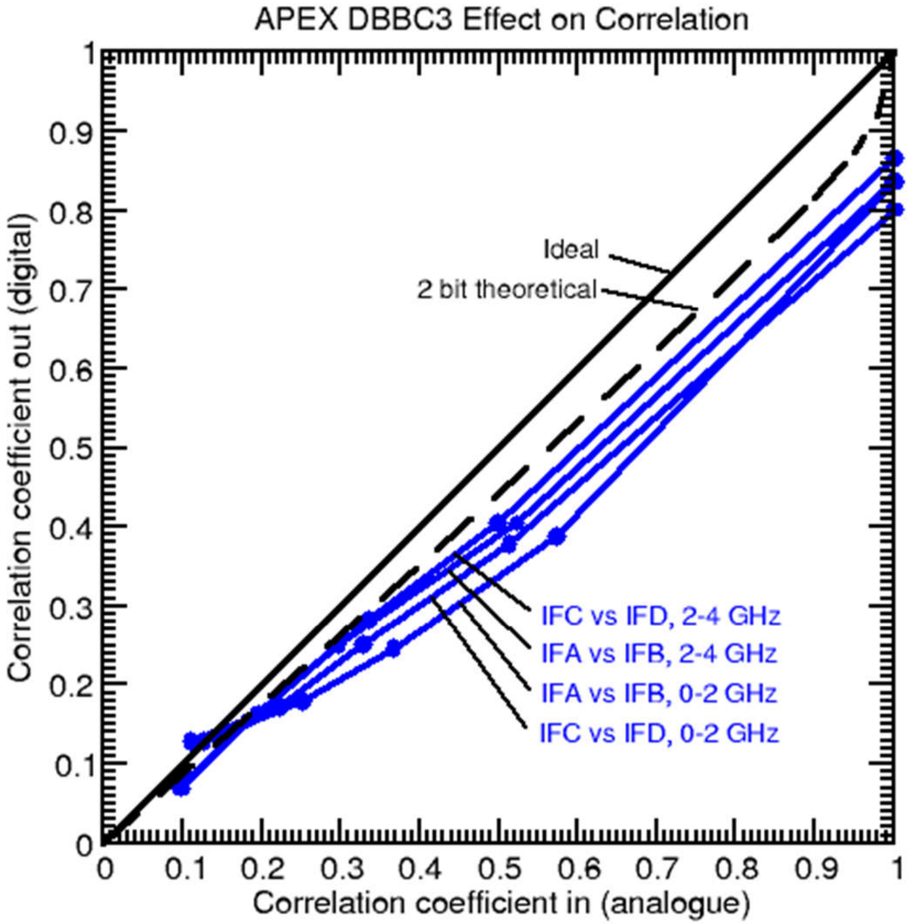
Cross-Correlation Amplitude Normalized by Autos

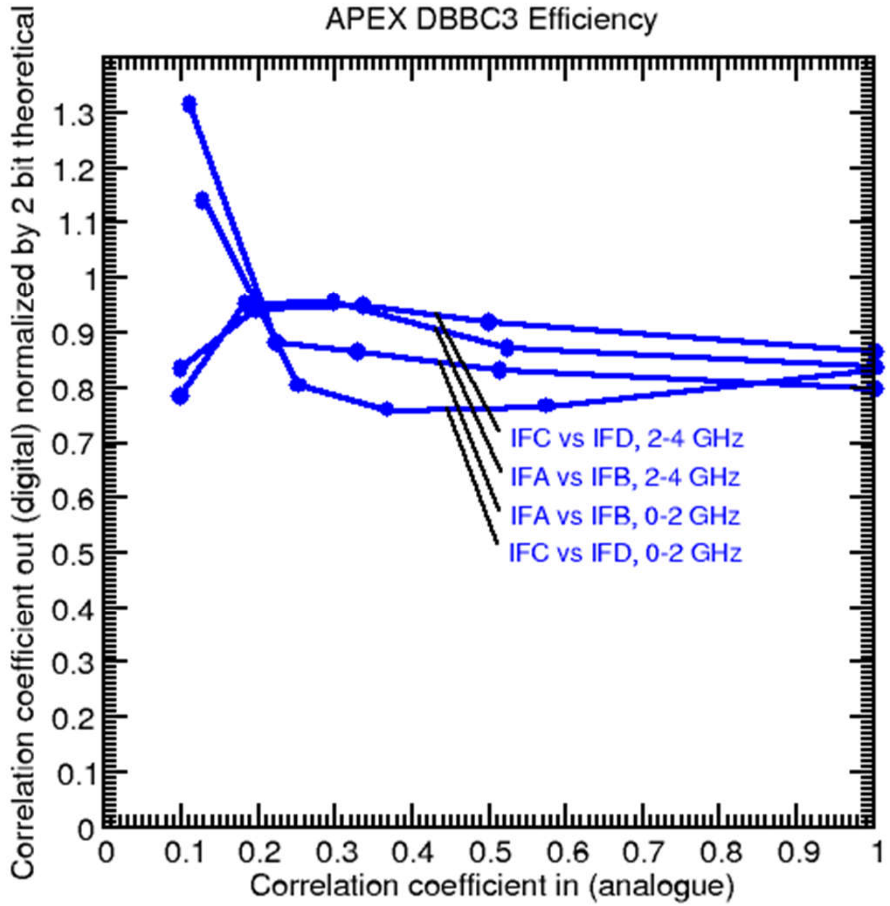


Fringe Peak in Delay Space



Zero Baseline Test: zerocorr analysis example for ρ_0 = 0.336





Efficiency of each DBBC IF: 87 % to 94 %

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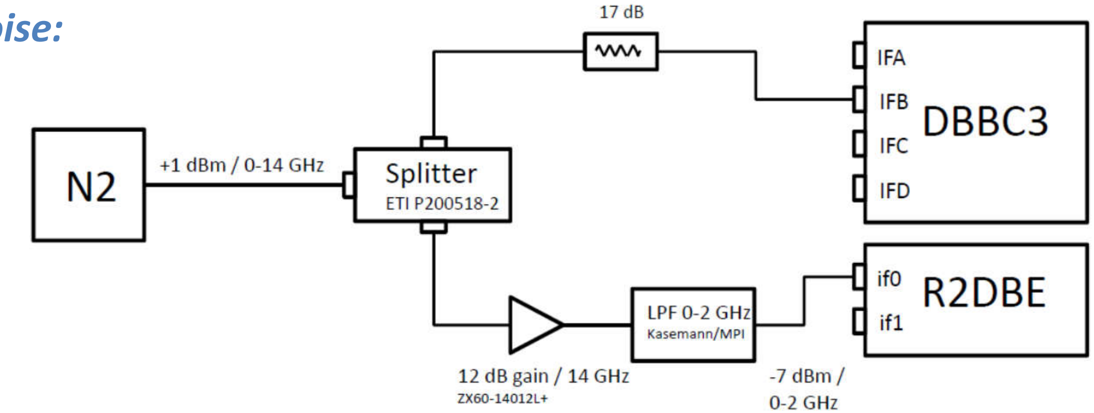
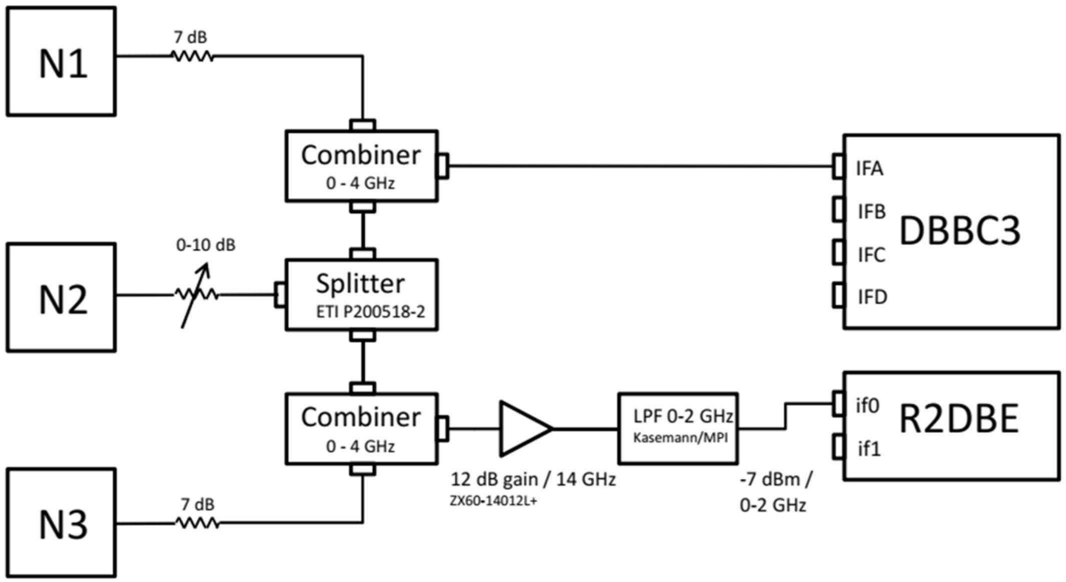
Zero Baseline Test: R2DBE vs DBBC3 Setup

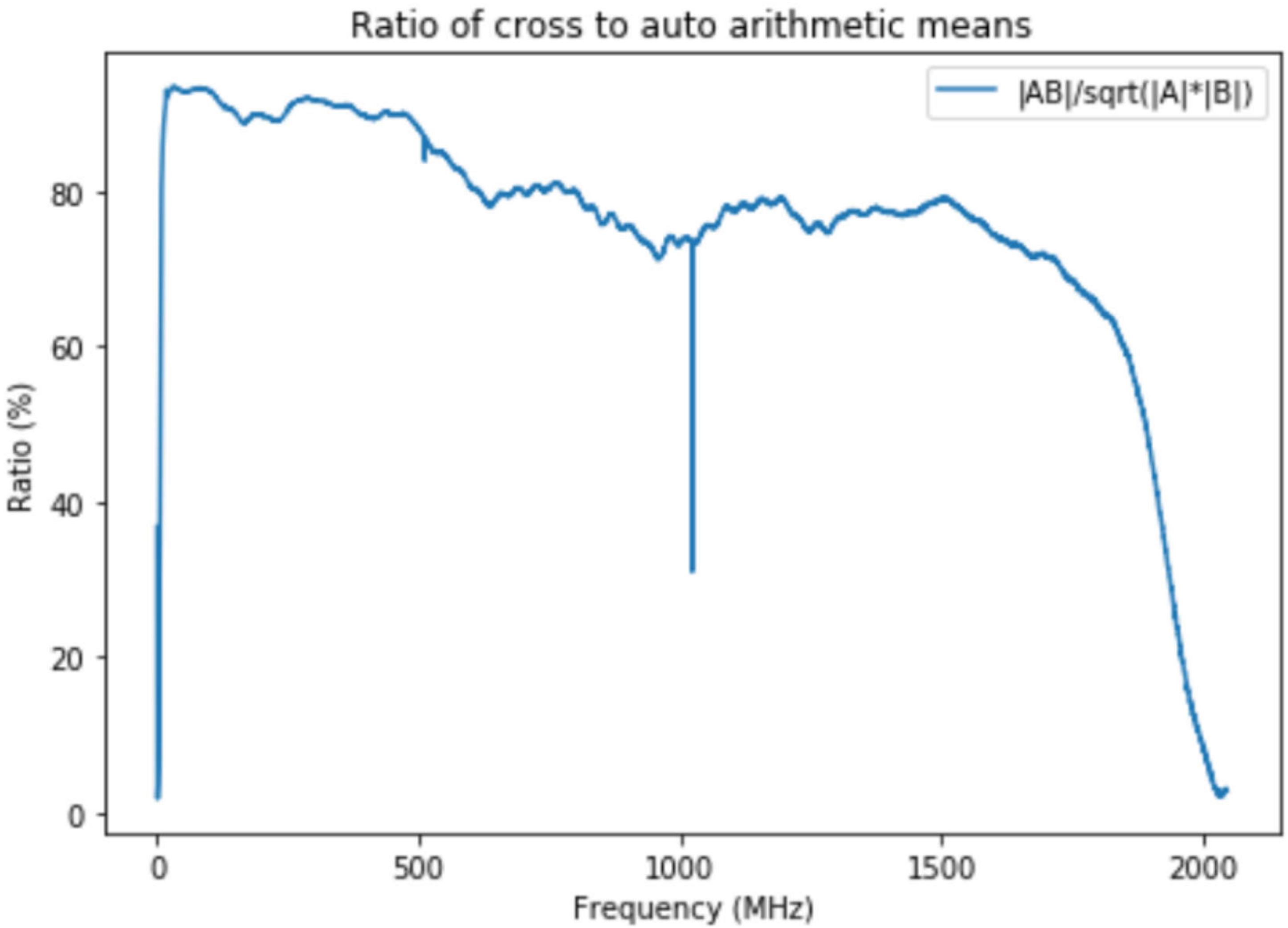
For 100 % correlated noise:



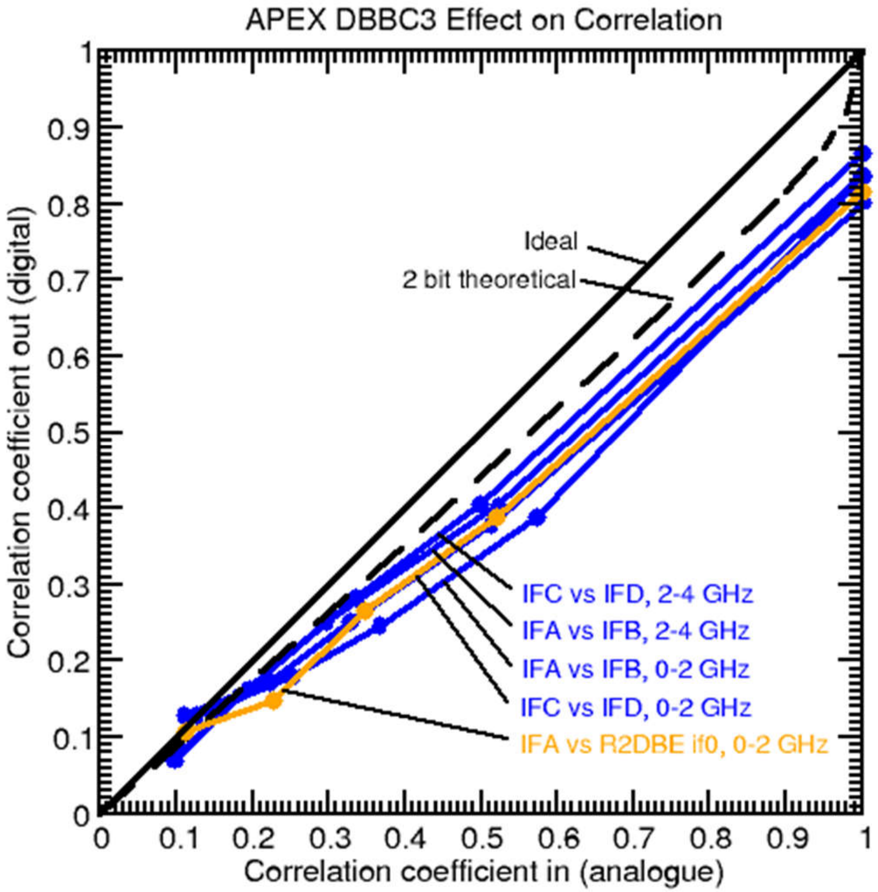
For partially correlated noise:

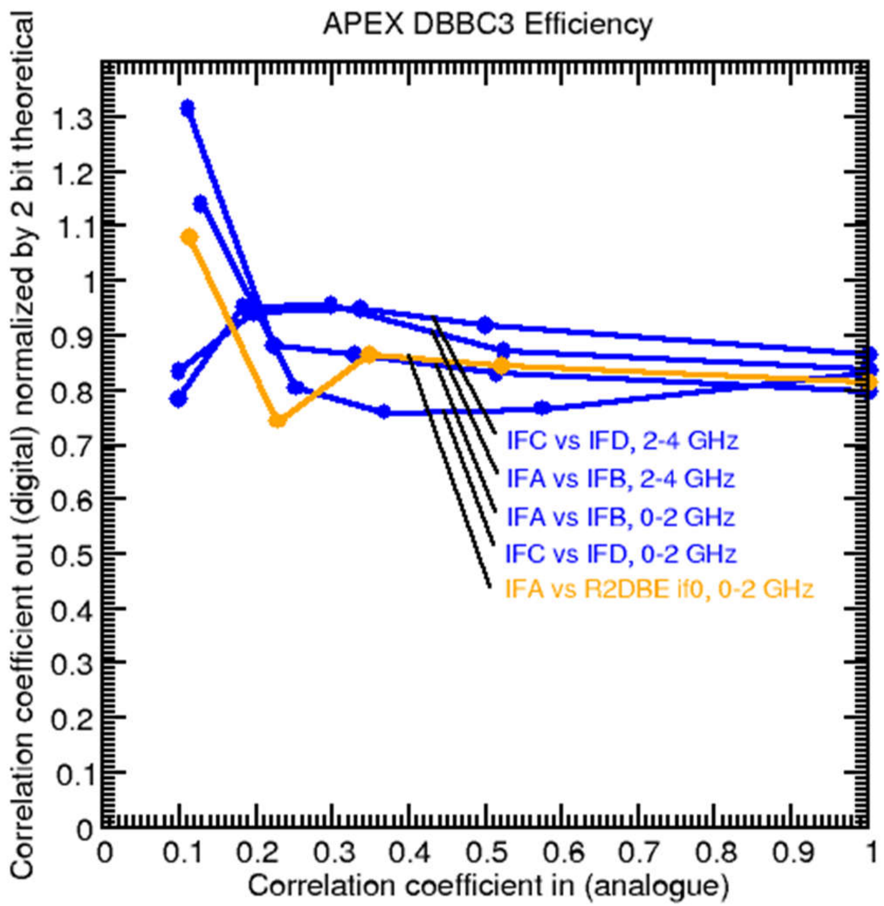


Zero Baseline Test: R2DBE - DBBC3 Cross-Corr Bandpass



Zero Baseline Test: zerocorr analysis example for ρ_0 = 0.336





Efficiency of each backend: 90 % to 93 %

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On-Sky Fringe Test: Kashima - Onsala

People:	Mamoru Sekido	NICT, Kashima Space Technology Centre, Japan
	Kazuhiro Takefuji	NICT, Kashima Space Technology Centre, Japan
	Karl-Åke Johansson	Onsala Space Observatory, Sweden
	Simon Casey	Onsala Space Observatory, Sweden
	Rüdiger Haas	Onsala Space Observatory, Sweden
	Gino Tuccari	MPIfR
	Sven Dornbusch	MPIfR

Date: 27.03.2018, 19 h observing track

Stations:
Kashima 34 m
Onsala 13.2 m twin telescope (ONSA 13NE)

Targets: 203 radio sources, 300 s each, broadband radio source survey

Frequency Setup:
4x 1 GHz bands in range 3 GHz to 11 GHz
Dual linear polarization
1 bit sampling
16.384 Gbps data rate

Data Acquisition:
Japanese DAS: K6 GALAS (at Kashima)
DBBC3 running OCT firmware (at Onsala)

Correlation: Kashima / GICO3 software correlator (NICT)

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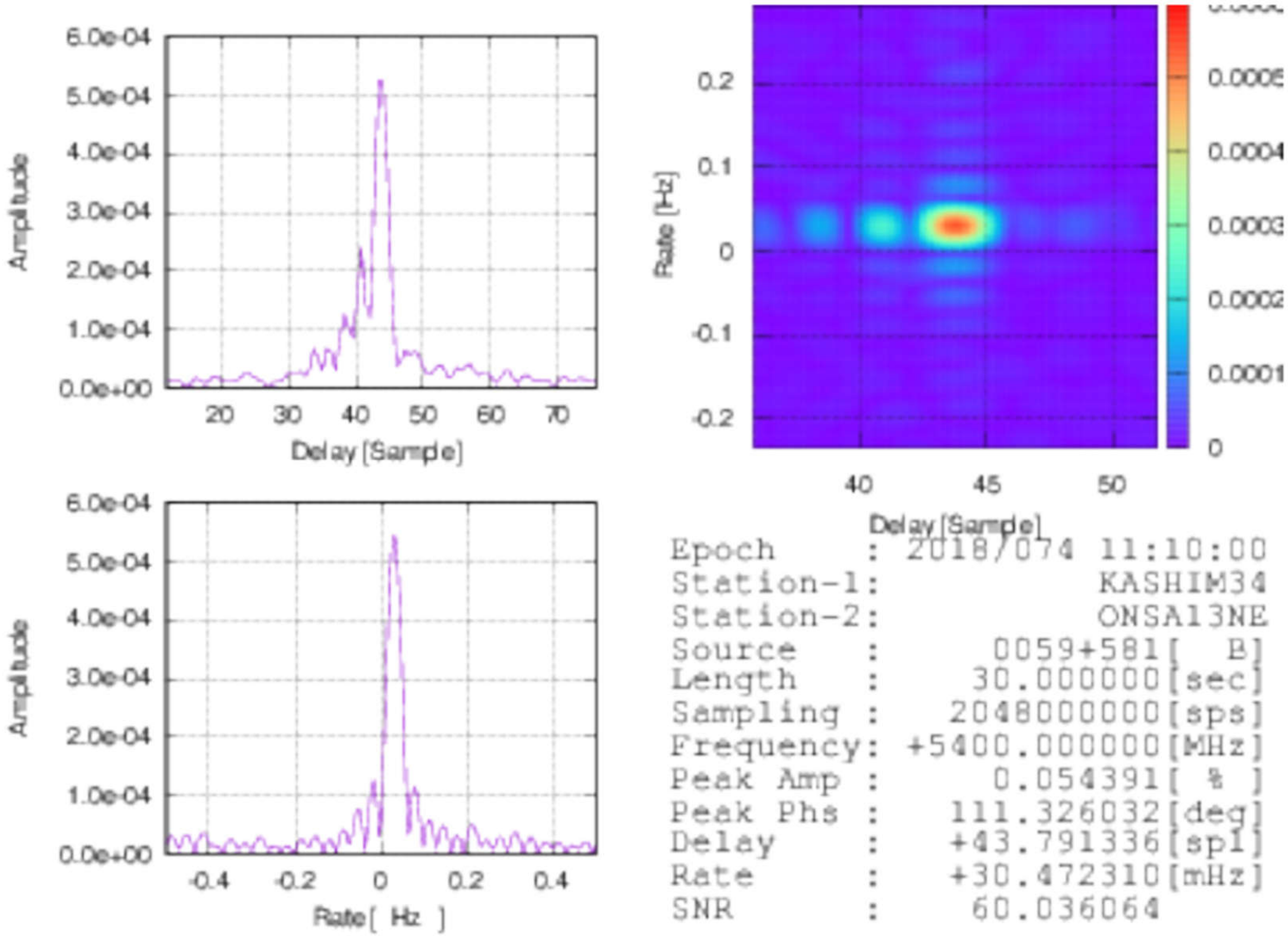
On-Sky Fringe Test: Kashima - Onsala



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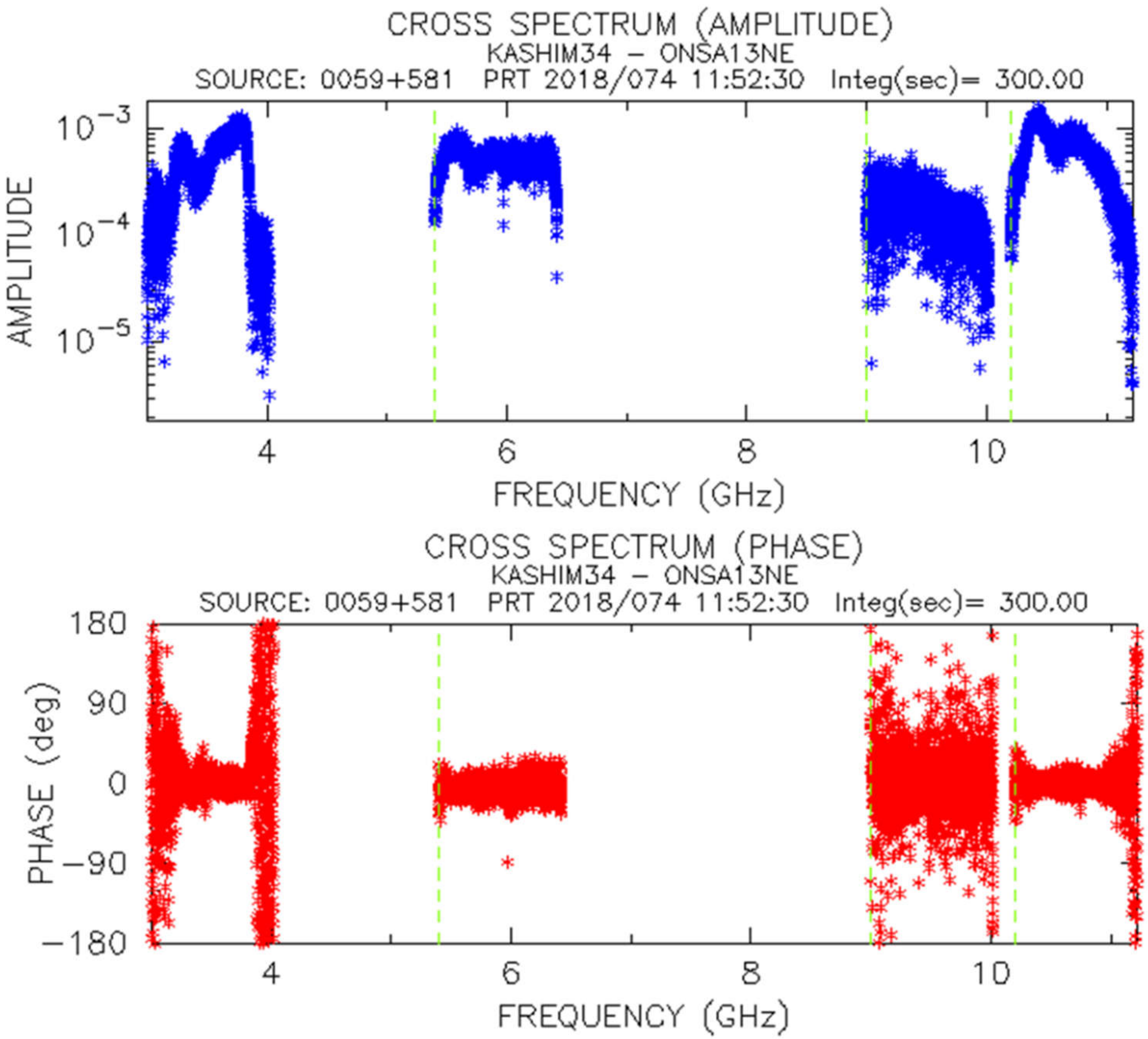
On-Sky Fringe Test: Kashima - Onsala



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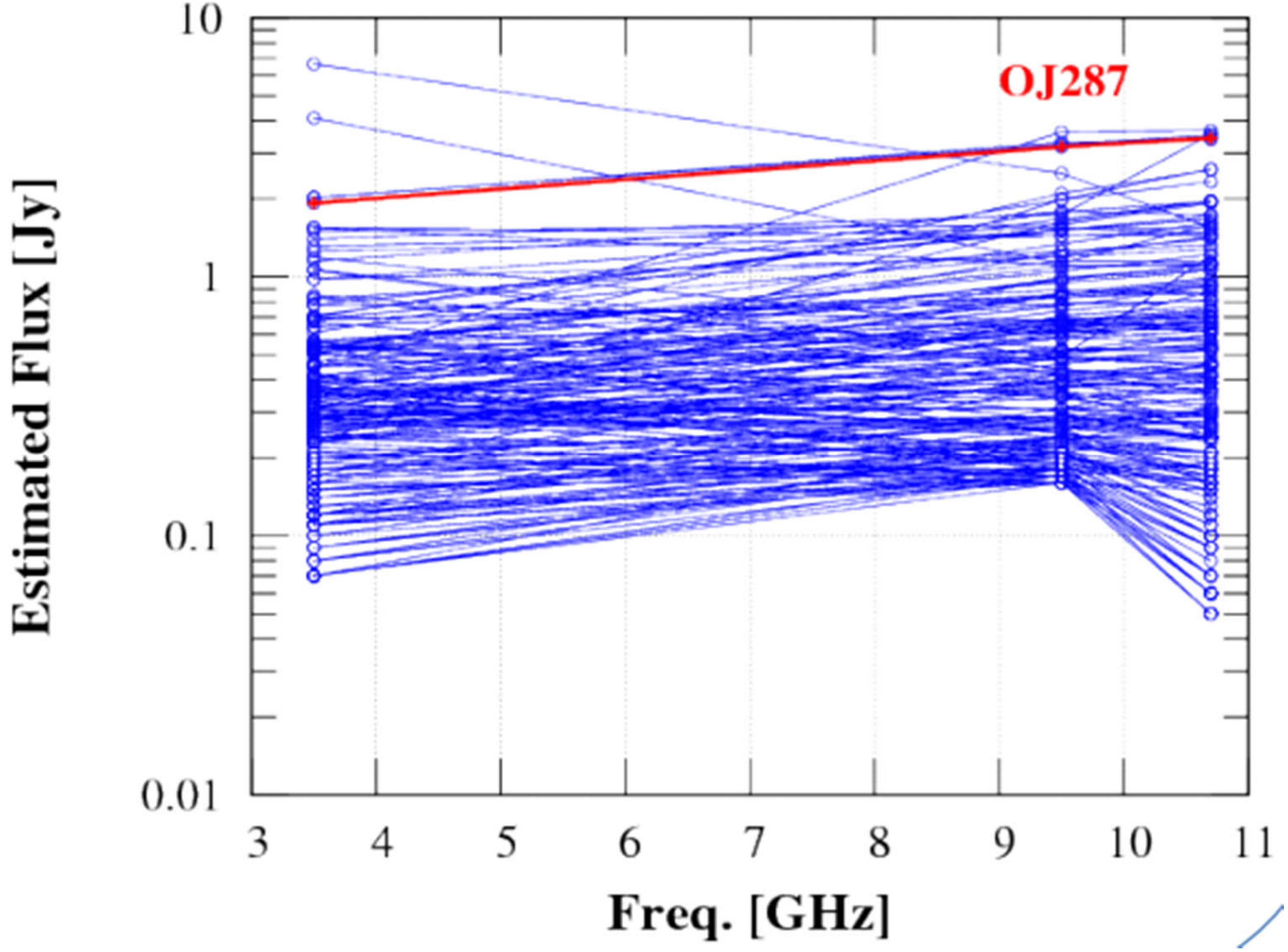
On-Sky Fringe Test: Kashima - Onsala



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DBBC History in EHT at APEX

Session History:

2009 Mar	Project start VLBI at APEX			
2011 Mar	**Install DBBC2**			
2011 Mar	EHT 2011 campaign	(No APEX fringes)	2 Gbps	1x Mark 5C
2012 May	First APEX fringes		2 Gbps	1x Mark 5C
2013 Mar	EHT 2013 campaign		4 Gbps	2x Mark 5C
2015 Jan	First fringes to ALMA	(ALMA - APEX)		
2015 Jan	First fringes to SPT	(SPT – APEX)		
2015 Mar	EHT 2015 campaign		16 Gbps	2x Mark 6
2015 Mar	Fringe test 340 GHz	(APEX-Pico Veleta, APEX-SMTO)		
2015 Jul	ALMA phasing commissioning 230 GHz APEX-ALMA-SMA-JCMT			
2015 Jul	ALMA phasing commissioning 340 GHz APEX-ALMA			
2016 July	**DBBC2 to Bonn for upgrade to DBBC3**			
2016 Nov	Fringe test for PI230 at APEX (2x R2DBE)			
2017 Apr	**Install DBBC3**			
2017 Apr	EHT 2017 campaign	(parallel DBBC3 / R2DBE)	(32 Gbps	2x Mark 6) x2
2017 Apr	**Return DBBC3 to Bonn for refinement**			
2018 Apr	EHT 2018 campaign		64 Gbps	4x Mark 6
2018 Sep	***Now: ready to re-install DBBC3 at APEX and Pico Veleta***			
2018 Oct	*EHT 345 GHz Test*			