DBBC3 Testing for APEX and Pico Veleta

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07.09.2018

Objective

Ensure the DBBC3 is operating correctly for use with EHT at APEX and Pico Veleta.

Introduction to the DBBC3

The DBBC3 is the latest generation of VLBI backend from HAT-Lab/MPIfR in the series of DBE, DBBC, DBBC2, each with successively increasing bandwidth. The DBBC2 was the workhorse backend at APEX and Pico Veleta for EHT observations from 2011 to 2015 and is in constant use in the EVN and other telescopes. The APEX DBBC2 was upgraded to DBBC3 in 2016 and has been in use at APEX since then. The DBBC3 provides downconversion and sampling of 4 GHz per IF and can be configured with up to 8 input IF bands, giving a total sampled bandwidth of up to 32 GHz and output data rate up to 128 Gbps.

The DBBC3 offers three different firmware versions for channelizing the 4 GHz of bandwidth per IF input - DDC, DSC, and OCT (PFB development is in progress). The digital downconverter firmware is a port of the DDC from the DBBC2, which is the main mode used in the EVN and elsewhere. The DBBC3 DDC firmware offers the selection of up to 16 sub-bands per IF input with a selectable bandwidth between 1 MHz and 64 MHz per sub-band. The DSC firmware (direct sampling) offers the full 4 GHz band. The latest firmware, OCT, offers arbitrary band selection within the 4 GHz input IF with the use of one or two digital FIR-filters per IF input. An OCT mode with 1 GHz wide sub-bands for VGOS has been extensively tested by Onsala and Hobart, including a successful fringe-test with the Kashima antenna in Japan. The EHT OCT mode uses a 2 GHz wide OCT derivative which allows one to split the 4 GHz downconverted and sampled baseband into two 2 GHz pieces (0 GHz to 2 GHz and 2 GHz to 4 GHz). The OCT mode offers full compatibility with the R2DBE backends. The port of PFB firmware from DBBC2 has begun.

For T_{sys} measurement at EVN, VGOS, and elsewhere, the DBBC3 generates a TTL output signal at 80 Hz to switch the noise diode signal on and off for noise-adding radiometry and synchronously detects the total IF power in DDC firmware.

Hardware:

Sampler:	e2v, 4 GHz bandwidth, quad-core, interleaved sampling	
FPGA:	Virtex 7 485	
Sampler clock synthesizer:	National Instruments LMX2531	
Embedded GPS	Provides time to nearest second for initializing the data timestamp register	
Interfaces on back panel (SMA-F):	10 MHz in	
	10 MHz out	Output power-split copy of *10 MHz in*
	1 PPS in	
	1 PPS out	Output Power-split copy of *1 PPS in,* 2.0 V p-p into 50 Ω
	Analog Mon.	Output from 256 MHz DAC for monitoring sampled data
	1 PPS Mon.	1 PPS generated from firmware
	SYS CL. OUT	For monitoring sampler clock synthesizer output
	Cont. Cal. OUT	Output TTL for switching noise diode
	GPS	Input from GPS antenna, has DC bias for pre-amplifier
Interfaces on GCoMo (SMA-F):	Cont Cal In	
	4-15 GHz In (unfilt.)	Input RF to mixer for downconversion
	Out (unfilt.)	Output IF from mixer after downconversion
	0-4 GHz In	Input baseband to sampler, (-20 ± 9) dBm / 4 GHz
Interfaces on CORE3 card:	4x SFP+ ports per sampler-FPGA chain, 10 GE fibre transceivers, simplex	
Interfaces to embedded PC:	Ethernet RJ 45, VGA, PS/2 keyboard + mouse	
Interface for operations M&C:	Socket connection for ascii text, can be commanded from FieldSystem or other	
Interface for engineering M&C:	Socket connection to embedded PC then serial or 32-bit parallel PCI-7200 bus	
Interface to GCoMo:	PCI-9111 from embedded PC	
Interface for FPGA programming:	JTAG with bit files resident locally on embedded PC	
Output data format:	VDIF packetized by FiLa10G firmware on CORE3 board	
Physical:	19” rack mount, 8U (357 mm) high, 500 mm deep, 35 kg	
Electrical:	240 V, 50 Hz, 450 W (depending which firmware is running)	

3 | DBBC3 Testing

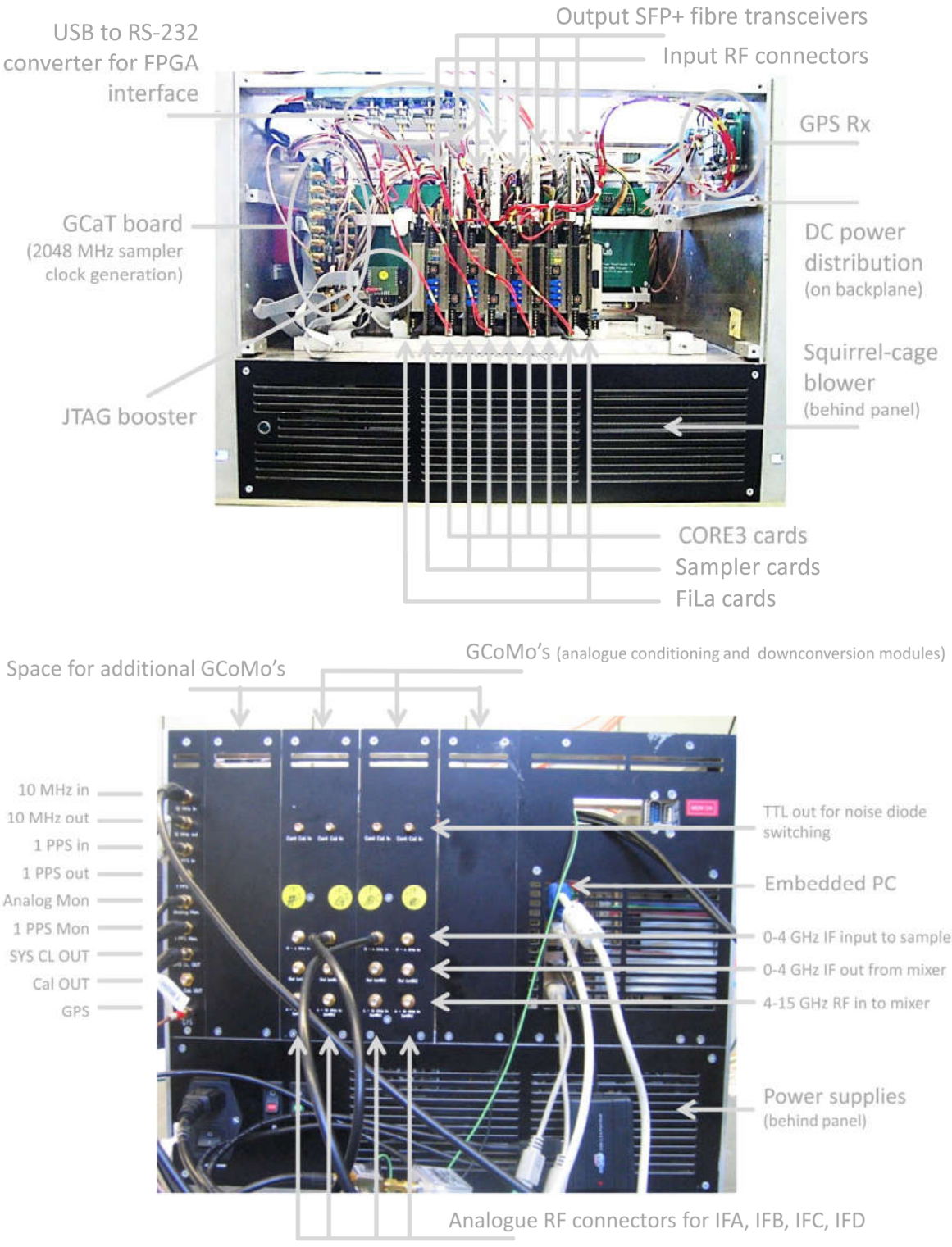


Figure: APEX DBBC3 front and back panels. Input: 4x 4 GHz IF. Output: 8x 8 Gbps VDIF streams on 10 GE fibre. Each fibre output carries 2 GHz of sampled bandwidth for compatibility with R2DBE.

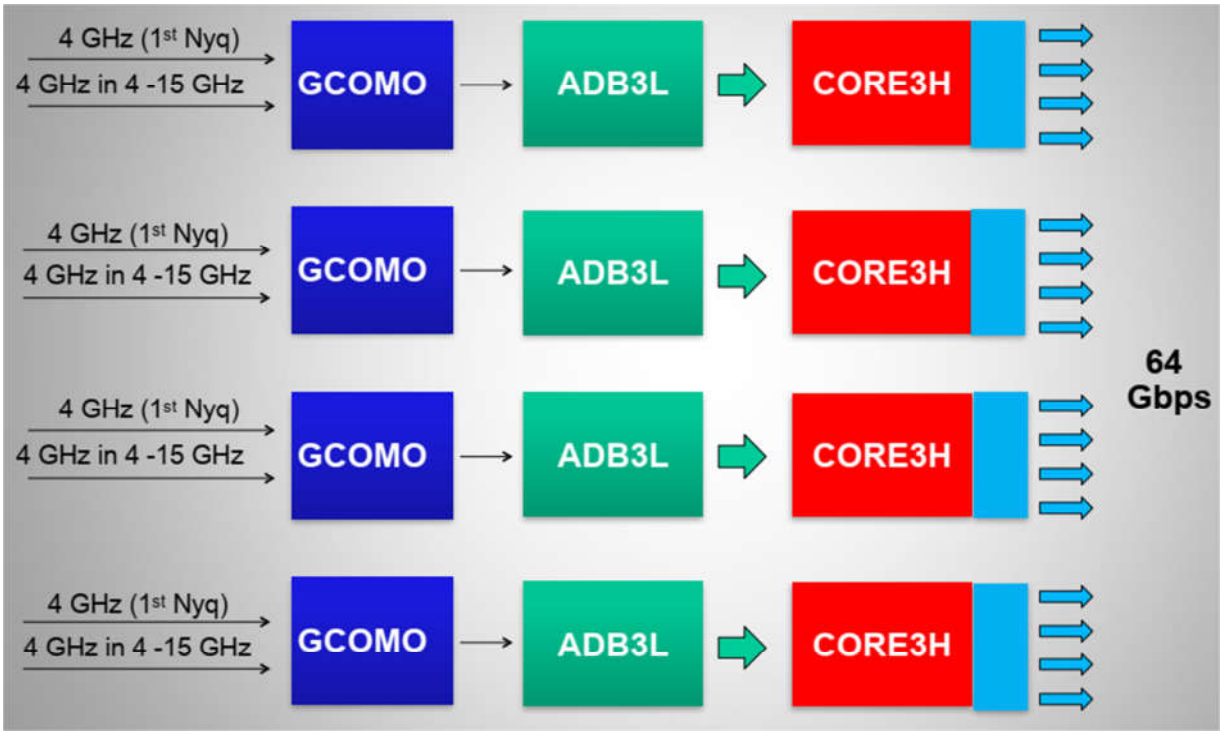


Figure: Block schematic of DBBC3L-4L4H architecture for use at APEX

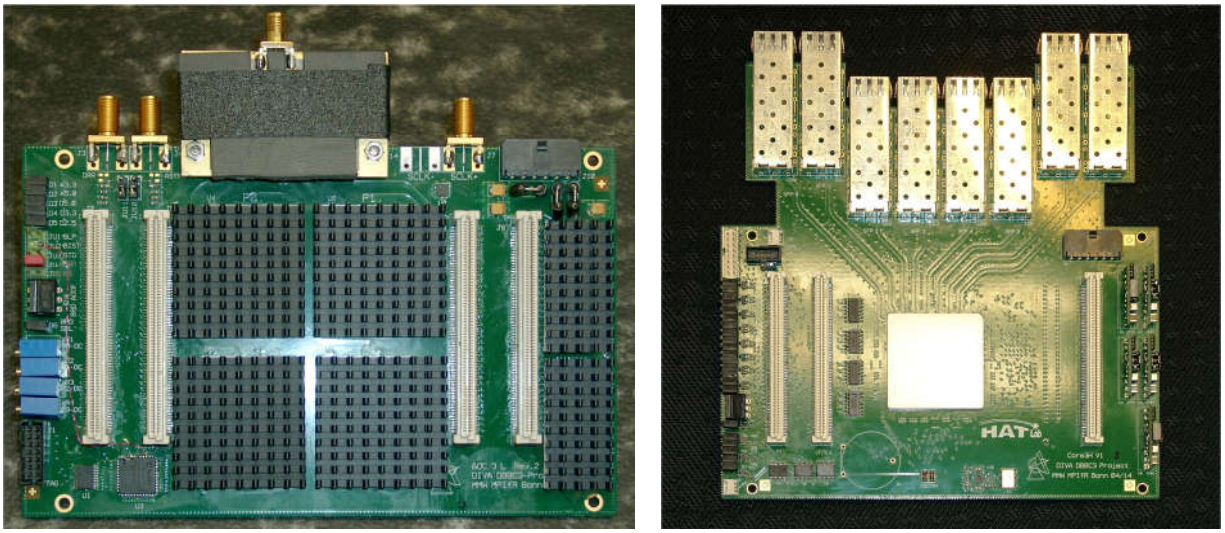


Figure: *Left:* ADB3L sampler card with phase adaptor. Number of IFs: 1 – 4, equivalent sample rate IF: 8 Gsps, instantaneous bandwidth: 4 GHz, sampling depth: 10 bit, real/complex sampling, compatible with existing DBBC. *Right:* CORE3H FPGA card – Virtex 7 FPGA, input bus HSI and HSI2, input 8-10 bit depth, 1x 4 GHz, 2x 2 GHz, 4x 1 GHz, max output: 8x 10 GE SFP+, inter-board bus: 8 input 10 GE SFP+, compatible with existing DBBC environment.

Firmware:

DSC (direct sampling):

- 0-4 GHz bandwidth direct sampled
- 4x 4 Gbps streams, one from each sampler quadrant — operational
- 2x 8 Gbps streams (implemented but not thoroughly tested) — in progress
- Data needs re-interleaving in post-processing

OCT1:

- Samples the full 0-4 GHz IF input band
- Digital filter selects a band using 32-tap FIR filters
- 0-2 GHz, 2-4 GHz — operational
- 0-1, 1-2, 2-3, 3-4 GHz — operational
- 0.5-1.0, 1.0-1.5, … , 3.5-4.0 GHz — operational

OCT2 (dual octopus mode):

- Two filters as for OCT1 at the same time per IF — operational
- Re-interleaves 2 sampler core streams on CORE3 for standard VDIF output, no correlator pre-processing
- EHT compatibility uses 2x 2 GHz streams per 4 GHz IF band input — operational

DDC-L (legacy digital downconverter mode):

- 16 BBCs (U & L) select tunable sub-bands within 4 GHz IF input per CORE3H — operational
- 32 bands tunable to simulate PFB — operational
- Bandwidth selectable with between 1 MHz and 64 MHz per sub-band (128 MHz is in test)
- Continuous cal TTL output and synchronous total power detection in firmware for T_{sys} measurement

DDC-V (VGOS mode):

- Has broader video filters with steeper flanks than DDC-L
- 12 BBCs (U & L) select tunable sub-bands within 4 GHz IF input per CORE3H — operational
- 24 bands tunable 32 MHz PFB block in 0-4 GHz — operational
- 16 BBCs (U & L) select tunable sub-bands within 4 GHz IF input per CORE3H — in progress
- 32 bands tunable 32 MHz PFB block in 0-4 GHz — in progress

PFB (polyphase filterbank):

- Not needed since DDC can simulate PFB by placing many DDCs next to each other.

Test Procedures

Setup

Provide 10 MHz, 1 PPS, GPS, noise input, tone input

1 Timing Stability

1 Monitor 1 PPS output from firmware vs 1 PPS input to detect cycle slips
2 Clock synthesizer stability
3 Measure system phase stability end-to-end
4 Verify UTC timestamp in VDIF header
5 Check for delay jumps in recording

2 Analogue Input Components

1 IF conditioning module characteristics
2 Headroom
3 Mixer LO power requirement for downconversion
4 Total system bandpass characterization
5 Noise figure

3 Digital Transmission Integrity and Processing Correctness

1 Examine state counts of 8 bits from sampler
2 Examine state counts of 2 bits after thresholding
3 Examine 1 PPS rise time
4 Verify total power spectrum clean of artifacts
5 Verify 8 Gbps correct transmission
6 Verify OCT-D filter shape
7 Verify VDIF packet stream correctly formatted, no gaps, in time order, no stream mixing

4 Reliability

1 Cooling
2 Sustained recording test for infrequent errors.

5 Zero-Baseline Test

1 Check analogue correlation coefficient from noise source splitting
2 DBBC3 – DBBC3 Digital Correlation Coefficient for Partially Correlated Noise
3 DBBC3 – R2DBE Digital Correlation Coefficient for 100 % Correlated Noise

6 On-Sky Fringe Test

1 Kashima – Onsala Test

1 Timing Stability

1 Monitor 1 PPS Output from Firmware vs 1 PPS Input to Detect Cycle Slips

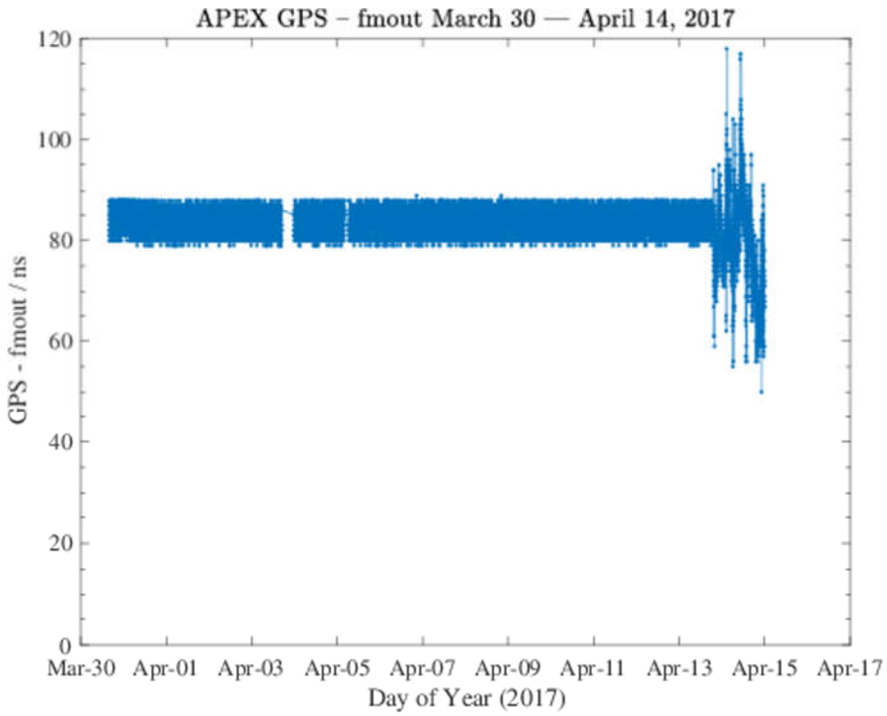


Figure: GPS-FMOUT for APEX DBBC3 during April 2017 EHT run shows no cycle slips over 11 days; a 10 MHz slip would make 100 ns step. On April 13 the counter was recabled to the R2DBE FMOUT.

2 Clock Synthesizer Stability

Clock Examination on Spectrum Analyzer

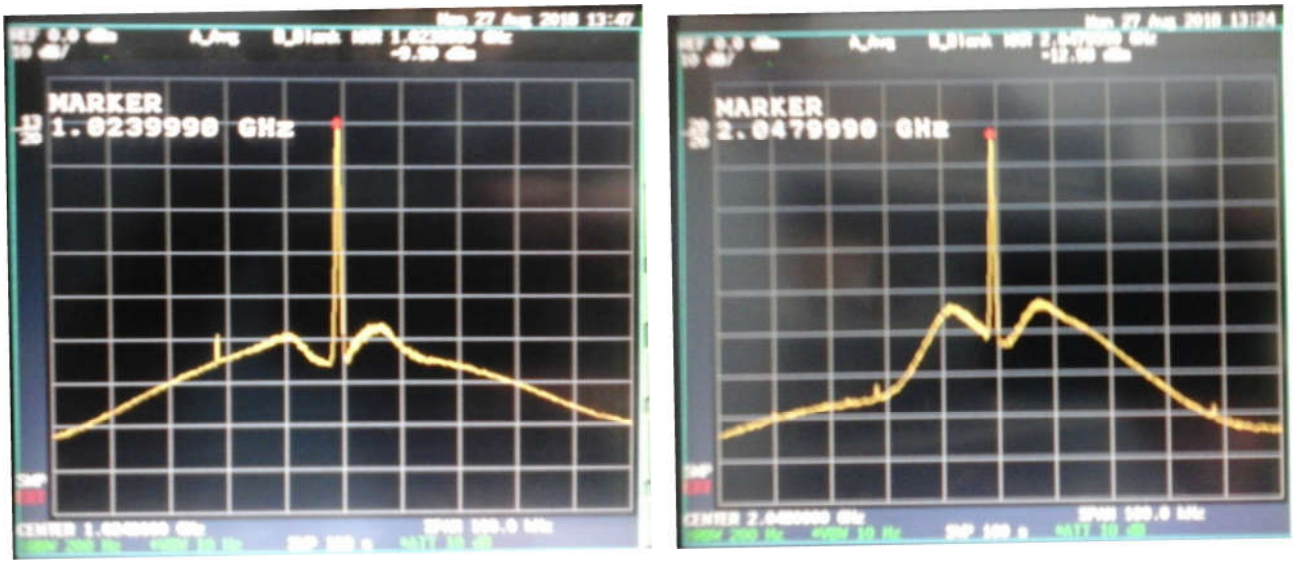


Figure: Sampler clock from synthesizer, on SYS CL OUT from DBBC3, locked to 10 MHz ref, shown at 200 Hz RBW, 100 kHz span, ref level = 0 dBm, 10 dB/div. *Left:* synthesizer set to 1024 MHz. *Right:* synthesizer set to 2048 MHz as would be used for EHT observations.

Phase Noise Analysis:

Offset	*SSB power*	*SSB power relative to carrier*	*Manufacturer spec LMX2531 @ 2089 MHz*	*Note*
0 Hz	-12 dBm	0 dBc/Hz		
1 kHz	-62 dBm / 200 Hz	-73 dBc/Hz		
10 kHz	-55 dBm / 200 Hz	-66 dBc/Hz	-87 dBc/Hz	21 dB worse than spec
30 kHz	-74 dBm / 200 Hz	-85 dBc/Hz		
40 kHz	-82 dBm / 200 Hz	-93 dBc/Hz		
100 kHz	-85 dBm / 200 Hz	-96 dBc/Hz	-113 dBc/Hz	17 dB worse than spec

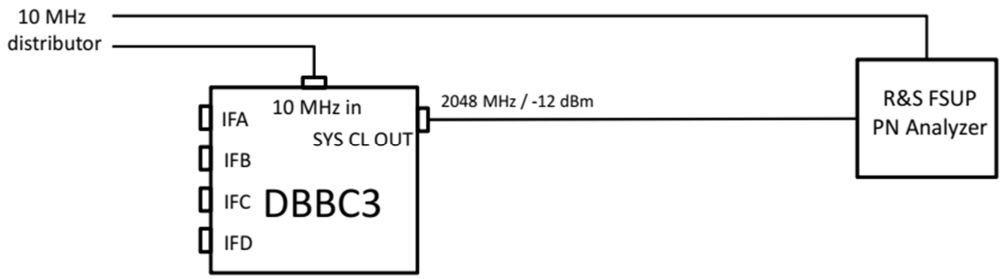
Integrating these SSB power measurements over frequency relative to the carrier gives random phase jitter of 5.3 ps = **3.9° RMS over 1 kHz to 100 kHz** using the calculator at
`https://www.jitterlabs.com/apps/pncalc/pncalc.html`

This phase noise is a bit high, especially since it does not include the phase noise closer than 1 kHz to the carrier where the dominant power is usually located. To measure the close-in phase noise one needs an FFT phase noise analyzer. The rms phase jitter of 3.9° corresponds to coherence of 0.9954, so the phase noise contribution over 1 kHz to 100 kHz produces minimal loss.

Clock Examination with an FFT Phase Noise Analyzer

Measurement Setup

Examine 2048 MHz clock from DBBC3 on Rohde & Schwarz FSUP phase noise analyzer.
Analyzer makes automatic analysis 1 Hz to 30 MHz, integrates the total power over the band and takes the ratio to the carrier power, and expresses the result as rms degrees variation.



Results

See plots on next page

Phase Noise Analysis at 2048 MHz:

Offset	*SSB power relative to carrier at 2048 MHz*	*Manufacturer spec LMX2531 @ 2089 MHz*	*Note*
1 Hz	0 dBc/Hz		
10 Hz	-47 dBc/Hz		Extreme slope; -47 dB/decade
100 Hz	-73 dBc/Hz		
1 kHz	-73 dBc/Hz		
10 kHz	-73 dBc/Hz	-87 dBc/Hz	14 dB worse than spec
100 kHz	-114 dBc/Hz	-113 dBc/Hz	on spec

The close-in phase noise (1 Hz to 10 Hz) is excessive, corresponding to 87° rms phase variations. This would be inconsistent with getting fringes, however the DBBC3 does routinely produce fringes and the tone injection test, later, showed good phase stability.

Phase Noise Analysis at 1024 MHz: Configuring the DBBC3 synthesizer to 1024 MHz yielded much lower phase noise, corresponding to 0.8° rms at 1024 MHz.

Check Analyzer at 2048 MHz on a Lab Synthesizer: Providing 2048 MHz from the Wiltron 6747B to the analyzer gave 2° rms at 2048 MHz; the high close-in phase noise is not intrinsic to the analyzer.

Phase Noise Analysis at 2048 MHz on a DBBC3 with Valon Synthesizer: The Onsala DBBC3 in the lab is equipped with a Valon in addition to the National Instruments synthesizer for optionally generating the 2048 MHz for internal distribution. The phase noise analyzer measured 1.8° rms at 2048 MHz when running on the Valon.

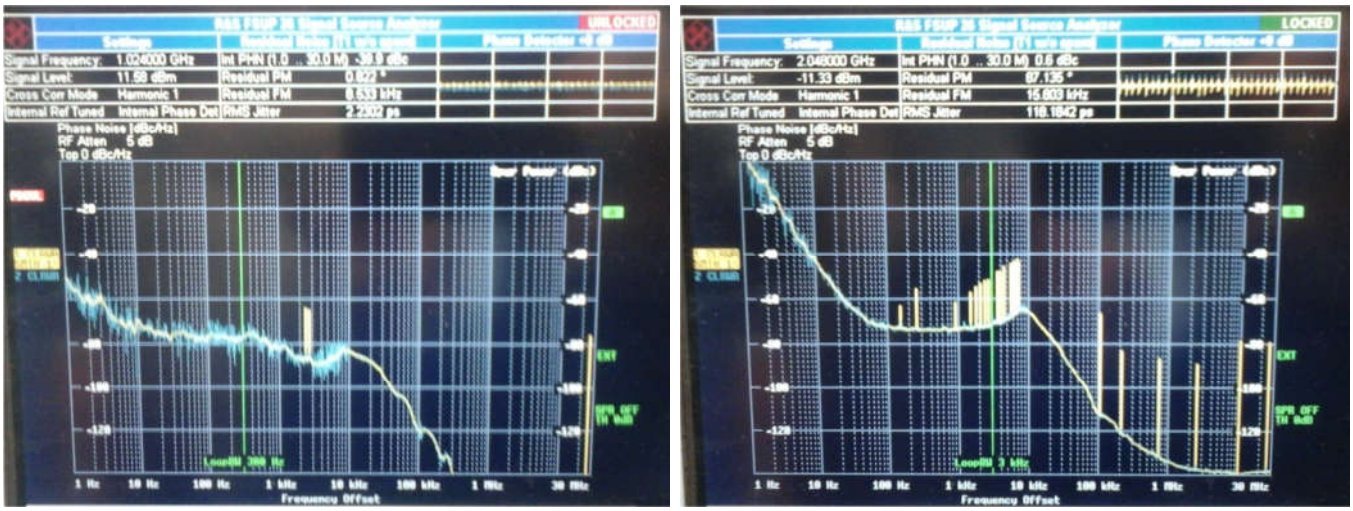


Figure: Phase noise analysis with R&S FSUP analyzer of sampler clock from synthesizer, on SYS CL OUT from APEX DBBC3. *Left:* clock synthesizer at 1024 MHz; phase noise is 0.8° rms. *Right:* clock synthesizer at 2048 MHz (National Instruments synthesizer); phase noise is 87° rms.

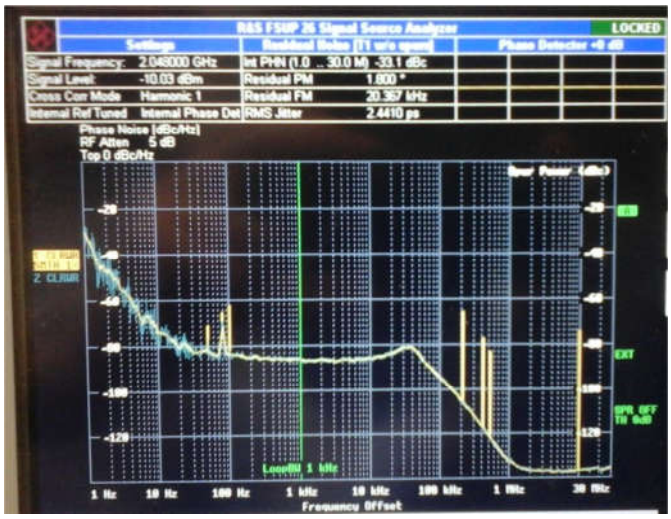


Figure: As above right but for the Onsala DBBC3, which has a Valon synthesizer in place of National Instruments for the 2048 MHz clock; phase noise is 1.8° rms.

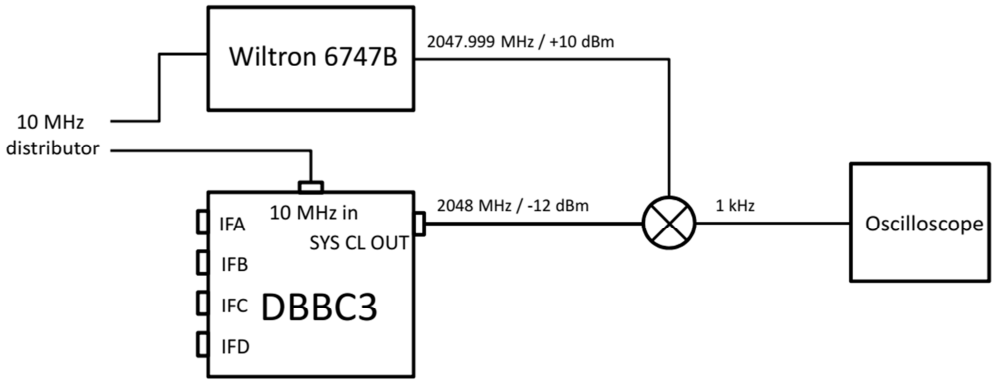
Discussion

The cause of the high phase noise measurement when using the National Instruments synthesizer was not found. The high value reported by the analyzer is inconsistent with other test results - high efficiency in zbt DBBC3-R2DBE, stable phase in tone recordings, stable fringes on-sky. We therefore inspected the synthesizer output more directly in the following test, producing a beat at 1 kHz and inspecting on an oscilloscope.

Clock Examination on Oscilloscope

Measurement Setup

Mix 2048 MHz clock from DBBC3 against 2047.999 MHz from lab synthesizer,
Examine 1 kHz beat on an oscilloscope.



Result

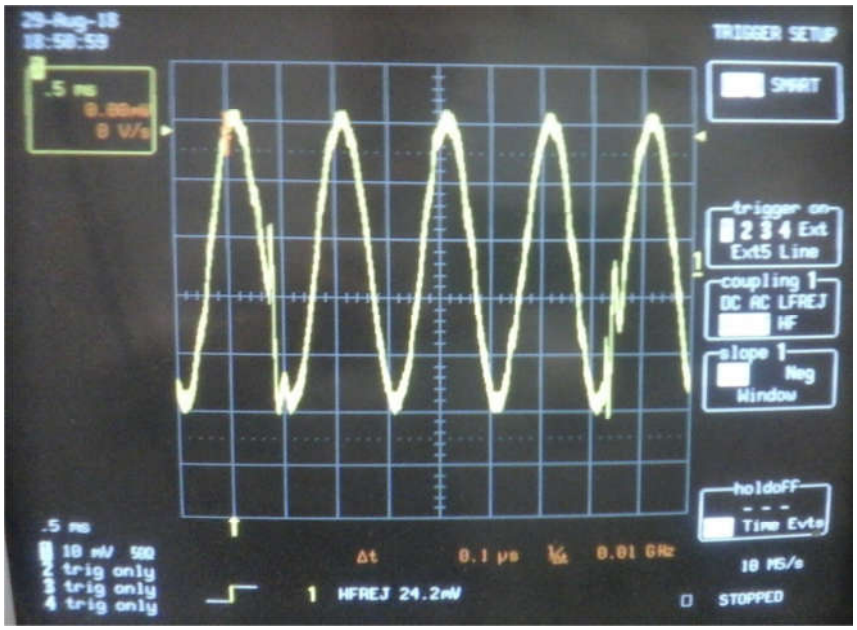


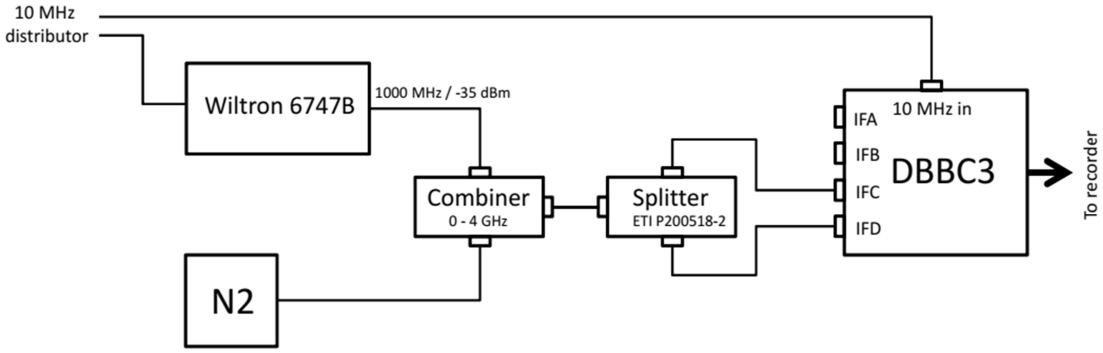
Figure: 1 kHz beat tone from mixing the DBBC3 2048 MHz internal clock against a reference synthesizer (Wiltron 6747B) at 2047.999 MHz. The difference is sensitive to relative variations in the tone phases.

The general visual impression is good stability with occasional wobbles after which the phase returns to the correct phase. This view gives a more direct impression than that of the R&S FSUP phase noise analyzer; on this signal the analyzer reported 87° rms, which is overly pessimistic.

3 Measure System Phase Stability End-to-End

Measurement Setup

Generate 1 GHz tone locked to 10 MHz, add noise, split two ways into APEX DBBC3 IFC and IFD
Record overnight on Mark 6, extract tone with m5tone.py



Analysis

20 min of tone recording was extracted in 64 h elapsed time over a weekend due to the slow run time in python. Porting to C gave a big performance improvement but the time series had massive noise excess due to leakage through the channel stop-band due to use of a rectangular window in the time domain for the FFT. A Kaiser window weighting was completed but stop-band performance was disappointing and time did not allow debugging. We analyzed the python result, using a good Kaiser window weighting implementation.

Result

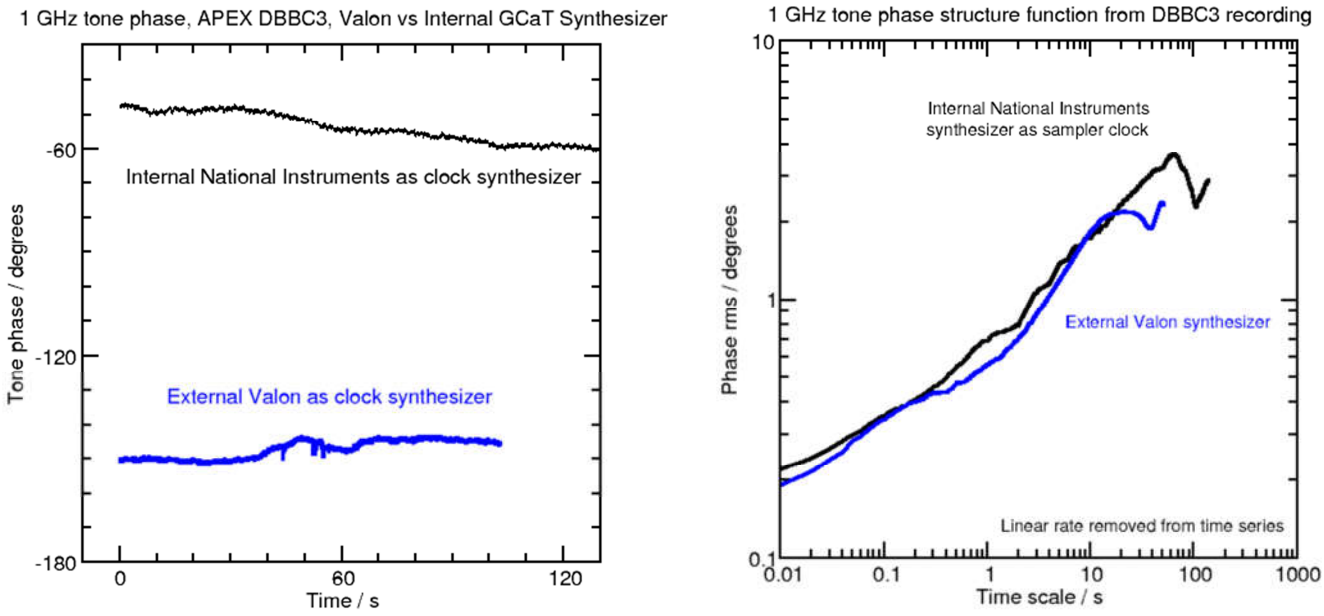


Figure: Tone phase vs time for internal and external synthesizers with the APEX DBBC3. *Left:* time series. *Right:* root-phase structure function. The peak phase RMS of 3.7° and 2.4° correspond to coherence of 0.996 and 0.998.

Discussion

The National Instruments synthesizer in the DBBC3 has similar phase noise to the Valon external synthesizer; the resulting coherence of 0.996 and 0.998 in both cases is acceptable.

The phase noise analyzer result is inconsistent with direct examination of the clock on the oscilloscope and with the end-to-end phase stability test with tone injection, thus we think the analyzer gave a spuriously high jitter estimate for causes unknown.

4 Verify UTC Timestamp in VDIF Header

Analysis with `vdiftimecheckUDP` shows the VDIF header timestamps are correctly decoded and agree with system time on the Mark 6 from NTP with differences of typically milliseconds.

5 Check for Delay Jumps in Recording

A long history of recorded data over many experiments had no delay jumps.

2 Analogue Input Components

1 IF Conditioning Module Characteristics

The DBBC3 provides the phase-locked LO and mixer for downconversion, but since the DBBC3 is a general purpose device and different telescopes have differing IF standards, additional components are required to adapt the signal levels for the DBBC3. The IF conditioning module for APEX processes four IF channels from the receiver and contains gain, impedance matching, and bandpass filter that defines a band of 5000 MHz to 9000 MHz for downconversion. The input signal is 4-12 GHz -33 dBm / 4 GHz, the output signal at baseband is 0-4 GHz -17 dBm / 4 GHz for sampling by the DBBC3. Total conversion gain is +16 dB.

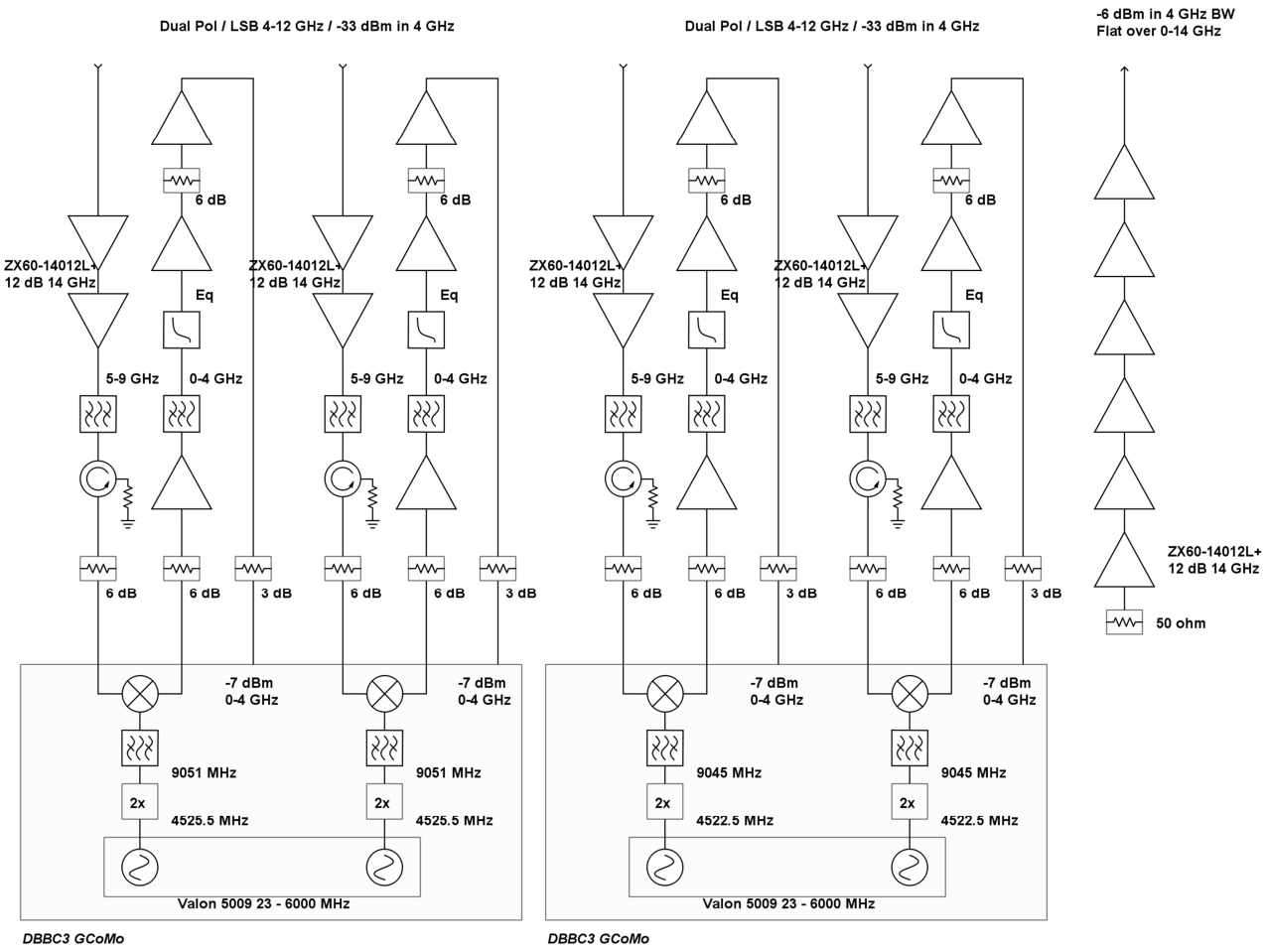


Figure: Block schematic of the IF conditioning module for using the DBBC3 at APEX with PI230. The IF conditioning module provides four channels of signal conditioning for downconversion; the LO and mixer for downconversion is in the DBBC3 analogue conditioning module.

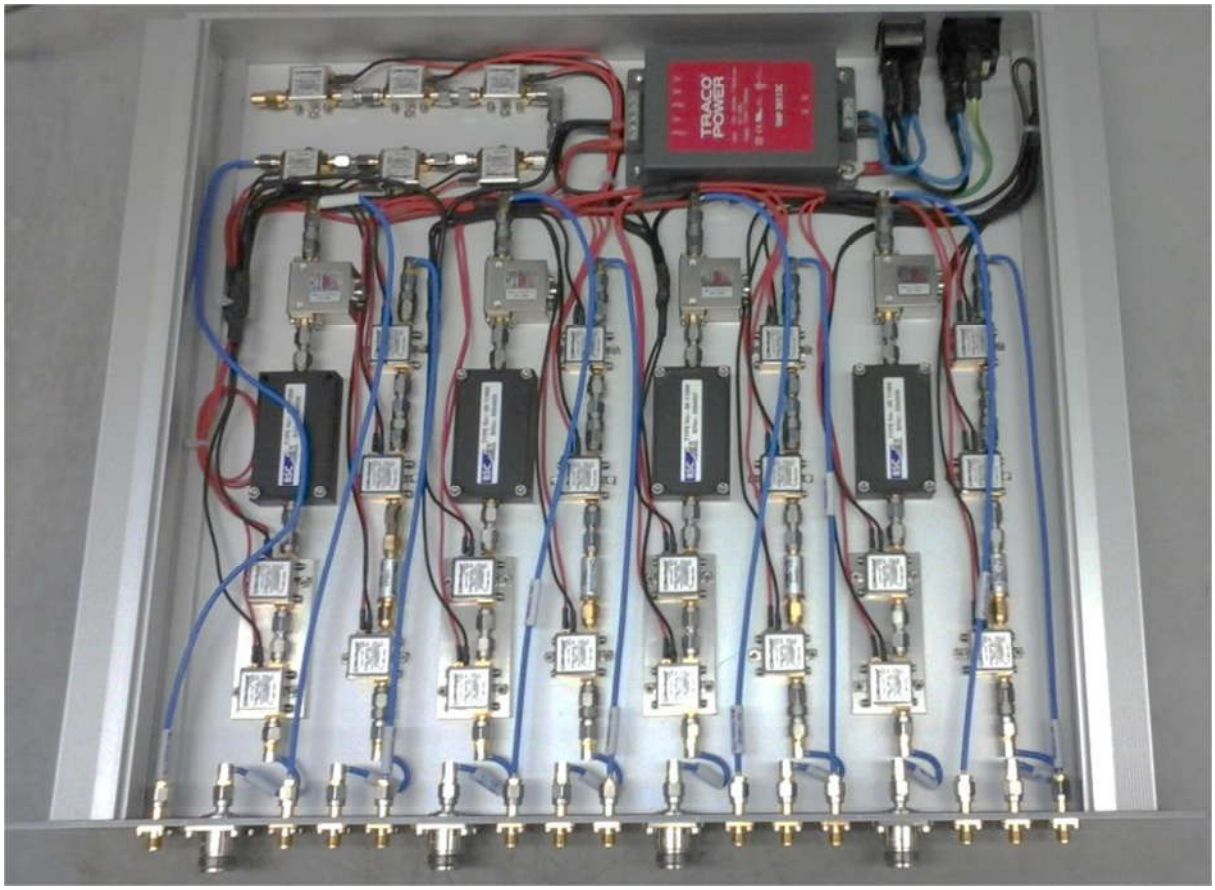
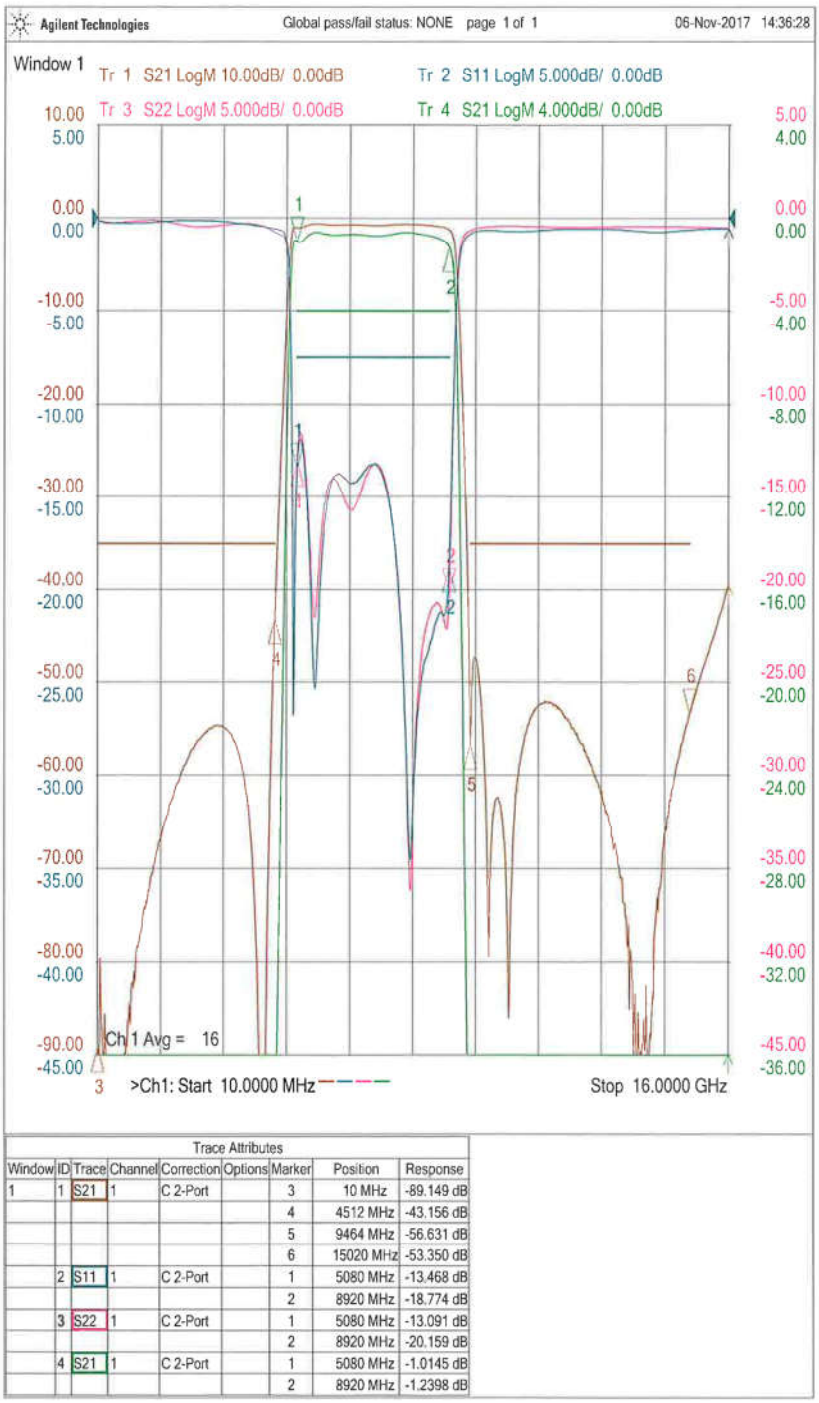


Figure: Photograph of the IF conditioning module for the DBBC3 with PI230 at APEX as shown in the block schematic in the previous figure. It provides four channels of analogue conditioning with gain, filtering, and impedance matching at 4-12 GHz before downconversion and 0-4 GHz after downconversion. The outputs go to the DBBC3 for sampling. It contains a noise source output for testing that is flat over 0-14 GHz at -3 dBm / 4 GHz.

Table: Power Levels for IF conditioning module at APEX

Location in IF Conditioning Module	***Band***	***Power***
Input from PI230 at rack 5 instrument container	4-12 GHz	-33 dBm / 4 GHz
Output to DBBC3 mixer	5-9 GHz	-25 dBm / 4 GHz
Input from DBBC3 mixer	0-4 GHz	-30 dBm / 4 GHz
Output to DBBC3 for sampling	0-4 GHz	-17 dBm / 4 GHz
Conversion gain		+16 dB
Noise figure		5.5 dB



Trace Attributes

Window	ID	Trace	Channel	Correction	Options	Marker	Position	Response
1	1	S21	1	C 2-Port		3	10 MHz	-89.149 dB
						4	4512 MHz	-43.156 dB
						5	9464 MHz	-56.631 dB
						6	15020 MHz	-53.350 dB
	2	S11	1	C 2-Port		1	5080 MHz	-13.468 dB
						2	8920 MHz	-18.774 dB
	3	S22	1	C 2-Port		1	5080 MHz	-13.091 dB
						2	8920 MHz	-20.159 dB
	4	S21	1	C 2-Port		1	5080 MHz	-1.0145 dB
						2	8920 MHz	-1.2398 dB

BSC

Part No.	SB 11966	Operator	AM
Specification	SB11966/01	Date.	06/11/17
S/No.	55649 05	Lab.	18
Job No.	55649	NQP	

Figure: Measured filter shape for the 5-9 GHz bandpass filters in the IF conditioning module, for filter SN 55649 05. All four filters are closely matched. Filter flanks are sharp to provide good sideband rejection in the downconversion process; the LO lies at 4952 MHz or 9048 MHz for USB or LSB downconversion.

Table: 5-9 GHz bandpass filter specification and measured performance

Parameter	*Frequency*	*Specification*	*Actual*
Passband insertion loss	5100.0 – 8900.0 MHz	-4.0 dB Max	-1.2 dB
Passband return loss	5100.0 – 8900.0 MHz	-6.95 dB Min	-11.8 dB
Stopband rejection	DC – 4500.0 MHz	-35.0 dB Min	-45.1 dB
Stopband rejection	9500.0 MHz – 15000.0 MHz	-35.0 dB Min	-52.2 dB
Rejection at lower band edge	4952 MHz		-2.0 dB
Rolloff at lower band edge	4952 MHz		106 dB/GHz
Rejection at upper band edge	9048 MHz		-2.0 dB
Rolloff at upper band edge	9048 MHz		140 dB/GHz

2 Headroom

Gain compression must be avoided in the analogue path to avoid signal distortion, and the design rule used in the analogue IF conditioning was that signal power levels should be 15 dB or more below than the 1 dB compression point for each component in the chain. The resulting power plan for the APEX IF conditioning is illustrated in the following figure.

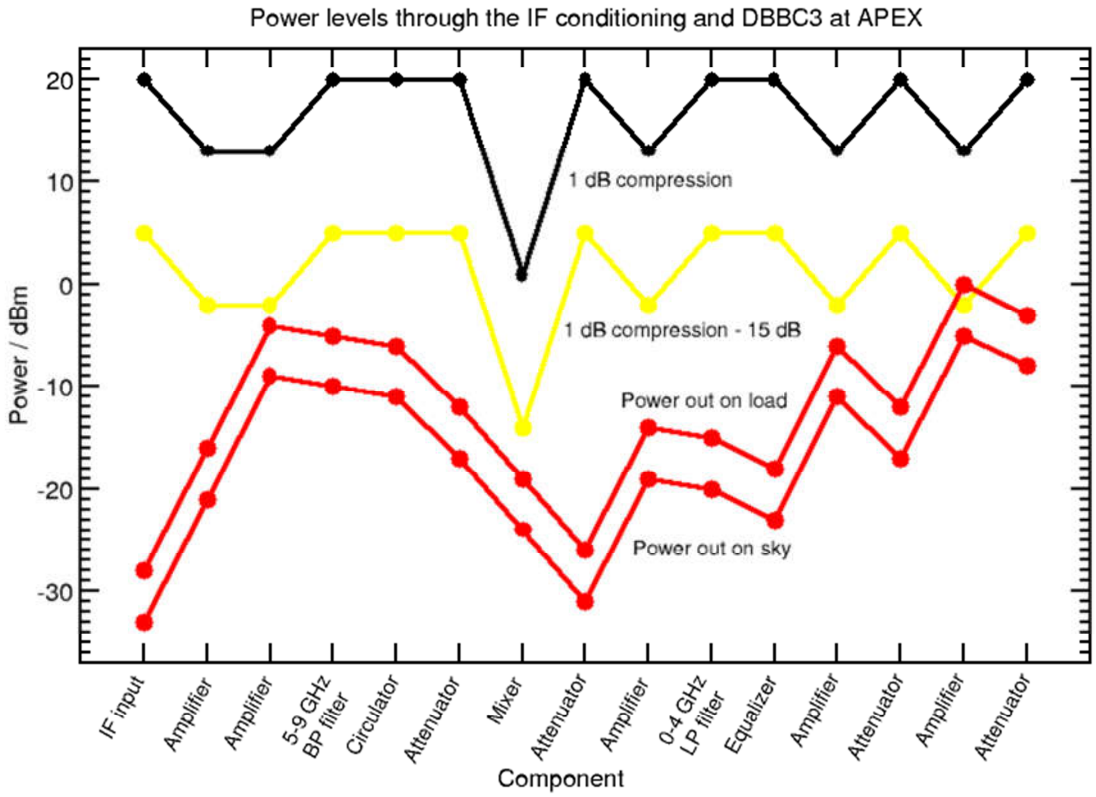


Figure: Power plan in the analogue conditioning for downconversion with the DBBC3 at APEX.

The power plan is always at least 15 dB below the 1 dB compression point except for the output of the last amplifier when observing the calibration load, at which point the headroom is 13 dB to the 1 dB compression point. This compromise was struck to obtain the required power of -7 dBm into the DBBC3 (requirement was later relaxed to -20 ± 9 dBm input power) when on sky and allow for a 3 dB attenuator after the amplifier for impedance matching and to provide a load for the last amplifier when cables are disconnected.

Linearity was verified by varying the input IF noise power and measuring the output baseband power from the GCoMo at 0-4 GHz at the input to the sampler card.

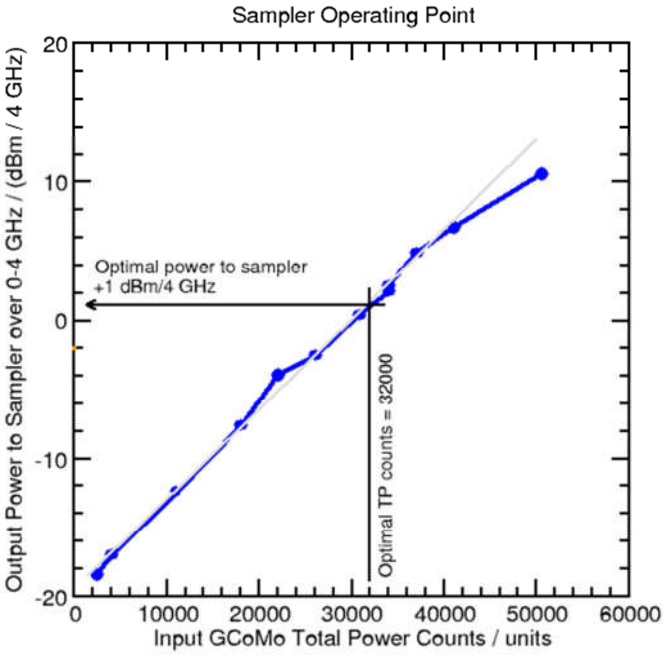


Figure: Optimal efficiency with the DBBC3 with power level adjusted in the GCoMo to give total power counts of 32000 on a range of 0 to 65536, which corresponds to an optimal power level to the sampler of +1 dBm / 4 GHz. Here we show the transfer curve between total power counts and power level to the sampler, traced by measuring the output power and total power counts while varying the digital input attenuation on an input noise source.

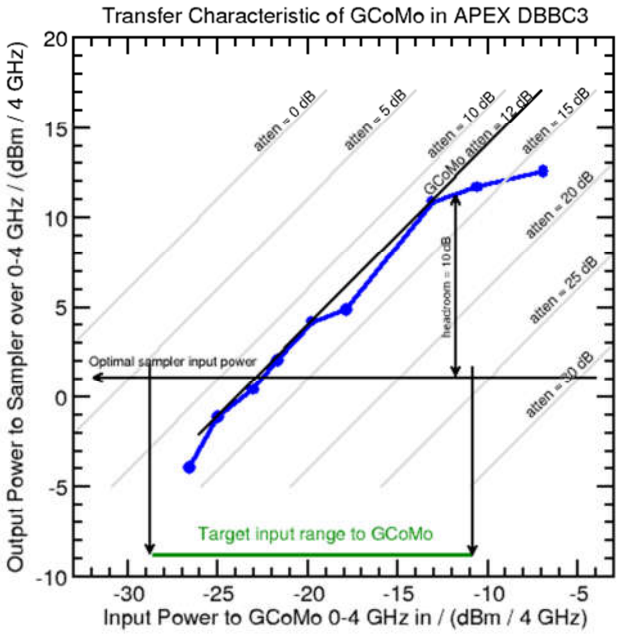


Figure: *Blue line:* Transfer characteristic of the APEX DBBC3 GCoMo, measured by varying input 0-4 GHz noise power for fixed attenuation of 12 dB and measuring the output power to the sampler. Gain compression occurs for output power above +11 dBm/4 GHz. For an optimal sampler input power of +1 dBm/4 GHz we have 10 dB of headroom before compression of the final stage amplifier. *Grey diagonal lines:* show the transfer characteristic expected for other settings of the digital attenuator in the GCoMo. The input power range that can be compensated to produce +1 dBm/4 GHz at the sampler with > 6 dB reserve attenuation is (-20 ± 9) dBm/4 GHz.

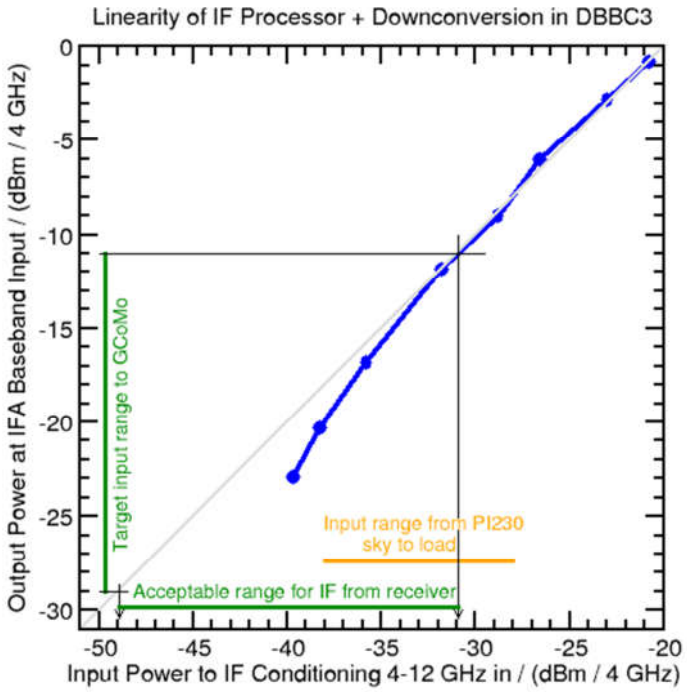


Figure: Linearity of analogue path from IF conditioning input at 4-12 GHz through DBBC3 downconversion to DBBC3 baseband input 0-4 GHz. The operating input power range for PI230 receiver at APEX is shown in orange, which lies in the linear range of the analogue processing. The high-power end shows linearity up to 0 dBm/4 GHz without signs of gain compression. The 1 dB compression point of the amplifiers used in the IF conditioning (ZX60-14012L-S) is specified as +11 dBm. The turn-down at low power is due to the noise floor of the spectrum analyzer, which added noise power to the input power to cause the input to be over-estimated.

3 Mixer LO Power Requirement for Downconversion

For efficient downconversion the mixer in the DBBC3 GCoMo must be driven into saturation with sufficient LO power. The Valon synthesizer in the GCoMo has a fixed output power that is attenuated internally by a digital attenuator, whose optimal setting we determined experimentally by injecting a tone in the RF port, stepwise reducing the LO attenuator setting, and looking when the output IF tone power reached saturation. The optimal setting is a little into the saturated region and should correspond to +7 dBm LO power.

Mixer type: Mini-Circuits ZX05-153+
LO power: +7 dBm, RF frequency range: 3400 MHz – 15000 MHz

LO synthesizer type: Valon 5009 / frequency: 23 MHz to 6000 MHz / frequency-doubled before mixer LO port

Measurement Setup:

Apply input tone at 7000 MHz / -20 dBm to 4-12 GHz IF input to GCoMo

Set Valon 5009 in GCoMo to 4000 MHz x2 = 8000 MHz

Vary att setting of Valon to vary LO power to mixer, measure tone output power at 1000 MHz.

Result:

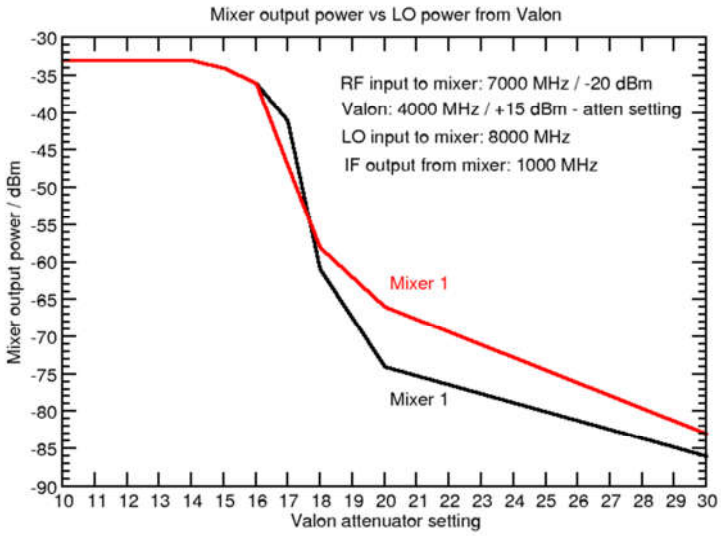


Figure: Output tone power from mixer vs LO power attenuation setting, for two mixers in IFA and IFB.

The output tone power reached saturation when the LO attenuation was reduced to 14 dB or less, so we operate in this saturated region with the Valon att parameter set to att = 13.

4 Total System Bandpass Characterization

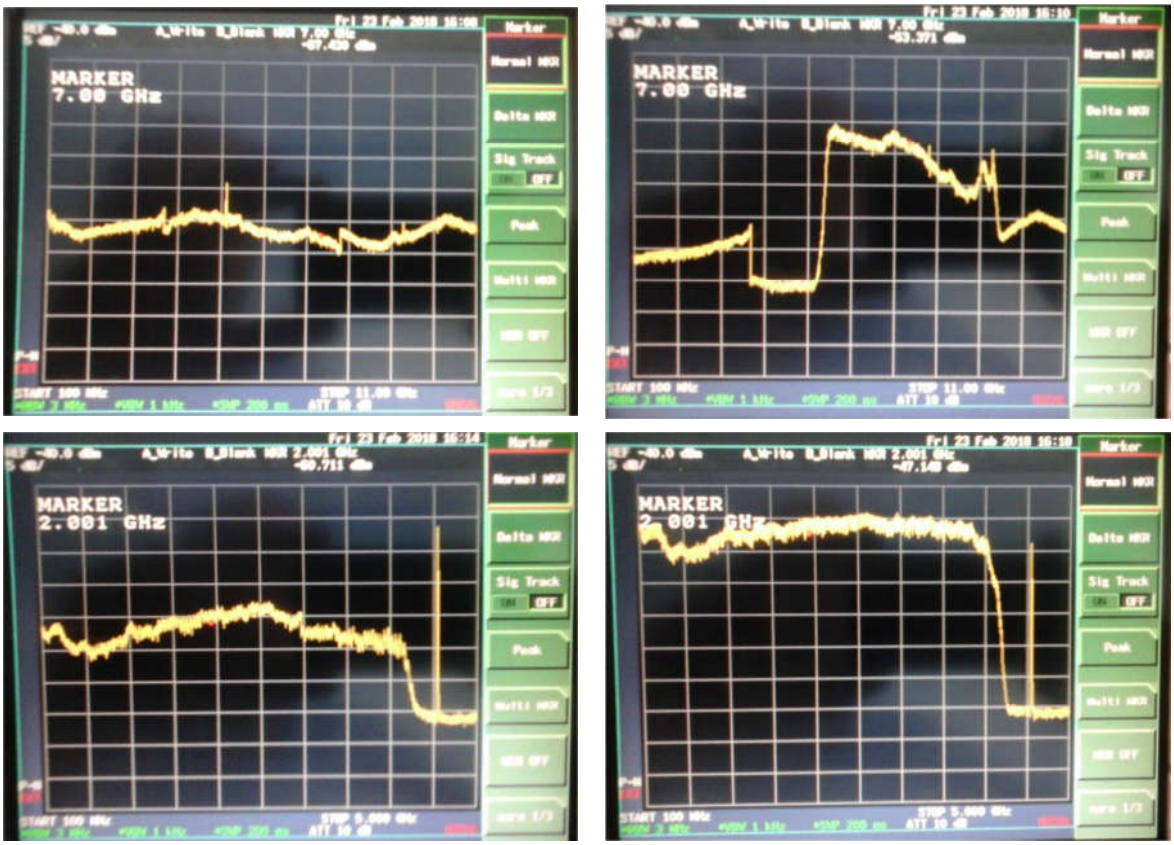


Figure: *Top left:* Noise source output (100 MHz to 11 GHz, 5 dB/div. Steps at 3 GHz and 8 GHz are in spectrum analyzer). *Top right:* noise source after passing through 5-9 GJz BPF and gain section of IF conditioning module, measured at output to DBBC3 GCoMo for downconversion (step at 3 GHz is in spectrum analyzer, high noise floor above 9 GHz is noise floor of spectrum analyzer). Bandpass filter is seen with sharp flanks at 5 GHz and 9 GHz. Band slope of -10 dB/4 GHz. Settings: 100 MHz to 11 GHz, 5 dB/div. *Bottom left:* GCoMo 0-4 GHz output after downconversion with LO at 9048 MHz. Settings: 100 MHz to 5 GHz, 5 dB/div. *Bottom right:* 0-4 GHz after gain and 0-4 GHz low-pass filtering, measured at IF conditioning module 0-4 GHz output to DBBC3 GCoMo for sampling. Settings: 100 MHz to 5 GHz, 5 dB/div.

5 Noise Figure

The system noise contribution by the DBBC3 to the IF signal from the receiver is determined principally by the first amplifier in the analogue conditioning module.

Amplifier type: Mini Circuits ZX60-14012L+
Noise figure: 5.5 dB typical over 10 MHz to 14000 MHz (Mini Circuits product data sheet)

The conversion between noise figure and noise temperature is given by:

$$Noise\ temperature\ (K) = T_{ref}\left(10^{\frac{NF(dB)}{10}} - 1\right)$$

For NF = 5.5 dB and T_{ref} = 300 K ambient temperature, the noise temperature, $\boldsymbol{T_{noise}}$ **= 765 K**.

Compare this to the IF signal level at the 4-12 GHz input from PI230:

IF signal power = -33 dBm / 4 GHz
= 1.3×10^{-16} W/Hz

Convert from IF power to equivalent noise temperature, *T*, using the relation for Johnson noise from a resistor, *P* = *kTB*, where *k* is Boltzmann's constant, *B* is the bandwidth, here 1 Hz. For *P* being the IF signal power then this yields $\boldsymbol{T_{signal} = 9 \times 10^6}$ **K**. Thus the signal to noise ratio = 9×10^6 K / 765 K = 11800, and so noise from the first amplifier in the IF conditioning for the DBBC3 is negligible compared to the input IF signal power; the DBBC3 system contributes very little noise.

3 Digital Transmission Integrity

1 Examine State Counts of 8 Bits from Sampler

Done during assembly. Checks for lines open or tied high or low. Result ok.

2 Examine State Counts of 2 bits after Thresholding

Done during every test, values after thresholding typically 16 % 34 % 34 % 16 % as required for best efficiency.

3 Examine 1 PPS rise time

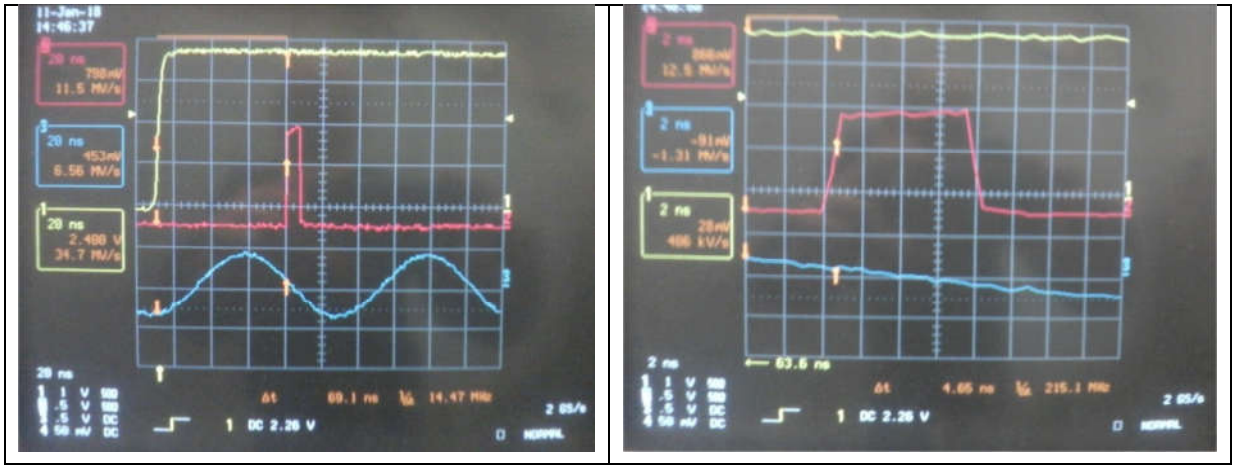


Figure: 1 PPS input (yellow trace), 1 PPS Mon output from DBBC3 firmware (red trace), 10 MHz input (blue trace), at 20 ns/div (left) and 2 ns/div (right). 1 PPS rise time is 0.6 ns, no ringing. Clean and matched. Delay between 1 PPS in and 1 PPS out is 68 ns.

3 Verify Total Power Spectrum Clean of Artifacts

Done, see bandpass figures in the next section. After ADC calibration the DSC mode 0-4 GHz band and OCT-D 0-2 GHz and 2-4 GHz autocorrelation passbands are clean of spurious lines. Tone injection shows tone at expected frequency and the rest of the band clean; no intermodulation products. By offsetting ADC phase or mis-calibrating the FPGA clock timing one can generate intermods from the tone that fill the band, which verifies the test is sensitive.

4 Verify Correct Transmission at 8 Gbps

Done. Analysis of recorded VDIF shows no missing packets, no out of order packets, ADC thread re-interleaving done correctly. Data validity is high on DiFX/fourfit.

5 Verify OCT-D filter shape

The OCT-D firmware digitally filters to two 2 GHz bands from the sampled 0-4 GHz IF for compatibility with R2DBE using two 32-tap convolutional FIR filters. The filter coefficients can be easily and dynamically modified without recompiling the firmware and example plots of the filter shapes achievable are shown below. The 0-2 GHz is a low-pass filter, while the 2-4 GHz is a band-pass filter.

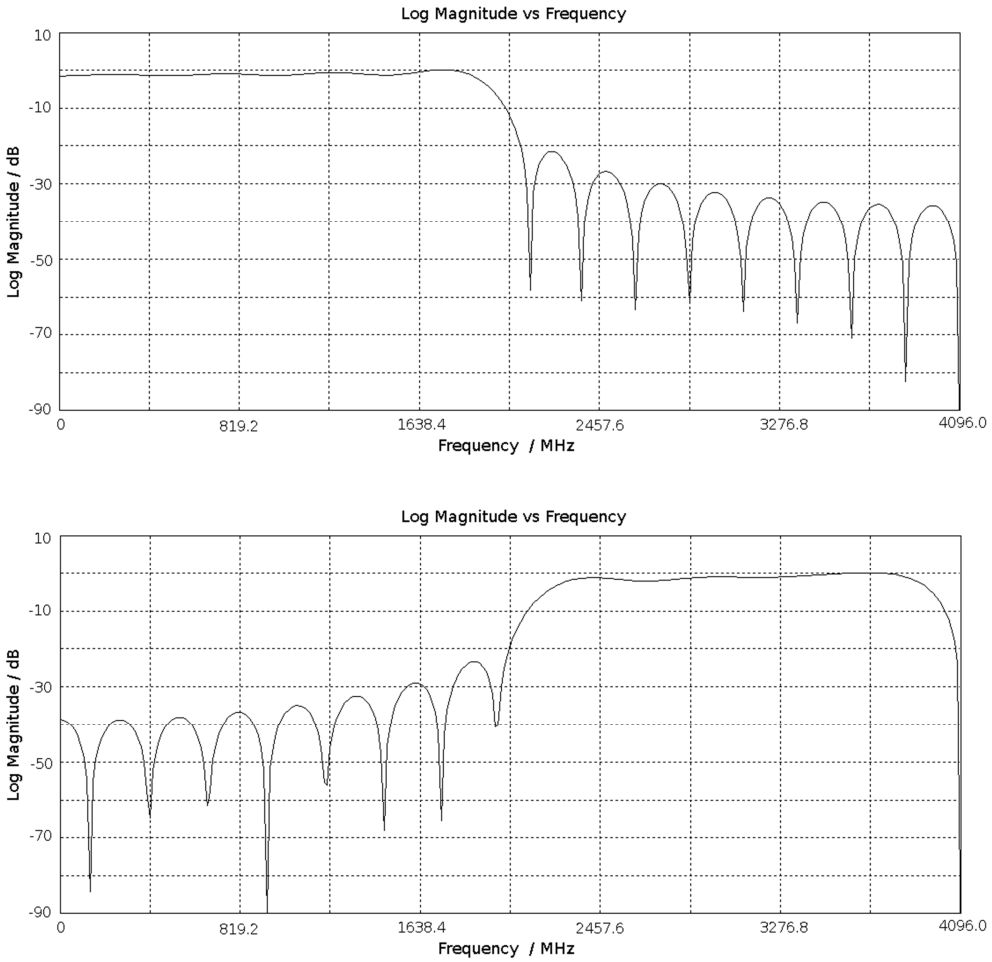


Figure: Calculated OCT-D filter shapes are shown. These digitalfilters follow after the sampler and before subsequent processing to select two 2 GHz bands from the sampled 4 GHz band for R2DBE compatibility. *Top:* 0-2 GHz low-pass filter. *Bottom:* 2-4 GHz bandpass filter. Both are 32-tap convolutional FIR filters operating on the 8 Gsps 8-bit time series.

Table: OCT-D digital filter simulated performance measured from plots above

Parameter	*0-2 GHz LP filter*	*2-4 GHz BP filter*
Passband p-p ripple	1.8 dB	2.1 dB
3 dB bandwidth	0 - 1920 MHz	2270 – 3930 MHz
Stopband rejection 0-1948 MHz		Better than -24 dB
Stopband rejection 2148-4096 MHz	Better than -22 dB	
Rejection at band edge at 2048 MHz	-11.9 dB	-19.2 dB
Rolloff at band edge at 2048 MHz	146 dB/GHz	112 dB/GHz
Sideband orientation	USB	LSB

The measured OCT-D filter shapes are shown below. A noise source was split to IFA and IFB 0-4 GHz baseband inputs, sampled, VDIF data were captured from the Mark 6 NIC, and an autocorrelation spectrum formed with `zerocorr`. The signal peak strength was measured from the cross correlation spectrum normalized by the autocorrelation spectra and plotted here.

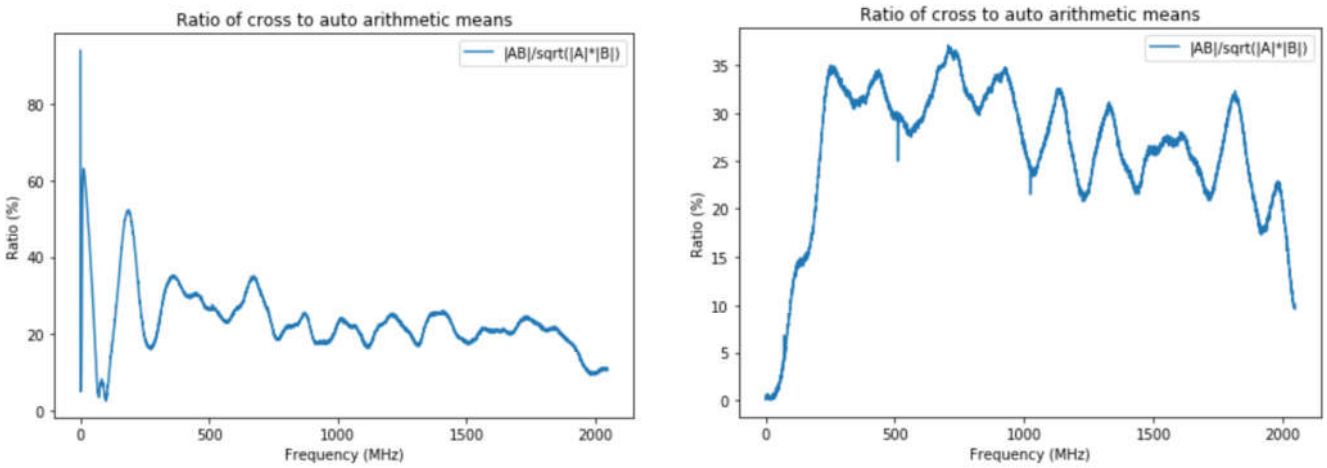


Figure: OCT filter shapes measured on a broad-band noise source and correlating with zerocorr between two Ifs. Bands are nominally 0 MHz - 2048 MHz and 2048 MHz – 4096 MHz. Filters show good rolloff, minimal response beyond band edges, some bandpass ripple indicating gain variations or mismatches; the passband ripple at the bottom of the 0-2 GHz band is not always present and might have to do with the noise source combination in this test. Tone sweep confirms 0-2 GHz band is USB, 2-4 GHz is LSB.

The measured plots look basically ok, shows good stop-band rejection. Passband ripple at the bottom of 0-2 GHz band might have to do with the analogue noise source.

6 Verify VDIF packet stream correctly formatted, no gaps, in time order, no stream mixing

Analysis with `vdifcontinuitycheck` on recorded VDIF files reports long periods with no lost frames, no frames out of order, no stream mixing. Correlation with DiFX produces high data validity and high correlation coefficients.

4 Reliability

1 Cooling

A squirrel-cage blower directs a broad airflow vertically through the FPGA and sampler boards and exhausts through the rear of the chassis cooling the embedded PC on the way. The FPGA die temperatures are monitored and typical values are shown in the following table.

Table: FPGA die temperatures at sea level in lab in Bonn

Ambient temperature	*Firmware*	*Relative power consumption*	*FPGA die temperature*
23 °C	DDC	1.1	49 °C to 51 °C
29 °C	OCT-D	1	57 °C
24 °C	OCT-D	1	49 °C to 50 °C

- Temperature limit for the FPGAs is 120 °C; industrial-grade devices are used in the DBBC3.
- Ambient temperature at APEX in the VLBI rack is typically 13° C, substantially lower than in Bonn.
- The DBBC3 has operated at APEX for two sessions without temperature issues.

Thus the die temperatures are comfortably below the limits and we do not expect cooling issues with the DBBC3.

2 Sustained Recording Test for Infrequent Errors

- Many weeks of run time on the APEX DBBC3 showed no firmware instability (eg no loss of sync, no delay jumps, no hangs). Much more run time has been accumulated counting all ten DBBC3's so far delivered for operations.
- Many hours of analysis of the output 10 GE data streams on fibre with a protocol analyzer (Teledyne LeCroy SierraNet M408) showed no errors, no packets out of order.
- Occasional bursts of data loss (up to 2 % loss) were sometimes found and was resolved by tuning configuration of Mark 6 recording software, after which no loss was seen.
- Packet loss of 25 % was found on initial recordings from the R2DBE 02:44:01:02:11 (Pico unit in Bonn for these tests), which was resolved by cleaning the SFP+ fibre transceiver modules copper connections with alcohol, after which no loss was seen.

5 Zero-Baseline Testing

1 Check Analog Correlation Coefficient from Noise Source Splitting

Measurement Setup

Split noise source to DBBC3 IFA and IFB 0-4 GHz inputs, gives nominally 100 % correlated noise
Examine GCoMo analogue output to sampler on digital oscilloscope in lab, 1 GHz BW, XY plot
Balance line lengths using trombone

Result

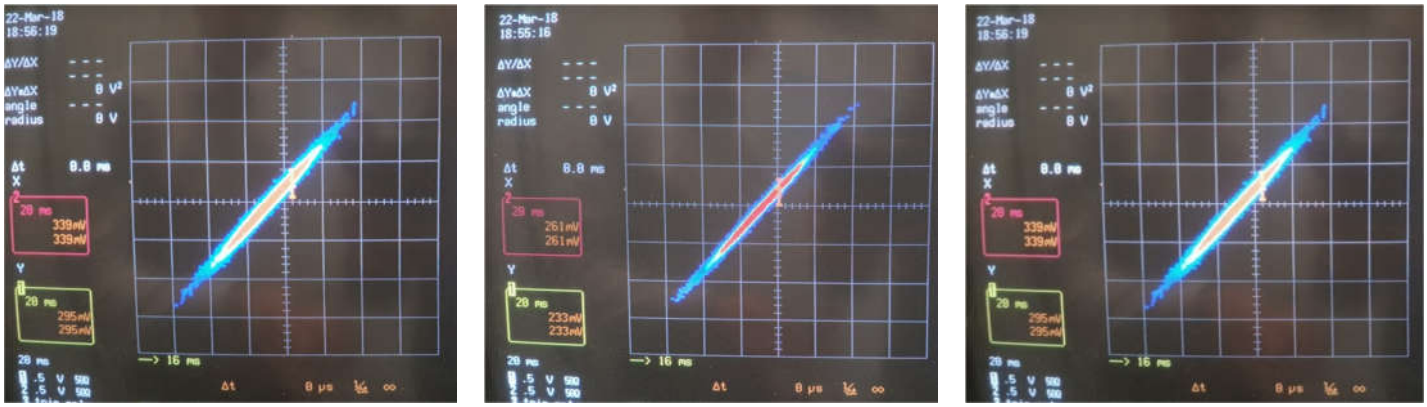


Figure: *Left to right:* Analogue correlation between GCoMo outputs IFA vs IFD, IFB vs IFD, and IFC vs IFD, all showing high correlation.

Pair	*Ellipticity*	*Correlation Coefficient (1 – ellipticity)*
IFAD	0.088	0.912
IFBD	0.077	0.923
IFCD	0.077	0.923
IFAB	0.108	0.892

Thus the analogue correlation coefficient in range 0-1 GHz bandwidth of oscilloscope is high.

Note this does not test noise correlation over the higher frequencies 1-4 GHz as these are outside the frequency range of the oscilloscope.

2 DBBC3 - DBBC3 Digital Correlation Coefficient for Partially Correlated Noise

Measurement Setup

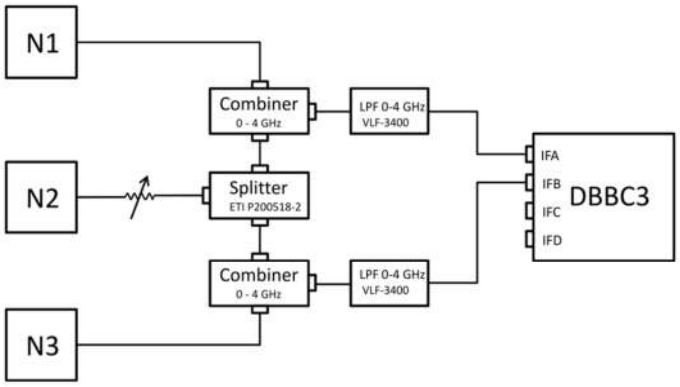


Figure: Lab setup combining three noise sources to give known input analogue coherence

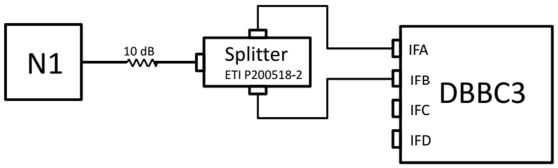


Figure: Lab setup for producing 100 % correlated noise

Data Analysis

Power was measured at combiner inputs with an Avantest R3272 spectrum analyzer digitally averaging the power over the 0-2 GHz band and converted to analogue correlation coefficient using TMS Eq 9.1 for correlation for a point source:

$$\rho_0 = \varepsilon \sqrt{\frac{T_{A1} T_{A2}}{(T_{S1} + T_{A1})(T_{S2} + T_{A2})}}$$

where T_A = antenna temperatures
T_S = system temperatures
ε = efficiency, typical systems ~ 0.5 allow for quantization and processing losses.
Use ε = 1 here to give analogue input correlation coefficient.

To measure the digital correlation coefficient: we acquired 1 s VDIF data from NIC into memory then wrote to file, correlated and fringe fit with `zerocorr`. The cross-power spectrum was normalized by the geometric mean of the autocorrelation spectra on a channel-by-channel basis. The amplitude of the fringe peak gave the digital output correlation coefficient.

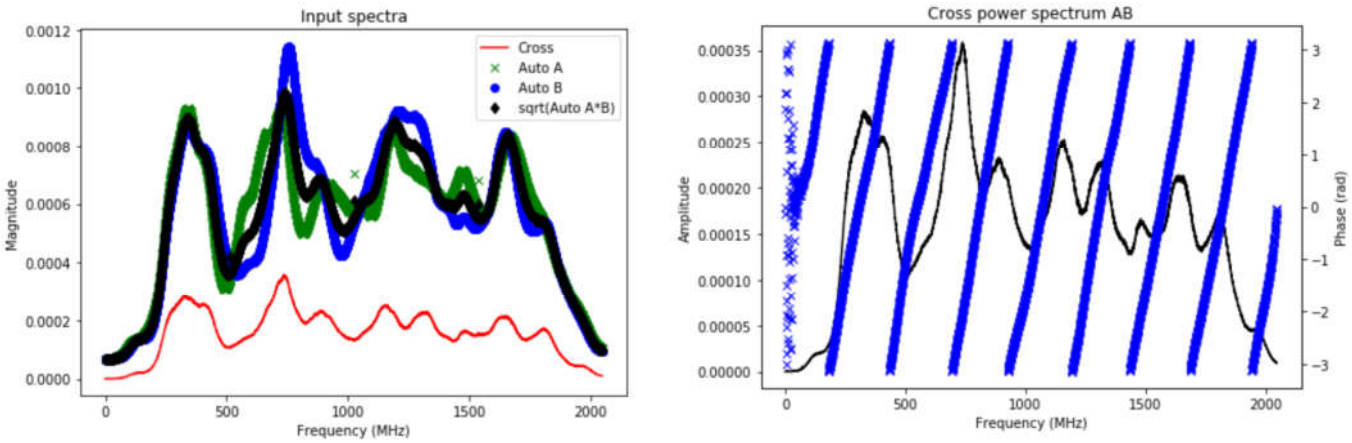


Figure: Example of digital correlation coefficient determination, for DBBC3 IFCD 2-4 GHz band with input analogue correlation of 0.336. *Left:* The cross-power spectrum (red), two auto-correlation spectra (blue and green), and the geometric mean of the autocorrelation spectra (black). *Right:* The corresponding cross-power phase vs frequency.

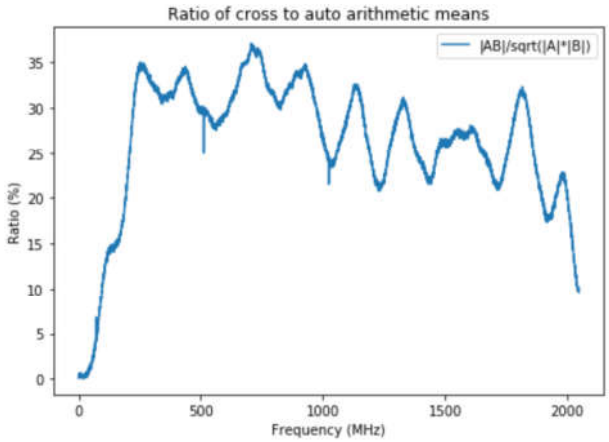


Figure: Bandpass shape for 2-4 GHz band after normalizing the cross-power spectrum (red in the previous figure) by the geometric mean of the auto-correlation spectra (black in the previous figure). The amplitude scale indicates the degree of correlation between the two DBBC3 channels. The input analogue correlation coefficient was 0.336.

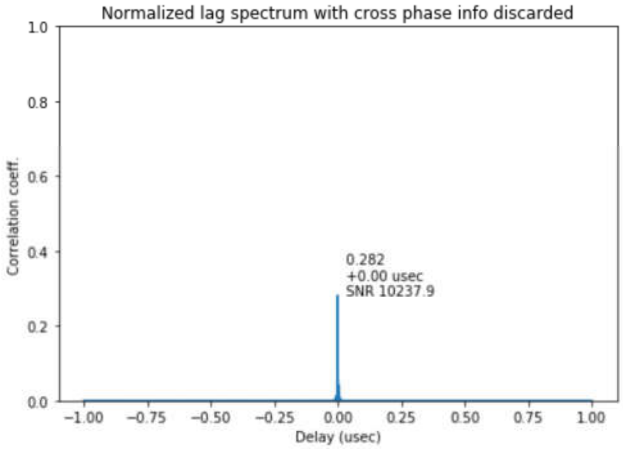


Figure: The lag spectrum after fringe fitting, including fractional-sample delay correction, giving an output digital correlation coefficient of 0.282 in this case.

Result

We varied the input analogue correlation coefficient between 0.098 and 1.0 and measured the output digital correlation coefficient between IFA and IFB, and between IFC and IFD of the DBBC3 for each case. The results are plotted below.

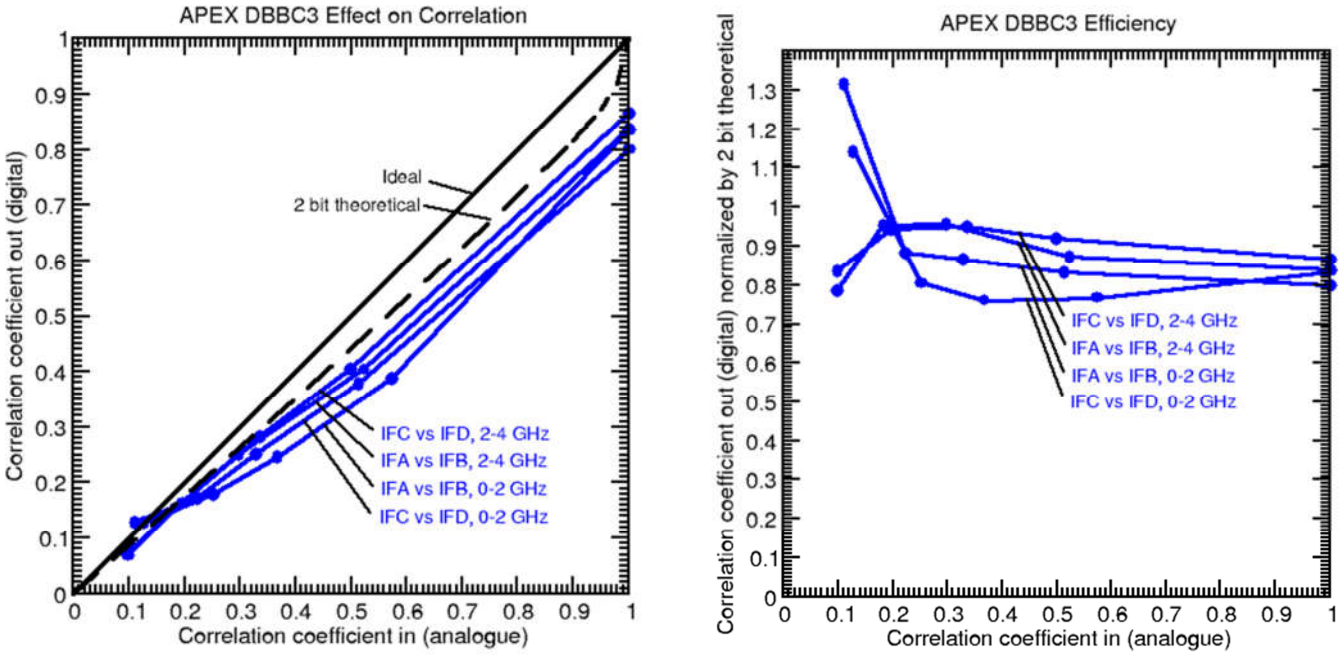


Figure: *Left:* Output vs input correlation coefficient measured in zero-baseline test between DBBC3 IFs. Dashed line for 2 bit theoretical is from Cooper (1970; AuJPh, 23, 521) Table 4 column 3. *Right:* Output correlation coefficient divided by the 2 bit theoretical value. The efficiency for a single IF as is recorded in VLBI is the square-root of the efficiency here. Target efficiency is > 0.85, actual efficiency is 0.92 to 0.98 in 2-4 GHz band after taking the square root for a single IF.

The efficiency relative to 2 bit theoretical on the zero baseline is 0.84 to 0.96 in the 2-4 GHz band cross-correlation. Here we ignore values for the lowest input correlation coefficient, which has high uncertainties due most likely to cross-coupling in the analogue combiner network. The efficiency on the zero baseline in the 0-2 GHz band is a little lower at 0.76 to 0.89, most likely due to band slope in the noise source used for the test in the 0-2 GHz band. There is scope for improvement in the 0-2 GHz filter, and, since the tap weights are loaded from text file during configuration, their later introduction is easy, however we should avoid building in bandpass of the noise source into the filter bandpass as the performance could differ with the IF band shapes at the telescope.

The efficiencies quoted here are on the zero baseline and include the losses in both IF channels. The efficiency for a single IF as recorded for VLBI is the square root of the efficiency found here on the baseline, thus the efficiency measured for a single IF is 87 % to 94 % in the 0-2 GHz band and 92 % to 98 % in the 2-4 GHz band.

3 DBBC3 – R2DBE Digital Correlation Coefficient for 100 % Correlated Noise

Measurement Setup

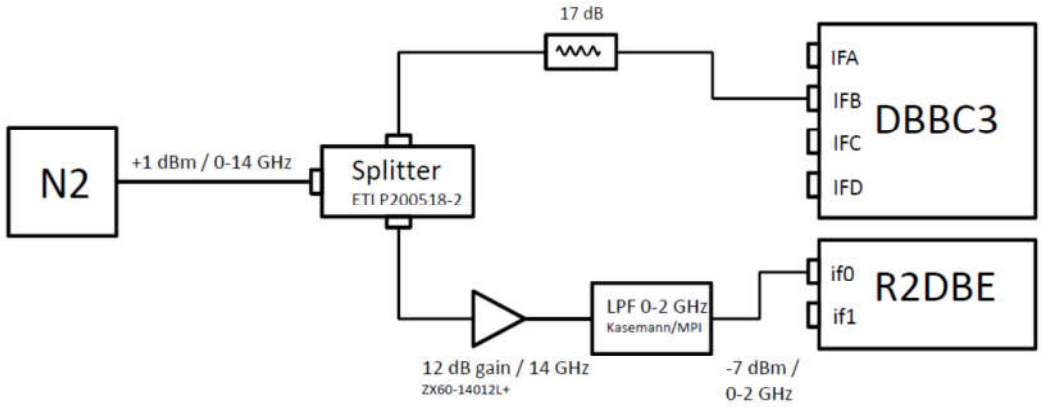


Figure: Lab setup for splitting noise to the DBBC3 and R2DBE for coherence test with 100 % correlated noise.

Results

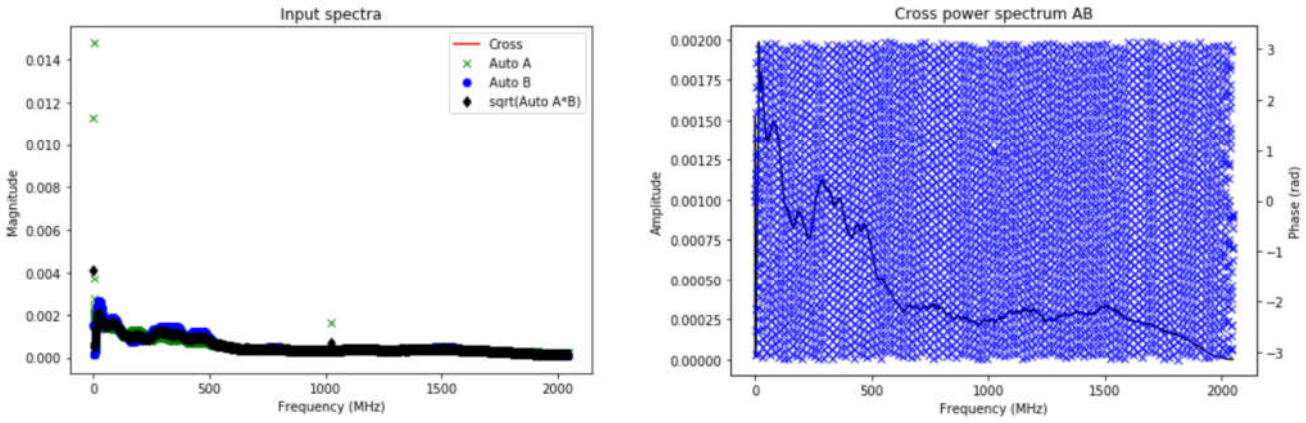


Figure: Digital correlation coefficient determination, for DBBC3 vs R2DBE with input analogue correlation of 1.0. *Left:* Two auto-correlation spectra (blue and green), and the geometric mean of the autocorrelation spectra (black), and the cross-power spectrum (red). *Right:* The corresponding cross-power phase vs frequency. The amplitude scaling is compressed by a spike at DC. The phase wraps quickly due to 0.05 µs delay difference between the backends. This delay difference is well within the correlator search window of tens of microseconds, and will anyway remain constant and be built into the station clock offset.

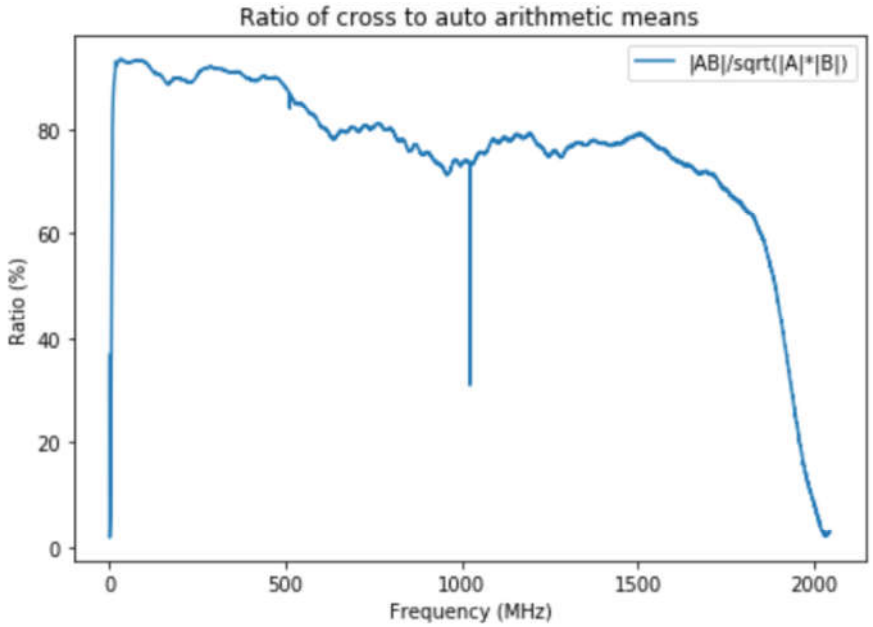


Figure: Bandpass shape of 0-2 GHz band after normalizing the cross-power spectrum by the geometric mean of the auto-correlation spectra. The amplitude scale indicates the degree of correlation between the DBBC3 and R2DBE. The average amplitude after fringe fitting is 0.812 on the baseline, or taking the square root to give the efficiency for a single IF as is recorded in VLBI gives an efficiency of each backend of 0.901.

The bandpass shape is good, quite flat and shows sharp rolloff at the top end due to the OCT filter in the DBBC3 and the LPF ahead of the R2DBE. The high digital correlation coefficient of 0.815 on the baseline shows good compatibility between the backends.

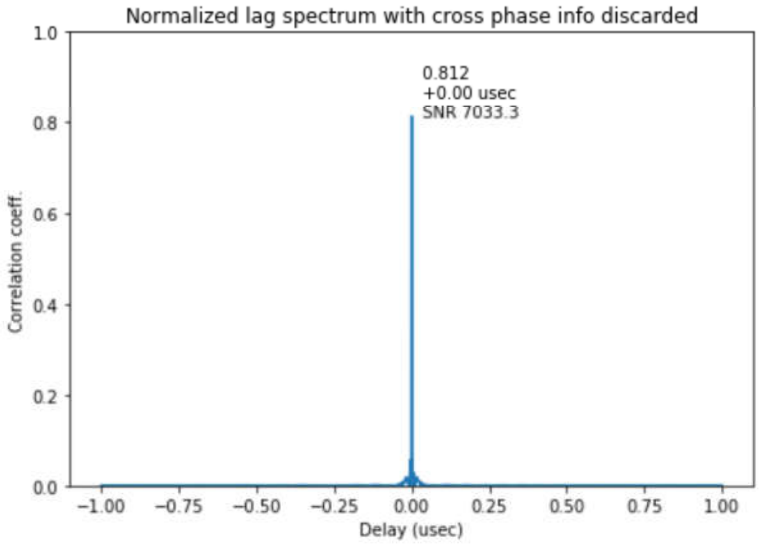


Figure: The lag spectrum after fringe fitting, including fractional-sample delay correction, giving an output digital correlation coefficient of 0.812.

4 DBBC3 – R2DBE Digital Correlation Coefficient for Partially Correlated Noise

Measurement Setup

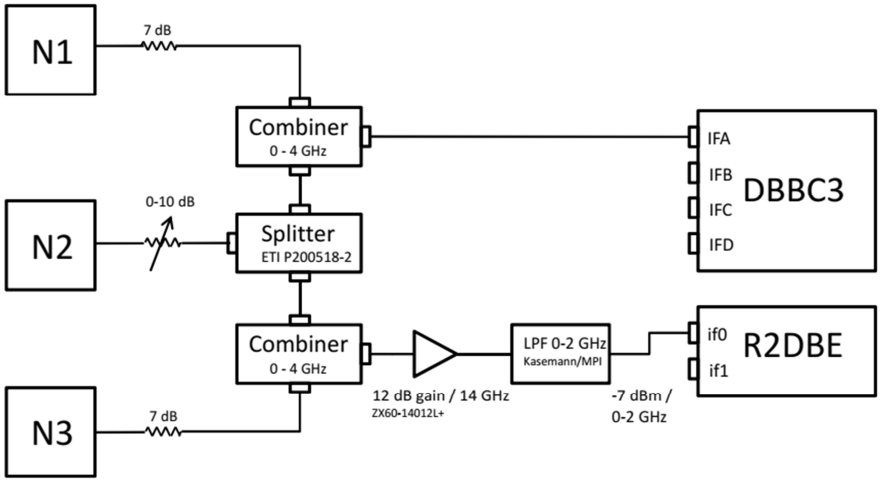


Figure: Lab setup for splitting noise to the DBBC3 and R2DBE for coherence test with partially correlated noise.

Results

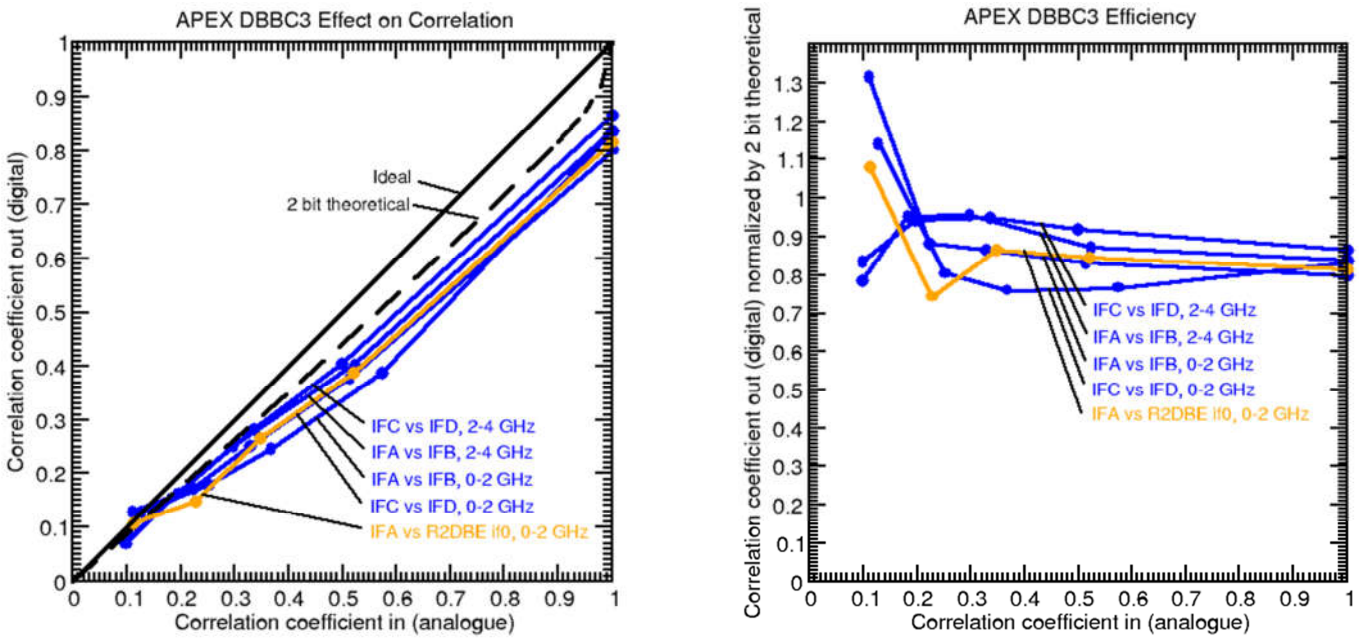


Figure: As for the efficiency plots in the previous section, with the DBBC3 - R2DBE zero-baseline test overlayed in orange. *Left:* Output vs input correlation coefficient. *Right:* Output correlation coefficient divided by the 2 bit theoretical value. The efficiency for either single backend is the square-root of the efficiency here. The DBBC3 and R2DBE show good efficiency in correlation against each other.

Discussion

The efficiency on the DBBC3 - DBBC3 baseline is the same as on DBBC3 - R2DBE baseline.

The **efficiency for a single backend** is the square root of the efficiency found here on the baseline, or from the DBBC3-R2DBE baseline is **90 % to 93 %** in the 0-2 GHz band in each backend, discarding the two points with lowest input analogue correlation due to higher uncertainty.

6 On-Sky Fringe Test

Kashima – Onsala Test

People:
Mamoru Sekido NICT, Kashima Space Technology Centre, Japan
Kazuhiro Takefuji NICT, Kashima Space Technology Centre, Japan
Karl-Åke Johansson Onsala Space Observatory, Sweden
Simon Casey Onsala Space Observatory, Sweden
Rüdiger Haas Onsala Space Observatory, Sweden
Gino Tuccari MPIfR
Sven Dornbusch MPIfR

Measurement Setup

Date: 27.03.2018, 19 h observing track

Stations: Kashima 34 m
Onsala 13.2 m twin telescope (ONSA 13NE)

Targets: 203 radio sources, 300 s each, broadband radio source survey

Frequency Setup:
4x 1 GHz bands in range 3 GHz to 11 GHz
Dual linear polarization
1 bit sampling
16.384 Gbps data rate

Data Acquisition Systems:
Japanese DAS: K6 GALAS (at Kashima)
DBBC3 running OCT firmware (at Onsala)

Correlation: Kashima / GICO3 software correlator (NICT)

Goals: 1) radio source survey to verify correlation amplitudes with the broadband antenna,

2) collect data for developing bandwidth synthesis of dual linear polarization data.

Results:

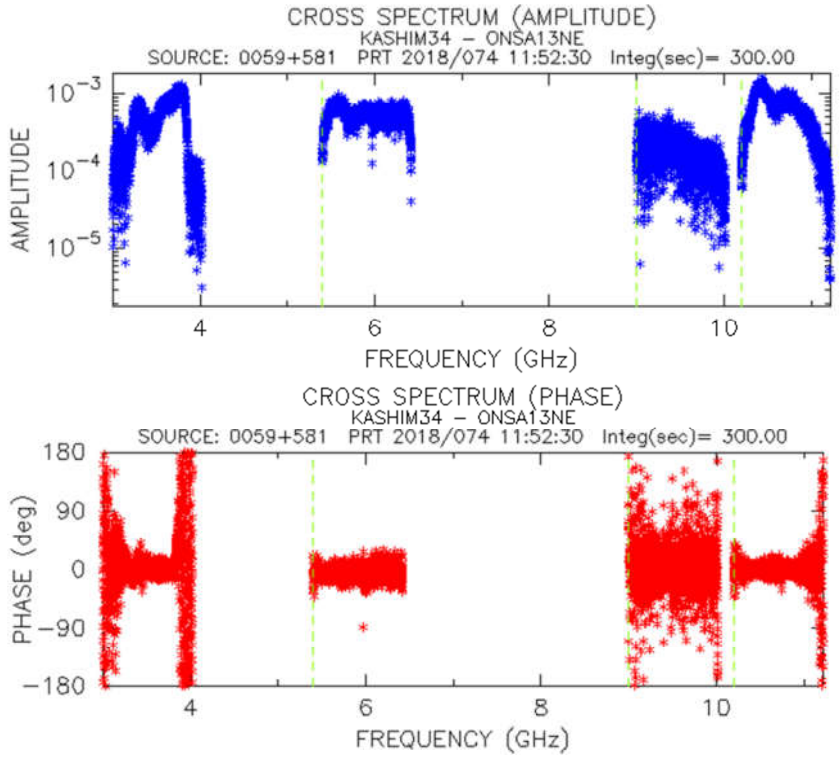


Figure: Fringes were detected in all four bands and in both polarizations at NICT with the GICO3 software correlator. This figure shows the fringe amplitude and phase vs frequency. At 5.4 GHz one pol produced no fringes for unknown reasons, thus fringes were found in 7 of 8 recorded IFs. The OCT firmware on the DBBC3 selected 1 GHz bands out of 4 GHz sampled IF bandwidth to match the K6 capability of 4x 1 GHz sampled bands.

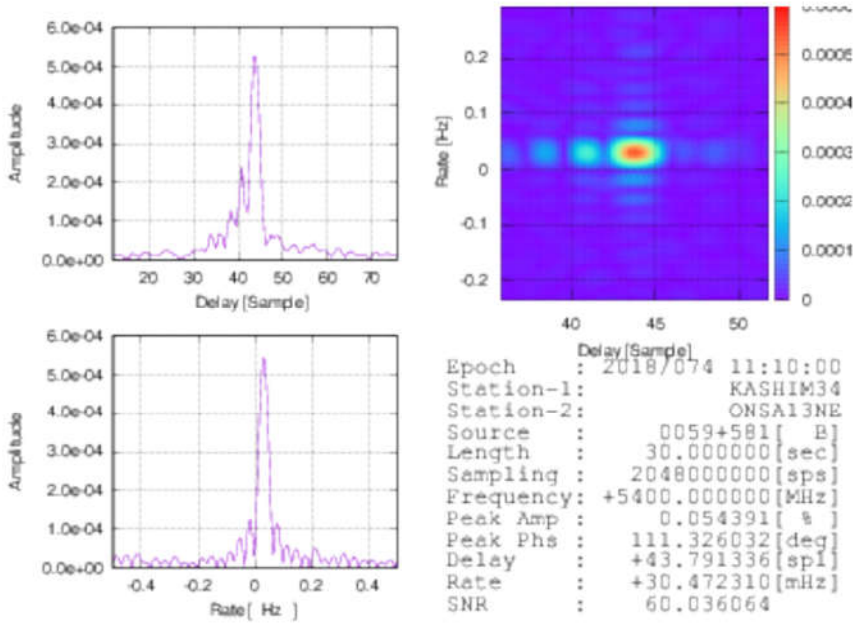


Figure: Fringes displayed in the delay-rate space during fringe fitting shows good SNR (60) in 30 s at 5.4 GHz on the source 7C 0059+5808.

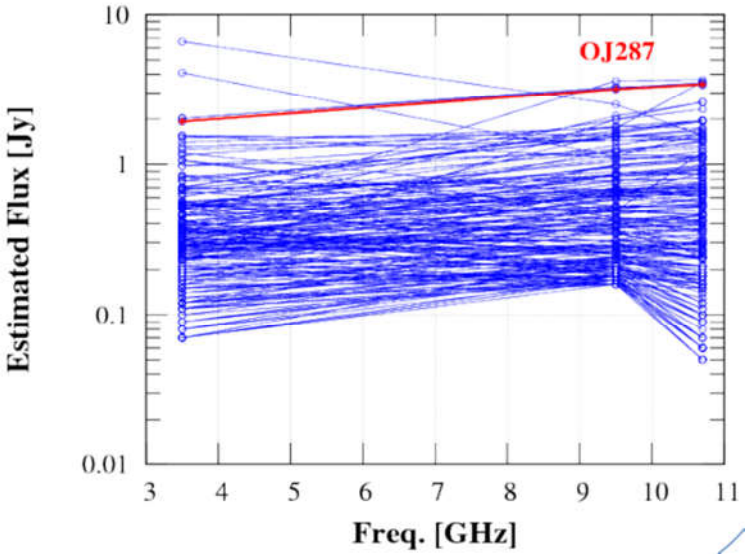


Figure: Broad-band radio spectra of 200 sources measured between DBBC3 running OCT firmware on ONSA13NE and K6 GALAS on Kashima 34 m on 2018mar27. Amplitudes were calibrated based on the adopted flux density of OJ 287 of 1.68 Jy at 2.3 GHz and 2.95 Jy at 8.4 GHz.