DBBC as Radar VLBI Backend

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VIRAC2012
15 August, 2012

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The researches were supported by the European Social Fund (project No. 2009/0231/1DP/1.1.1.2.0/09/APIA/VIAA/151).


D B B C


FRAGILE

- **HAT-Lab is a spin-off company endorsed by INAF, set in July 2009**

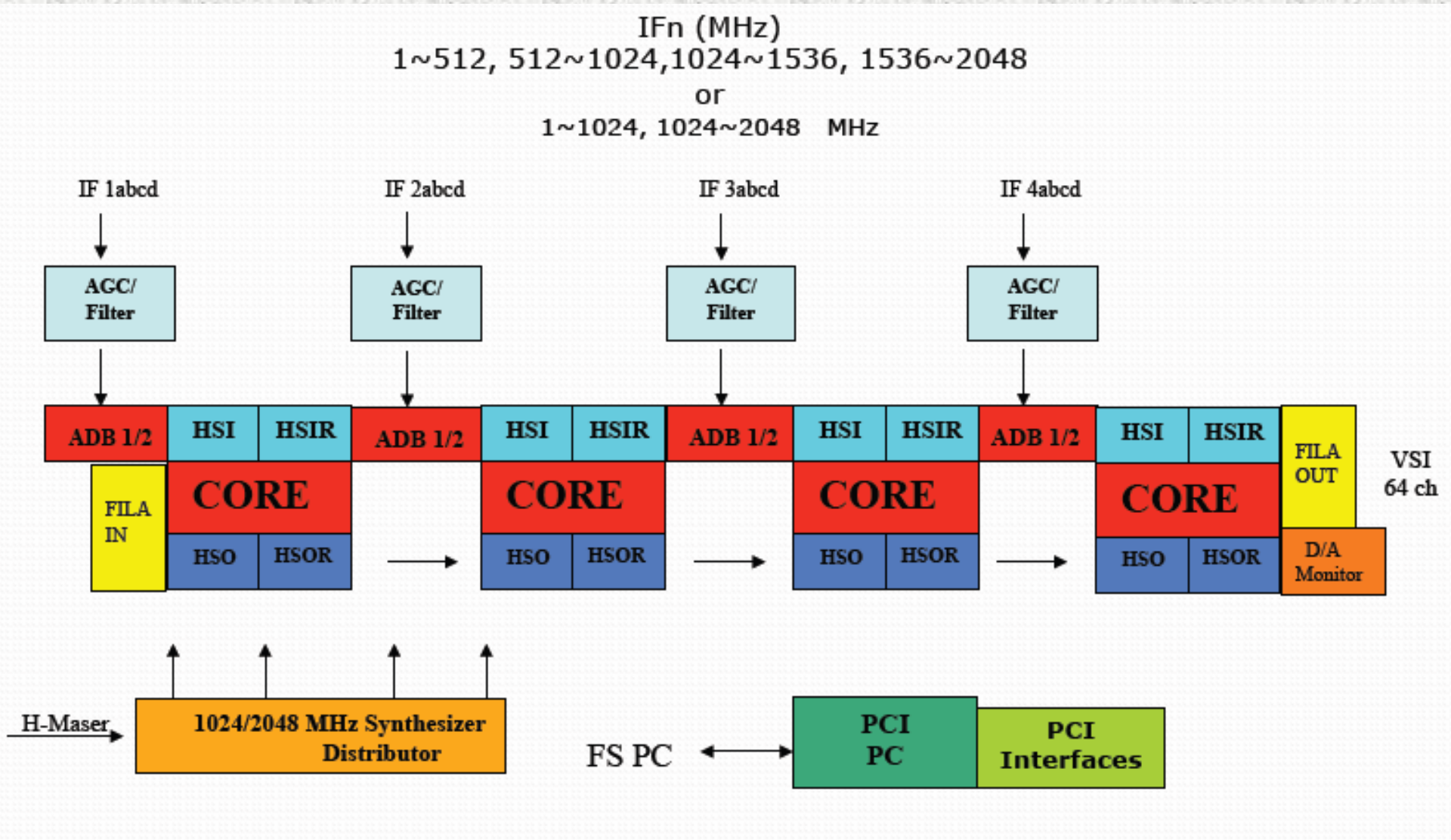
- **HAT-Lab main task is to produce DBBC back-ends in close collaboration with IRA and MPI**

- **Production activity is shared between Italy (Catania and Noto) and Germany (Bonn)**

- **Development of new VLBI components and equipment in collaboration with EVN partners**

Station	DBBC	Comment
Noto	Available (to be upgraded VLBI2010)	FILA10G order under way
Effelsberg	Available	FILA10G available
Onsala	Available	FILA10G ordered
Yebes	Available	FILA10G order under way
Wettzell	Available 3 (to be upgraded UNICA4)	
Torun	Available	
Metsähovi	Ordered (to be delivered in few weeks)	FILA10G ordered
Hartebeesthoek	Available 2	FILA10G available 2
Medicina	Ordered (to be delivered in September)	FILA10G ordered
Westerbork	-	
Jodrell Bank	-	
Cambridge	-	
Svetloe	-	Own semi-digital system
Zelenchukskaya	-	Own semi-digital system
Badary	-	Own semi-digital system
Urumqi	-	Own digital system
Shanghai	Ordered	FILA10G ordered + own digital system
Arecibo	-	RDBE
Robledo	-	
Sardinia	Available	FILA10G available
Simeiz	-	
Venspils	Available	Second system with FILA10G to be ordered
Evpatoria	-	

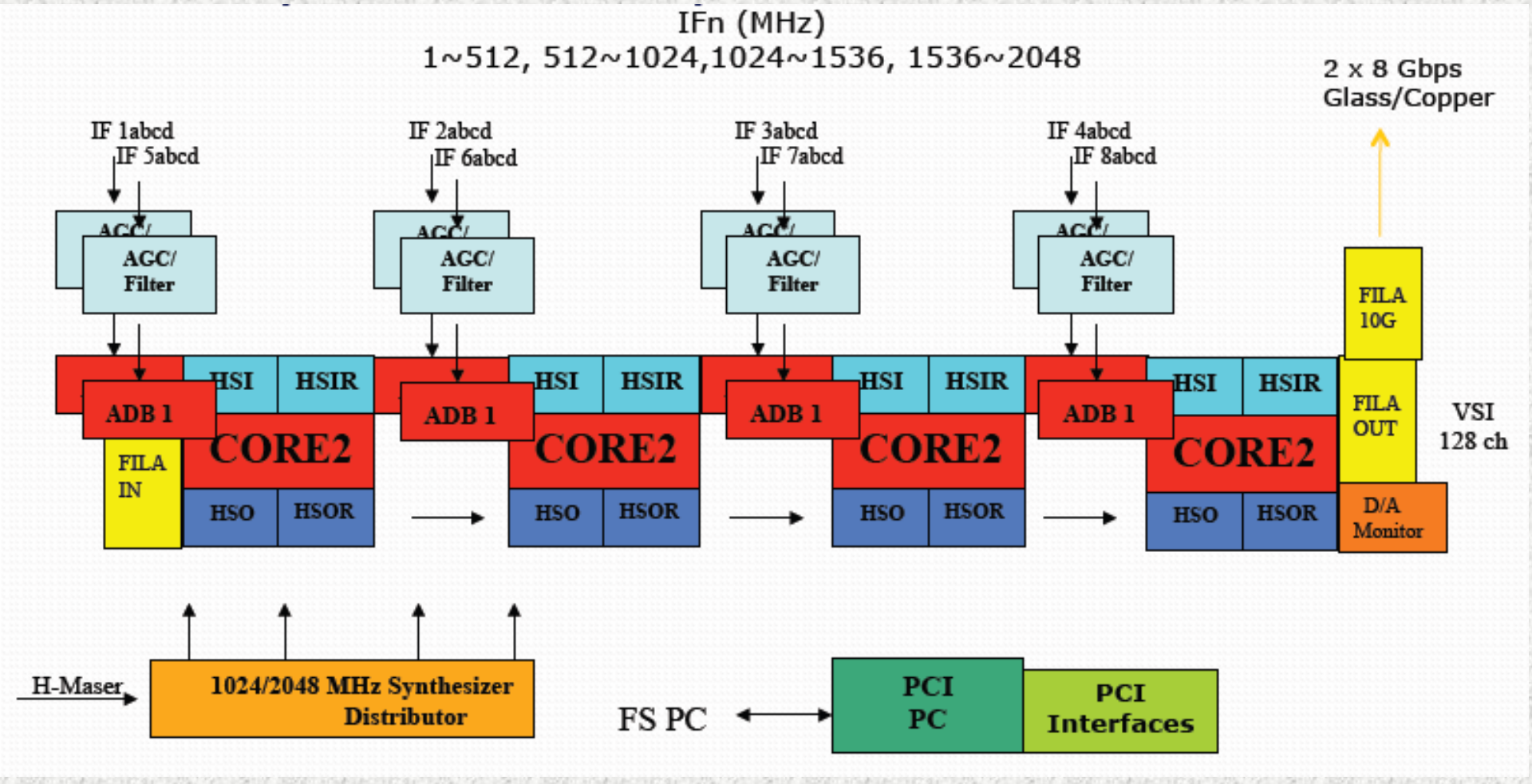
Hardware architecture DBBC2



Hardware architecture

DBBC2010 Architecture

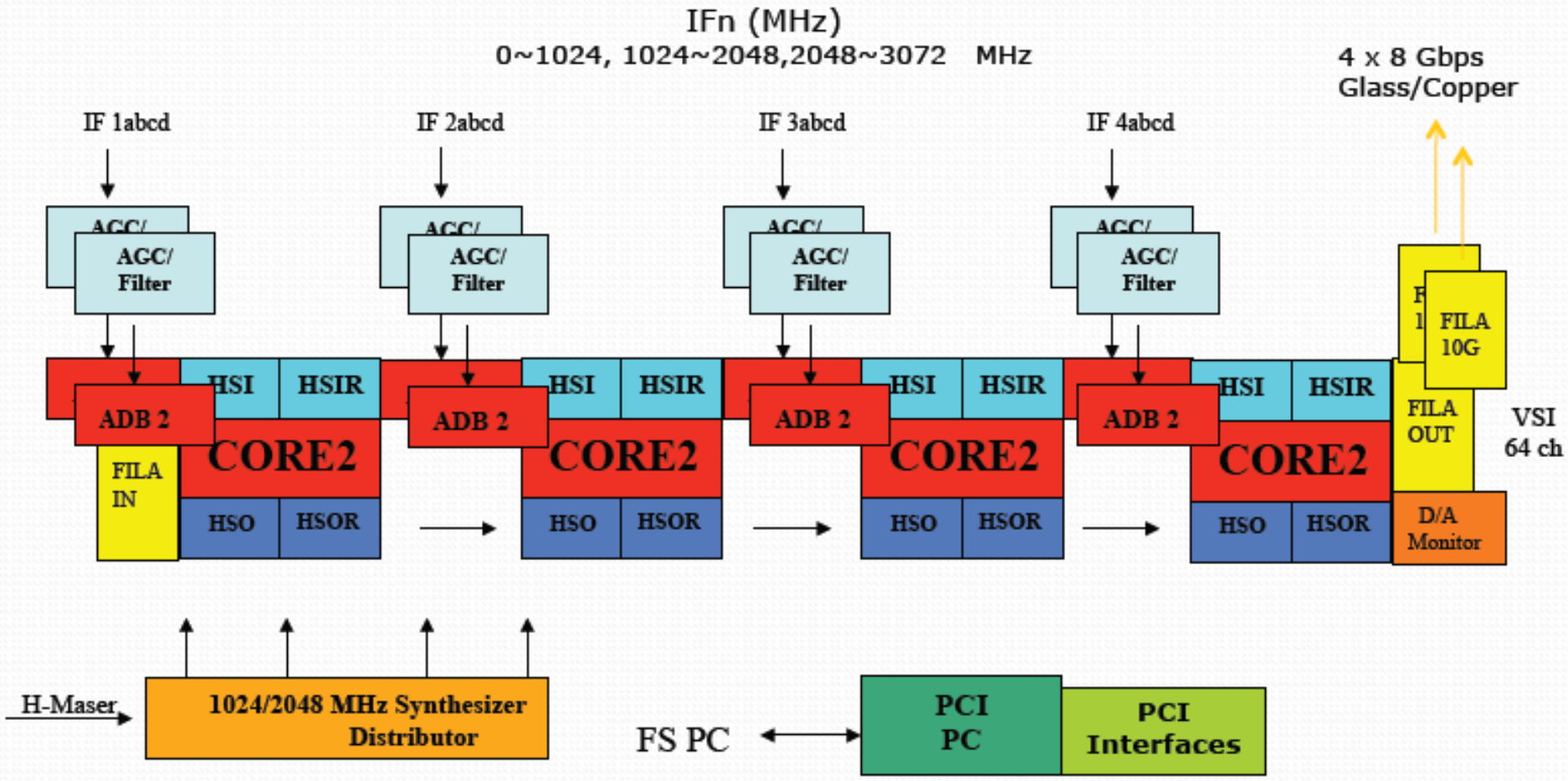
A 8 IFs @ 512 MHz Output data rate 16 Gbps



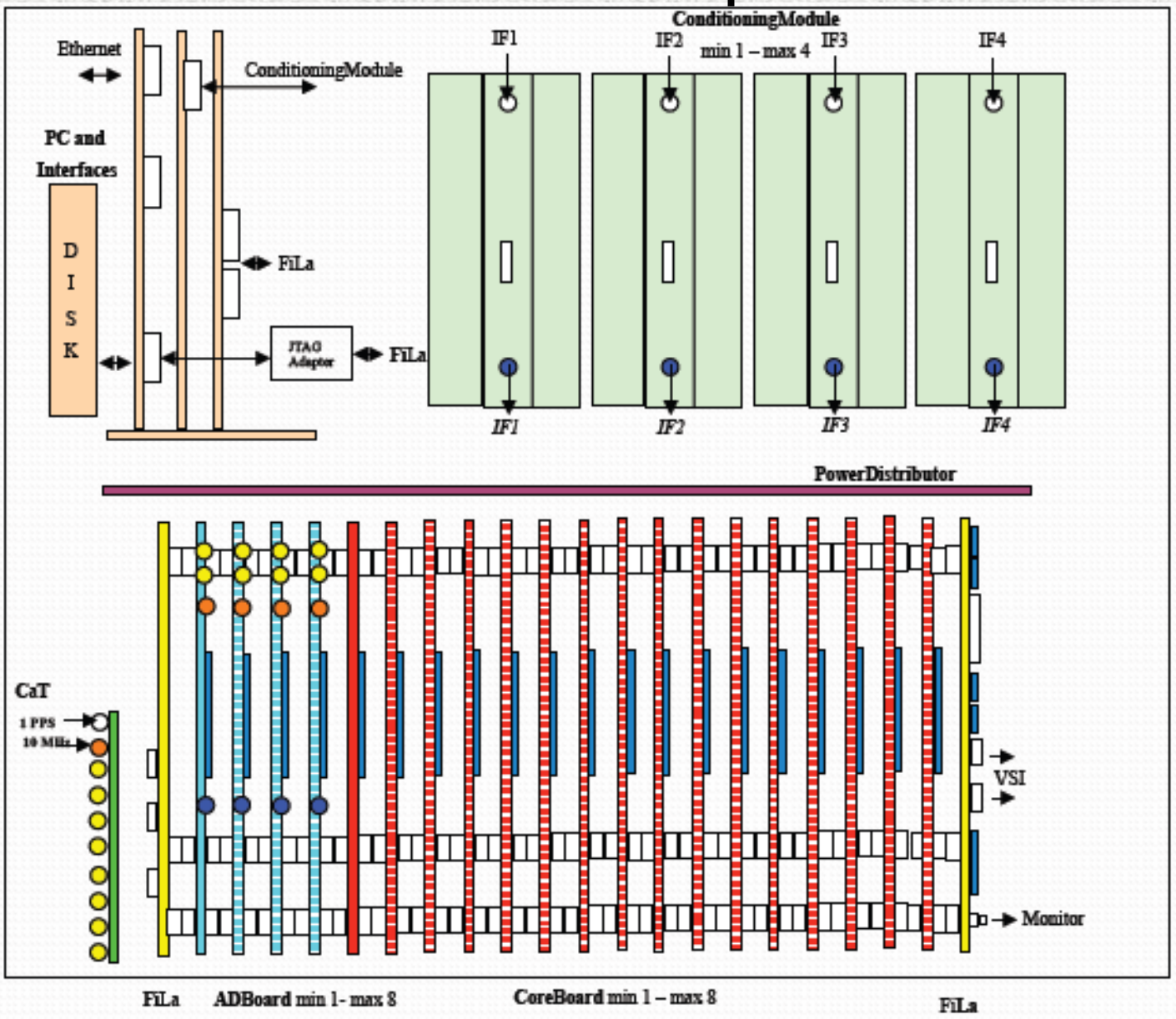
Hardware architecture

DBBC2010 Architecture

A 8 IFs @ 1024 MHz Output data rate 32 Gbps



DBBC2
Schematic Top View

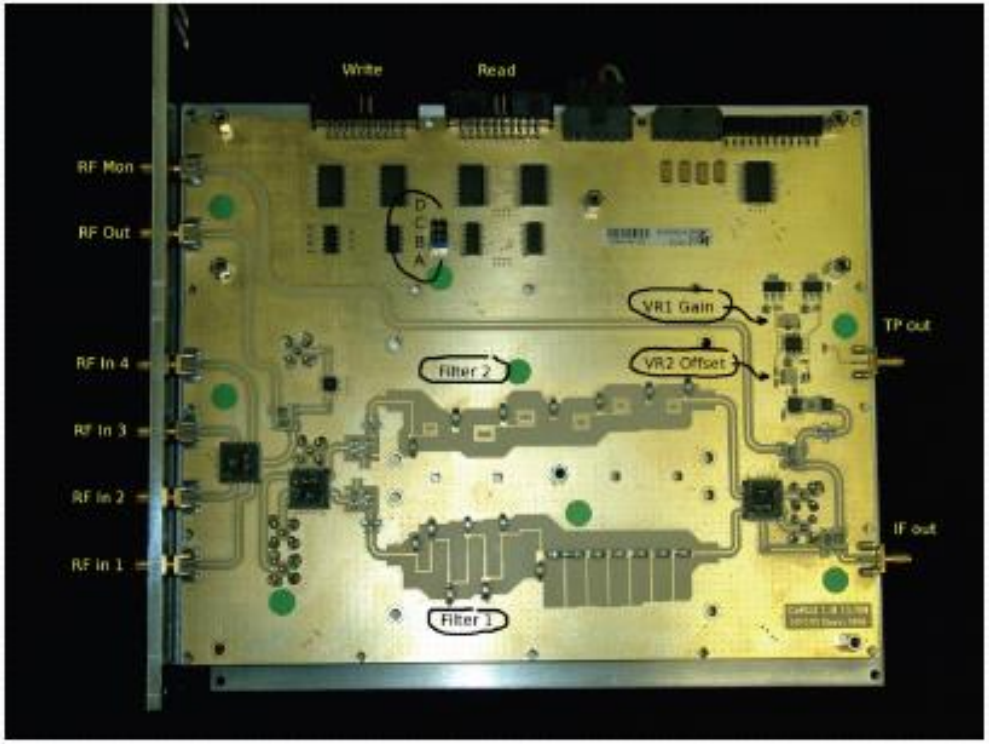


Review of the System Components

- Analog Conditoning Module
- Analog - Digital Converter (ADBoard1 - ADBoard2)
- Data Processing (CoreBoard2)
- Connection and Service (FiLaIN/OUT - FiLa10G)
- Timing and Clock (CaT1/2 – Clock and Timing Boards)
- Computer Control (PCSet)

How the DBBC is to be connected in your control room

Conditioning Module (Unica3)



- **4 selectable RF input**
- **4 selectable Nyquist filters**
- **32 dB programmable attenuation**
- **Total power full band**
- **Manual or automatic gain control**

ADBoard1

Analog to Digital Converter

Analog input: 0 - 2.2 GHz

Max Sampling clock single board: 1.5 GHz

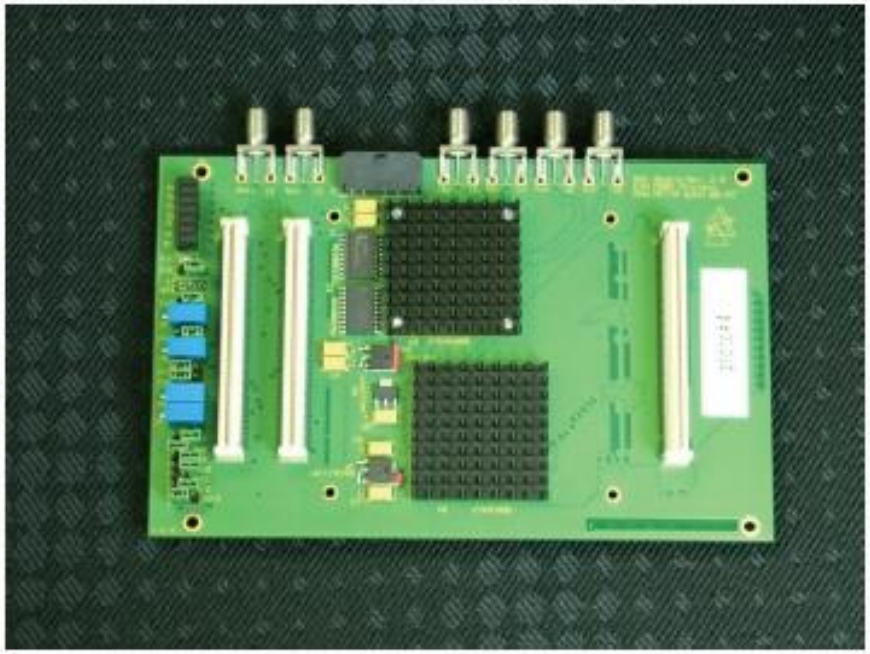
Max Istantaneous Bandwidth in Real Mode: 750 MHz

Max Istantaneous Bandwidth in Complex Mode: 1.5 GHz

Output Data: 2 x 8-bit @ ¼ SClk DDR

ADBoard2

Analog to Digital Converter



Analog input: 0 – 3.5 GHz

Max Sampling clock single board: 2.2 GHz

Max Istantaneous Bandwidth in Real Mode: 1.1 GHz

Max Istantaneous Bandwidth in Complex Mode: 2.2 GHz

Output Data: 2 x 8-bit @ ¼ SClk DDR
4 x 8-bit @ 1/8 SClk DDR

Piggy-back module support for 10-bit output and connection with FiLa10G board.

Core2

Basic processing unit

Input Rate:
(4 IFs x 2 bus x 8 bit x SClk/4 DDR) b/s
(2 IFs x 4 bus x 8 bit x SClk/8 DDR) b/s
More…

Typical Output Rate:
(64 ch x 32-64-128) Mb/s

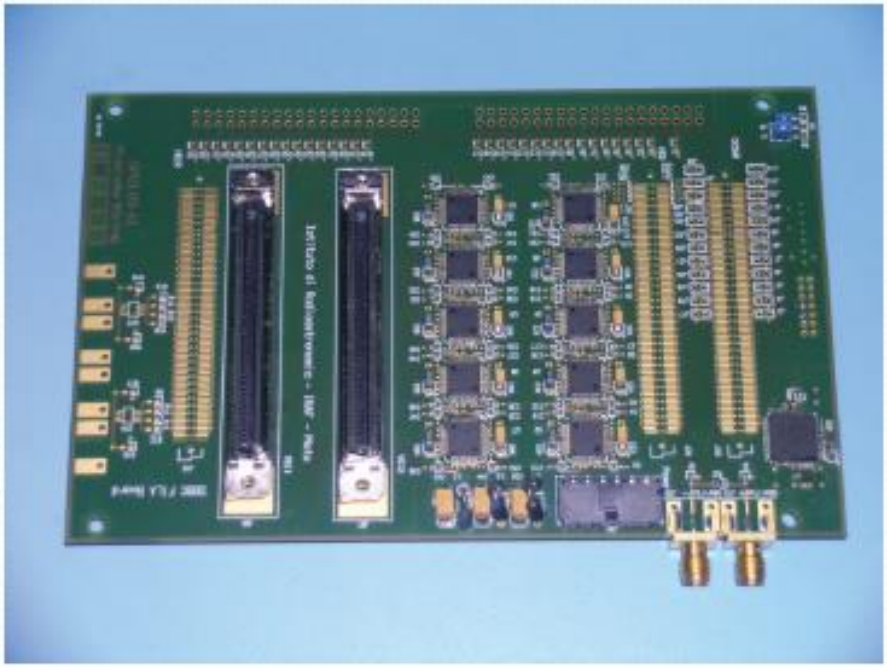
Programmable architecture

Es. Digital Down Converter:
1 CoreBoard2 = 4 BBC

Max Input/Output Data Rate 32.768 Gbps

FiLa Board

Connection and Service



First and Last board in the stack

First:
- **Communication Interface**
- **JTAG Programming Channel**
- **1PPS Input**

Last:
- **2 VSI Interfaces**
- **DA Converter**

1PPS Monitor Out

80Hz Continuous Cal Out

PCSet

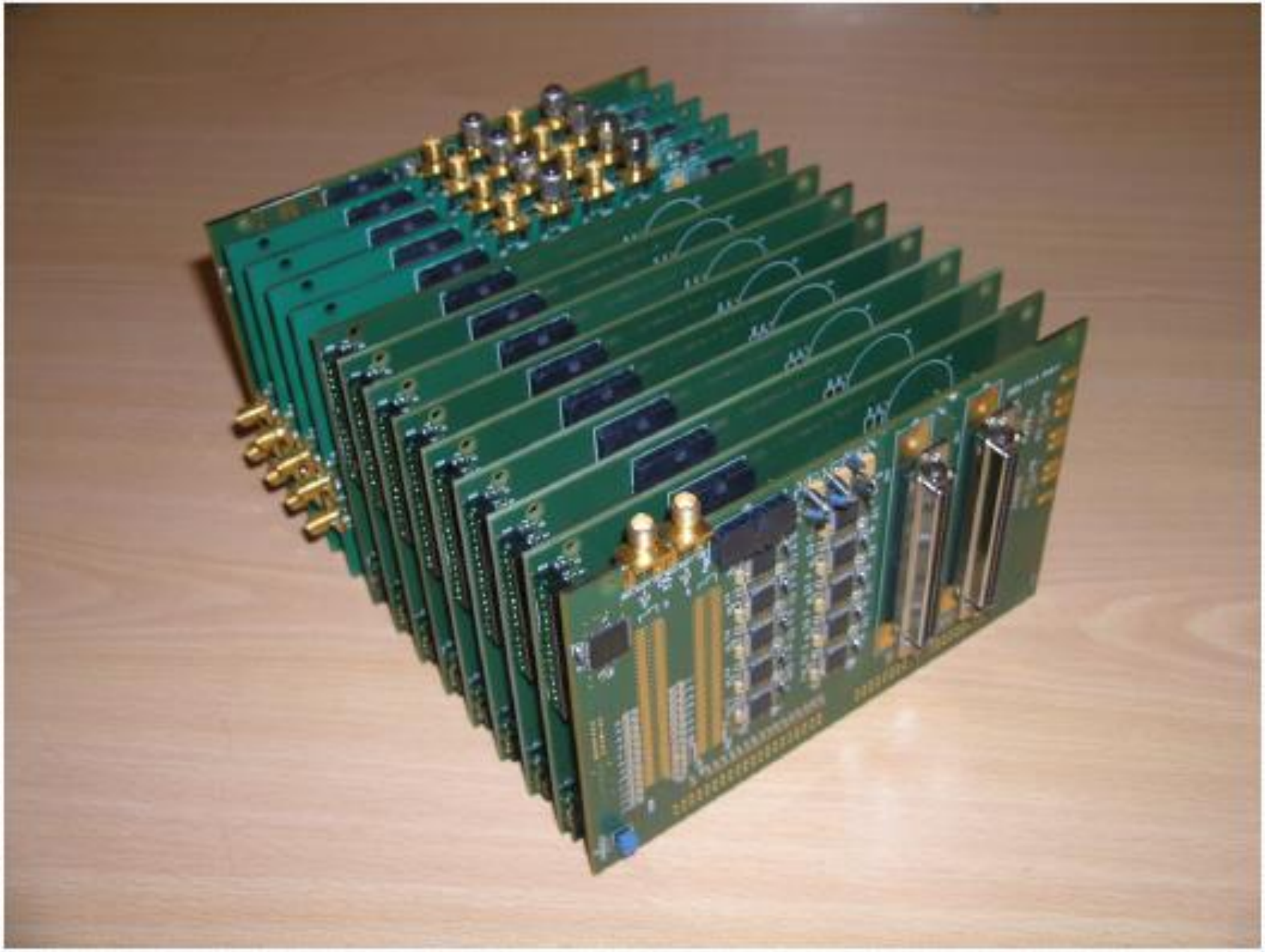
ADLink PCI9111HR:
Communication with Conditioning Modules for IF total power measure, automatic gain control, registers control, etc.

ADLink PCI7200:
Communication with 32-bit bus for Core2 register setting, total power measurement, state statistics, etc.

Adventech PCI-7030:
Half Size PCI Motherboard (Intel Atom) on PCI backplane

Xilinx programmer:
FPGA device configuration through USB – JTAG interface

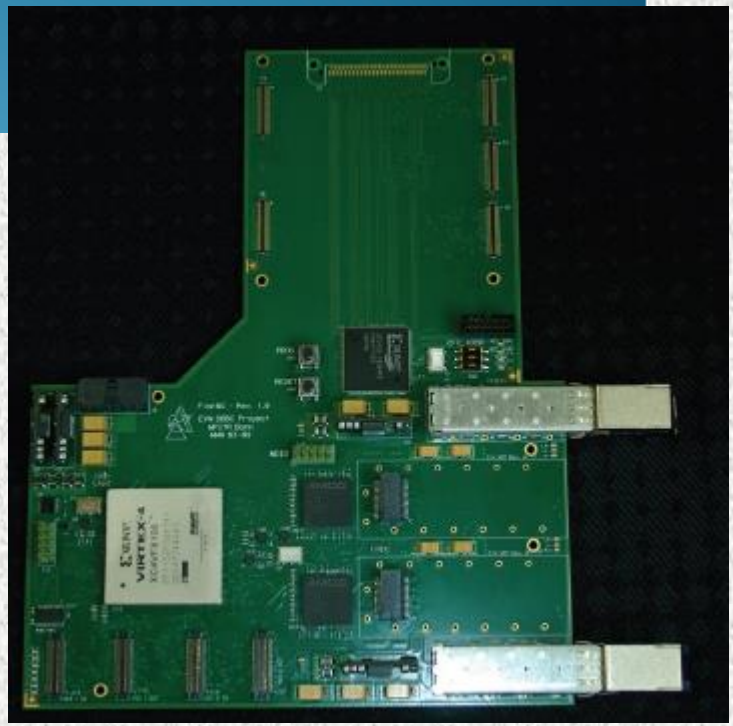
DBBC2 Module Stack



FiLa10G

10G Optical Fiber Ethernet Board

- Triangle connection between HSI (DBBC fast sampled data bus) – VSI – 10Gb link
- It can be placed either at the beginning or at the end of the stack chain → 10G link / MK5C
- Piggy-back board for ADB2



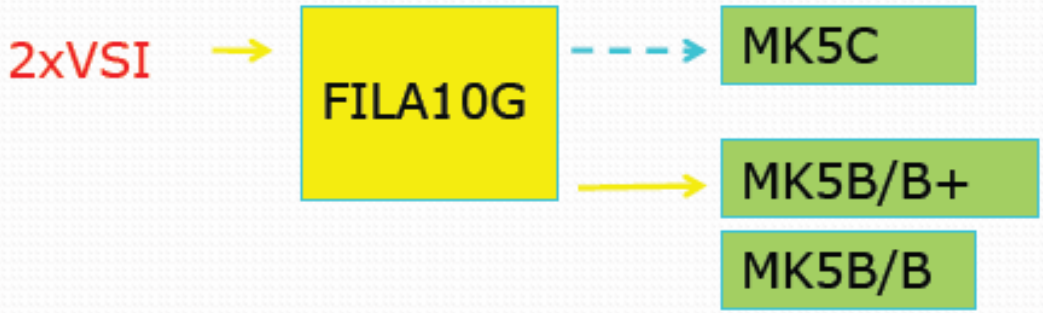
FILA10G main features

- Two independent 10G Ethernet UDP port
- Physical interface optical XFP
- 10G port fully bidirectional
- Installed inside the DBBC box or as stand-alone
- Data rate: 1 – 2 – 4 – 8 Gbps each 10G port
- Format mode: MK5B in two 5008 bytes packets
  VDIF-ST in any allowed packet size
  VDIF-MT corner turned under development

Connection examples

- 2 x VSI --> MK5C & 10GE net

- 2 x VSI --> MK5C & MK5B



Observing Modes

General Features (today)

- **4/8 RF/IF Input out of 16 (4x4) in a range up to 2.2 (3.5) GHz**
- **1024/2048 MHz sampling clock frequency**
- **More personalities for more observing modes**
- **Four/eight polarizations or bands available in 4 groups of 32 output data channel, each group max 4 Gbps output data rate**
- **Output from the FILA OUT to FiLa10G Ethernet card max as 2 x 4 Gbps, 8 x 4 Gbps from Core2 piggy-back (ask if required)**

Observing Modes (today)

- **DDC:**

tunable, channel bandwidth between 1 MHz and 16 MHz, U&L, Continuous cal with 80 Hz synchronization, mode ’astro’, ‘geo’, ‘w-astro’, ‘lba’, ’test’

- **PFB:**

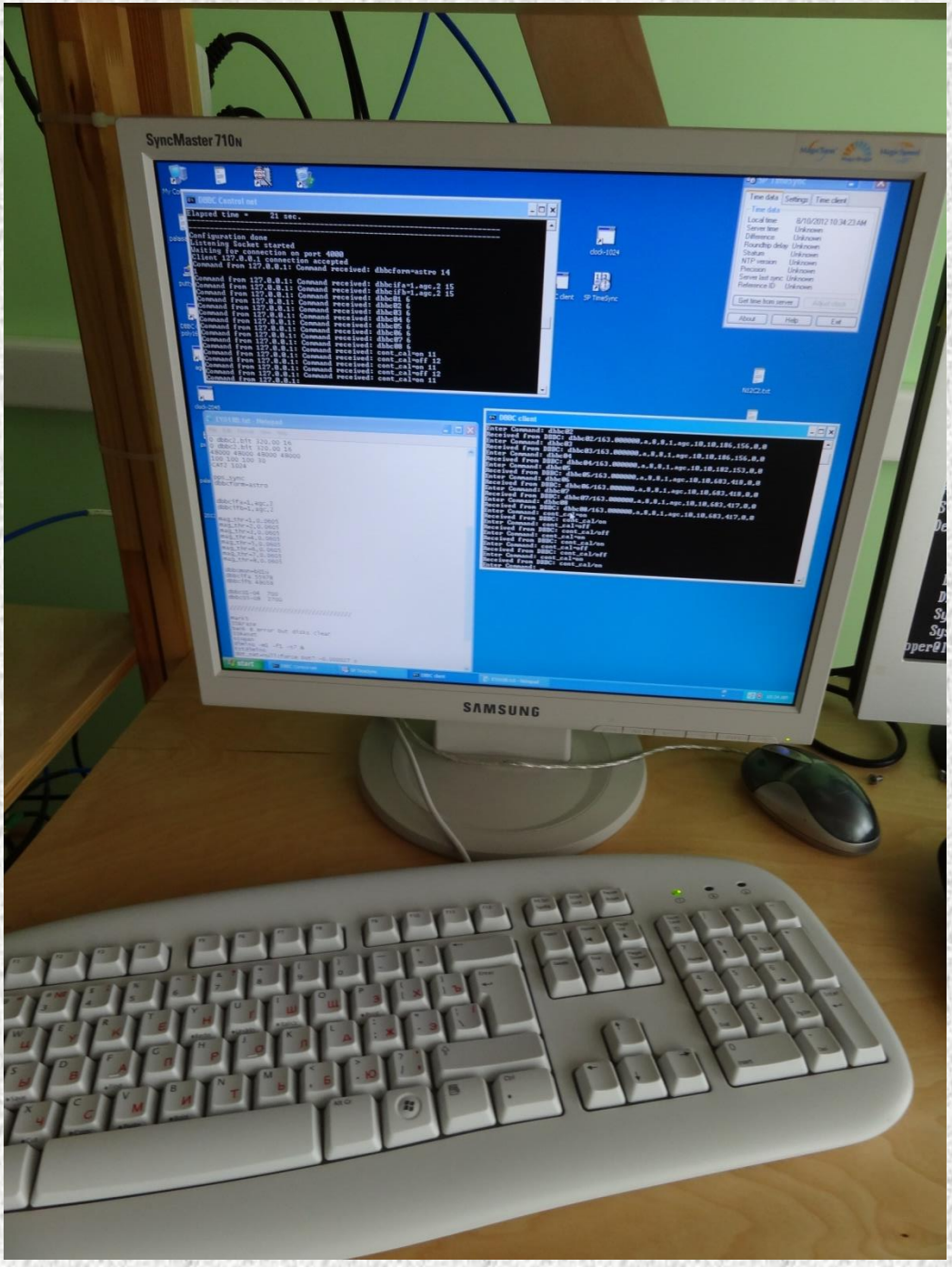
fixed tuning, channel bandwidth 32 MHz, all U or L depending on the Nyquist zone

- **DSC:**

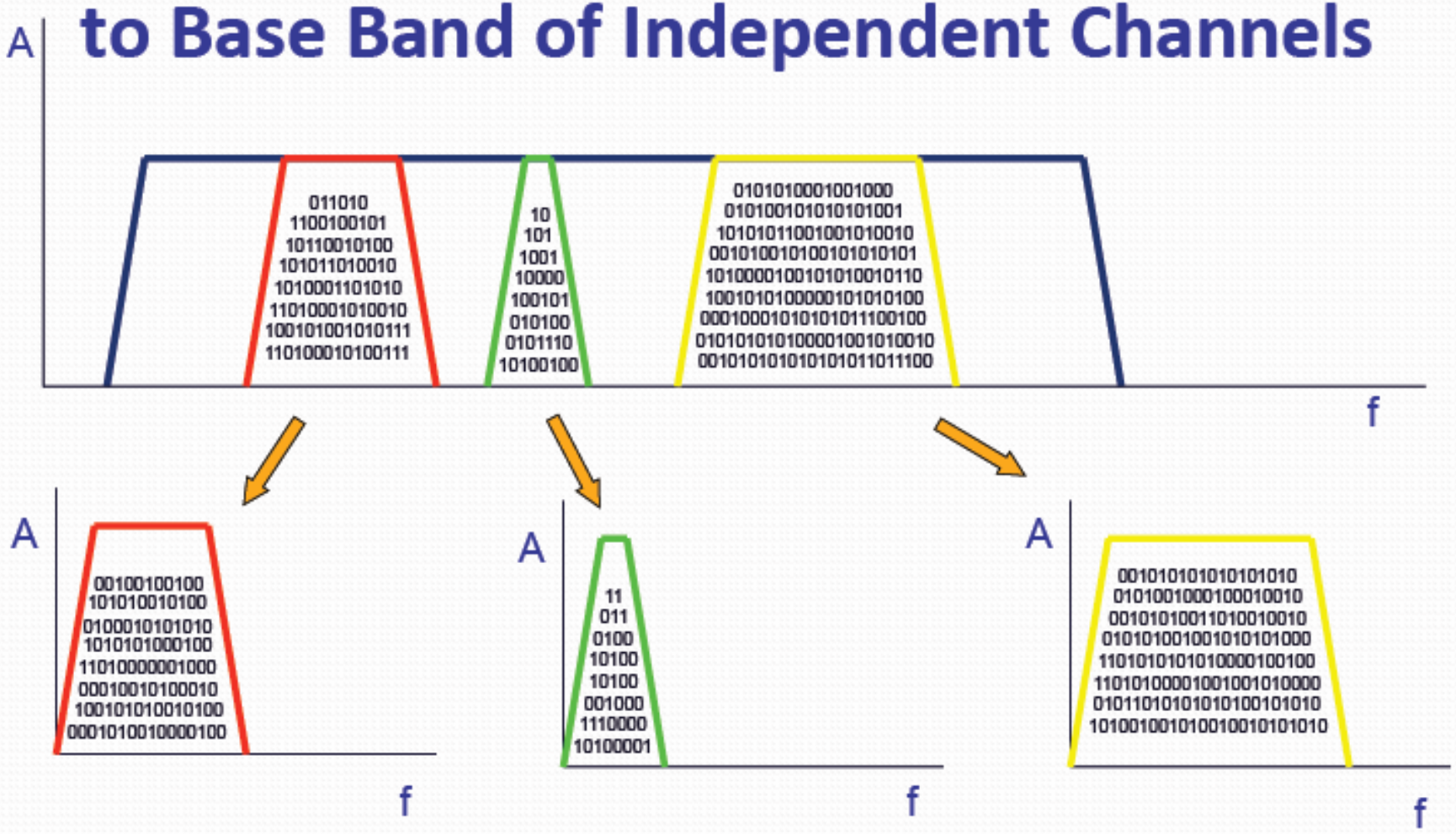
full 4 x 512 MHz , max 8 x 1024 MHz band direct sampling

- **SPECTRA:**

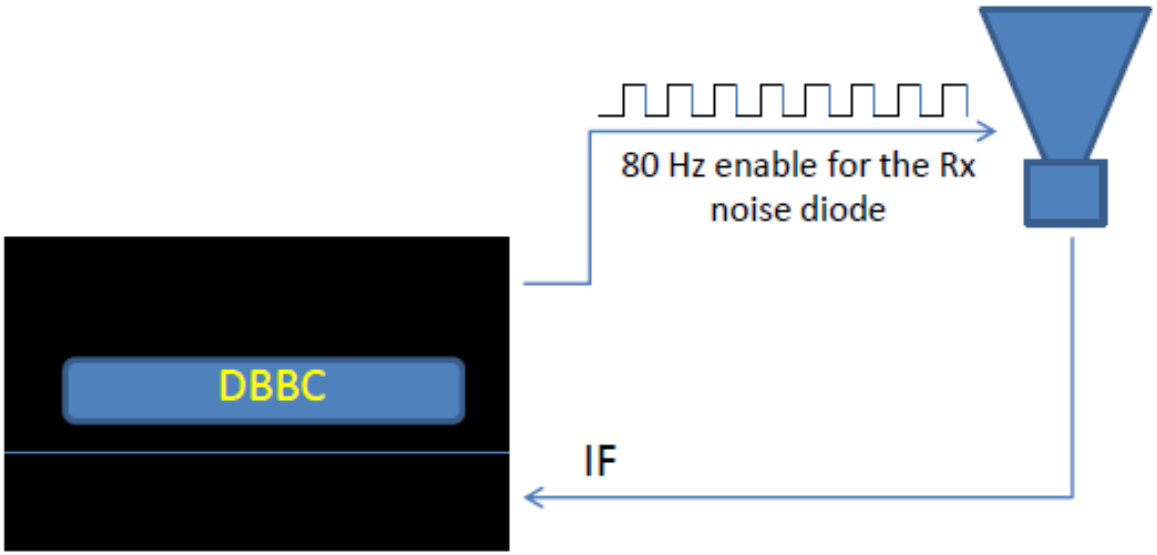
16K channels spectrometer


SyncMaster 710N
SAMSUNG

DDC - Digital Down Conversion to Base Band of Independent Channels

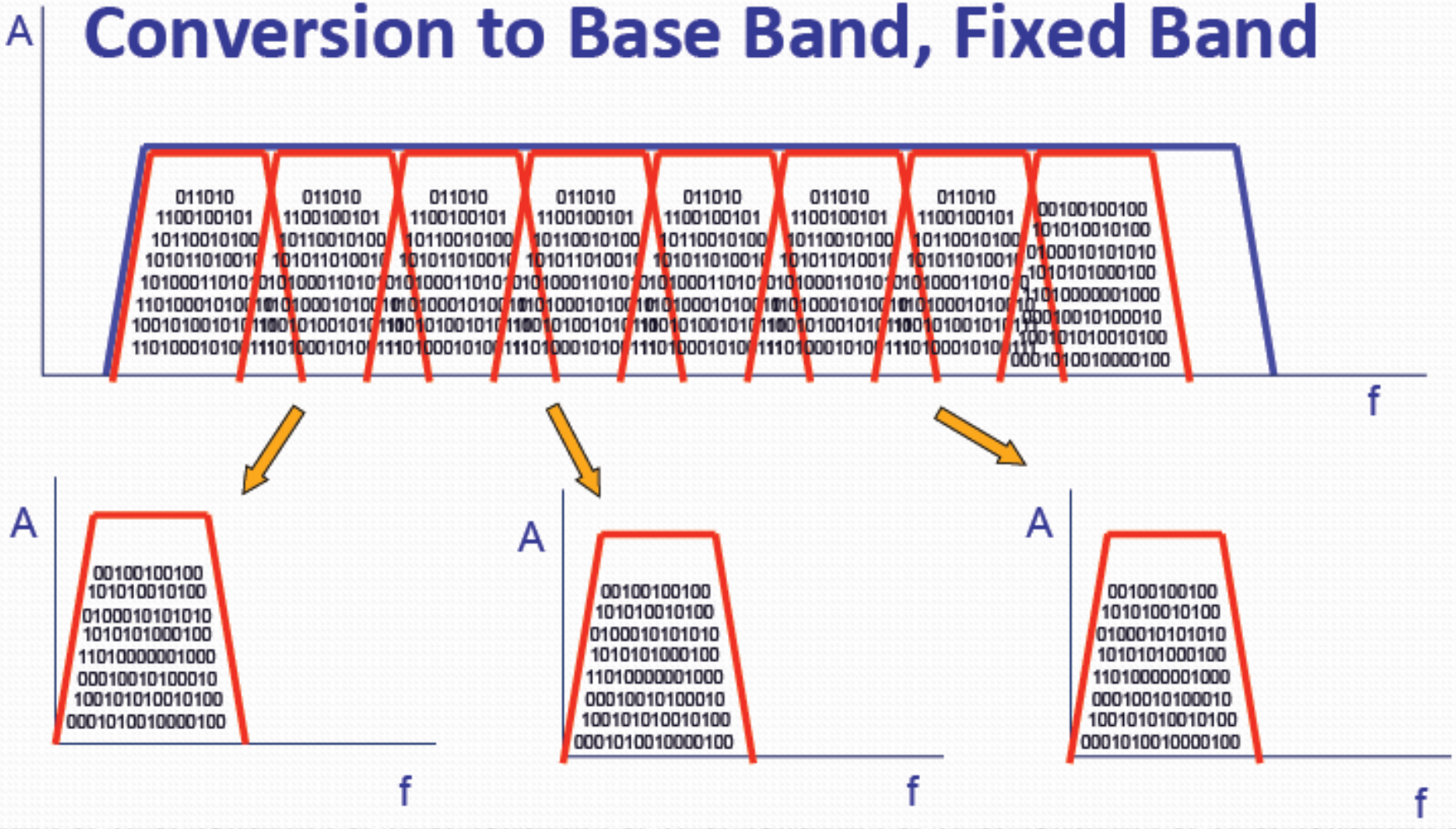


80 Hz Continuous Noise Calibration

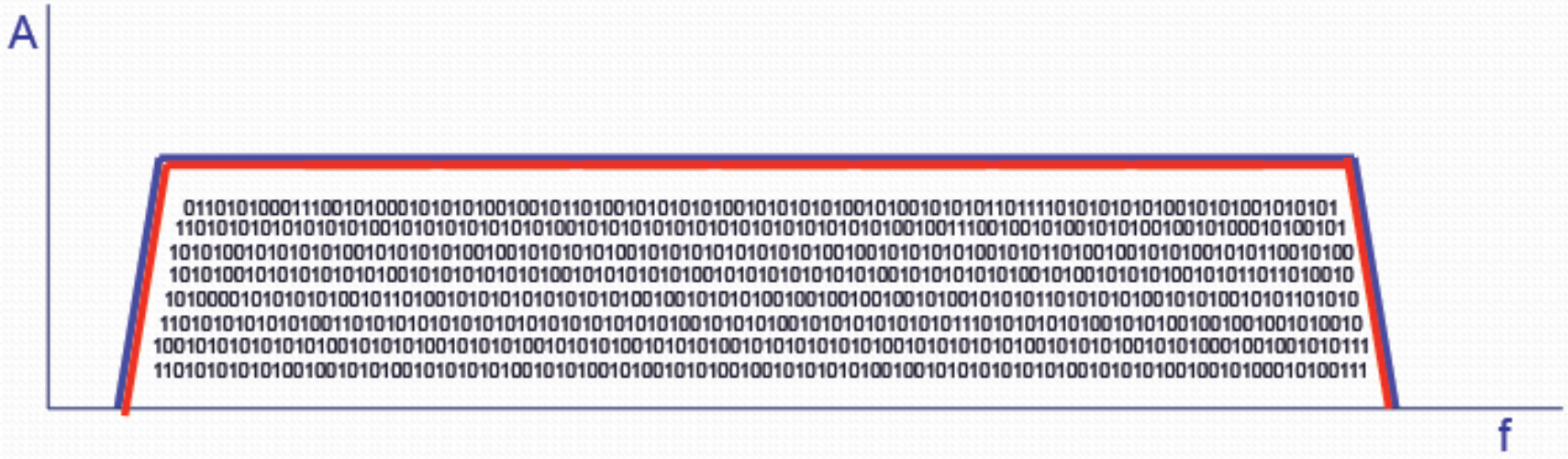


cont_cal=off
dbbc01= 567.99,a,8,1,agc,10,10,3480,3628,0,0
dbbc02= 715.99,a,8,1,agc,10,10,3129,2997,0,0
cont_cal=on
dbbc01= 567.99,a,8,1,agc,10,10,1860,1929,1615,1703
dbbc02= 715.99,a,8,1,agc,10,10,1693,1586,1421,1412

PFB – Polyphase Filter Bank
Conversion to Base Band, Fixed Band

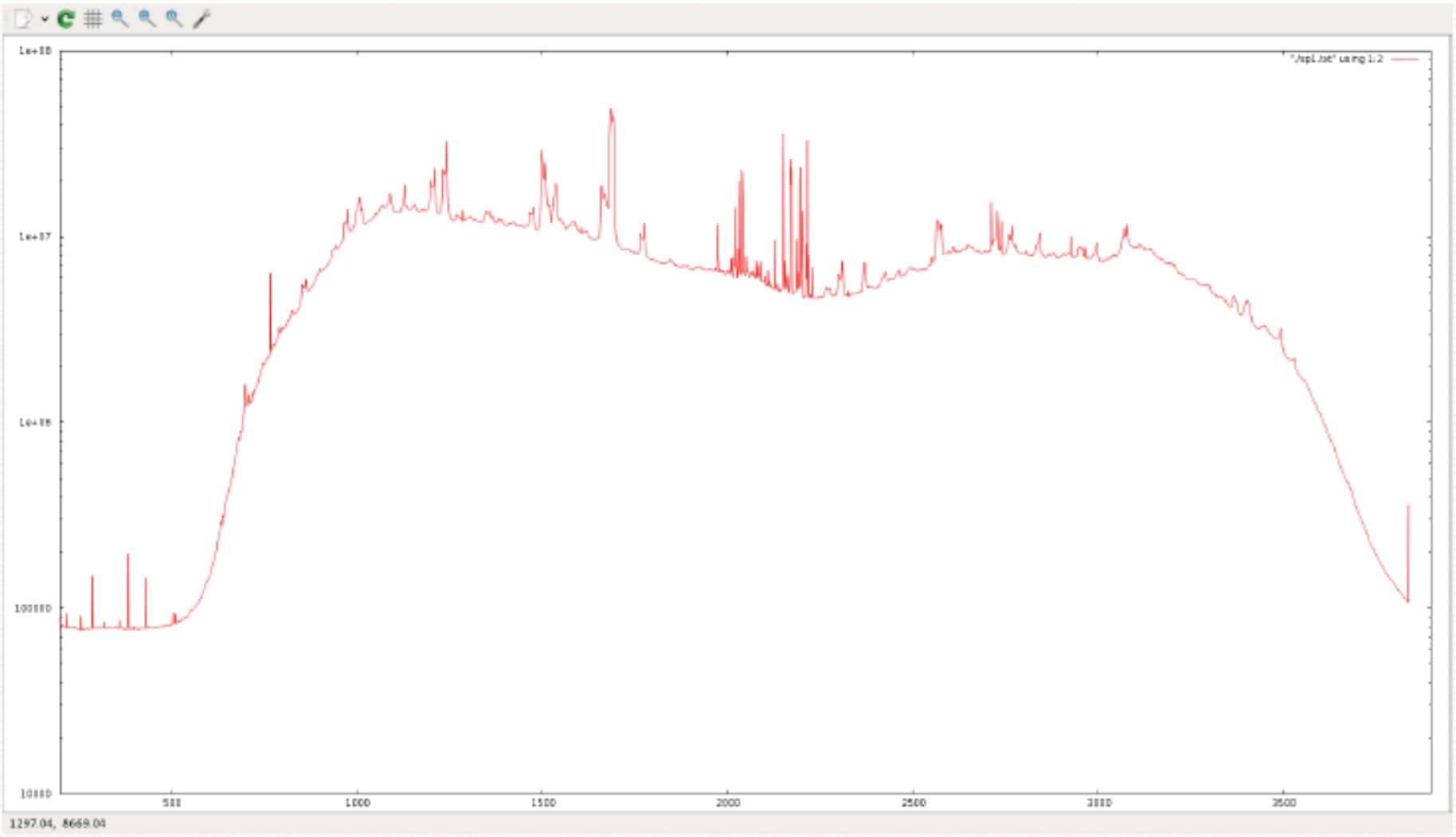


DSC – Direct Single band Conversion
Conversion to Base Band, Full Band



Spectra:

Noto L band cal tones off



DBBC Firmware for RadarVLBI

Two main functionalities added:

- **EFD** - Echo expected frequency ‘followed’ and detected in the observed sub-band

- **FSS** - VLBI fringes station stopped

EFC – Echo Followed and Detected

- Tuning frequency is finely upgraded with an user external software model
- Frequency variation parameters pre-calculated and downloaded each second to the firmware
- Final tuning frequency calculated by the firmware (linear and quadratic increment in time) and applied to the tuner
- Following timing clock (frequency recalculation and upgrade) 128 MHz
- Arbitrary frequency tone amplitude and phase detection

FSS - Fringes Station Stopped

- Added to the DBBC software control:
  - Observing station geometric parameters
  - Time epoch
  - Observed source coordinates
  - Sky frequency
- Final tuning frequency calculated by the firmware and applied to the tuner in order to get fringes stopped or quasi-stopped
- Zero baseline correlation software support

How the observing mode is selected

- **Using a dedicated firmware**
- **Using a dedicated control software**
- **Using a dedicated configuration text file**

Software Structure

- **C:\DBBC\bin → control software**
- **C:\DBBC\doc → manuals**

- **C:\DBBC_CONF\ → configuration text files**
- **C:\DBBC_CONF\FilesDBBC → firmware**

Software

- **General:**

  BASE Package

  c:\DBBC\bin\clock1024.exe (CAT2 1024)
  c:\DBBC\bin\clock2048.exe (CAT2 2048)
  c:\DBBC\bin\ad9858.exe (CAT1)
  c:\DBBC\bin\DBBC client v2.exe (general client)
  c:\DBBC\bin\power.exe (on-off hardware)
  c:\DBBC\bin\agc_if.exe (CoMo calibration)

Software on socket

- **DDC :**

c:\DBBC\bin\DBBC2 Control DDC v101.exe (server)

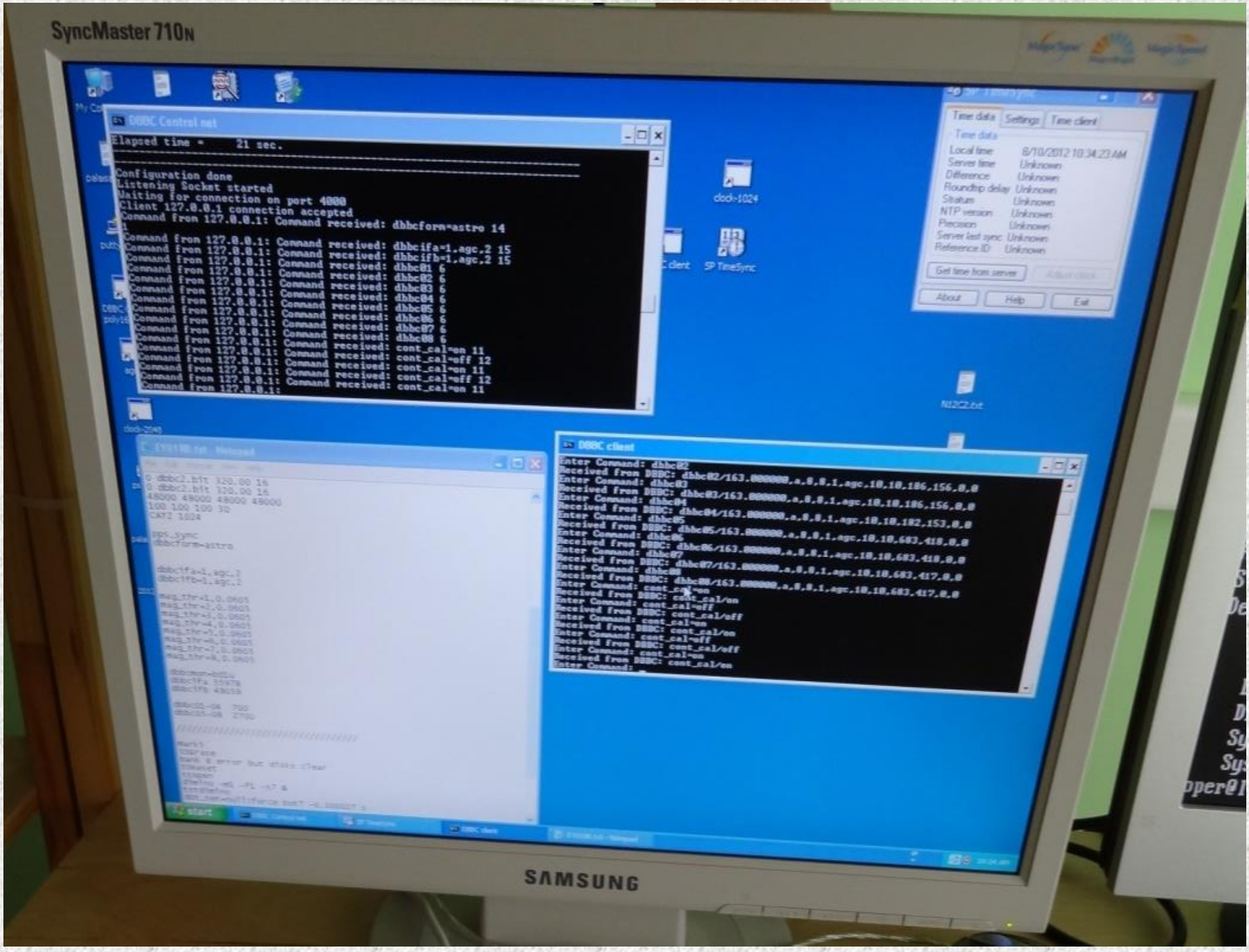
c:\DBBC_conf\dbbc_config_file_101.txt

c:\DBBC_conf\FilesDBBC\dbbc2_ddc_v101.bit

c:\DBBC\doc\DBBC2 DDC command set v101.pdf

- c:\DBBC_conf\dbbc_config_file_101.txt

```
1 dbbc2_ddc_v101.bit 597.00 8
1 dbbc2_ddc_v101.bit 682.00 8
1 dbbc2_ddc_v101.bit 853.00 8
1 dbbc2_ddc_v101.bit 938.00 8
1 dbbc2_ddc_v101.bit 597.00 8
1 dbbc2_ddc_v101.bit 682.00 8
1 dbbc2_ddc_v101.bit 853.00 8
1 dbbc2_ddc_v101.bit 938.00 8
1 dbbc2_ddc_v101.bit 597.00 8
1 dbbc2_ddc_v101.bit 682.00 8
1 dbbc2_ddc_v101.bit 853.00 8
1 dbbc2_ddc_v101.bit 938.00 8
1 dbbc2_ddc_v101.bit 597.00 8
1 dbbc2_ddc_v101.bit 682.00 8
1 dbbc2_ddc_v101.bit 853.00 8
1 dbbc2_ddc_v101.bit 938.00 8
0 fila10g_v2.bit
38000 38000 38000 38000
100 100 100 100
CAT2 1024
```


SyncMaster 710N
DBBC Control nat
Elapsed time = 21 sec.
Configuration done
Listening Socket started
Waiting for connection on port 4000
Client 127.0.0.1 connection accepted
Command from 127.0.0.1: Command received: dbbcform=astro 14
Command from 127.0.0.1: Command received: dbbcifa=1,agc,2 15
Command from 127.0.0.1: Command received: dbbcifb=1,agc,2 15
Command from 127.0.0.1: Command received: dbbc01 6
Command from 127.0.0.1: Command received: dbbc02 6
Command from 127.0.0.1: Command received: dbbc03 6
Command from 127.0.0.1: Command received: dbbc04 6
Command from 127.0.0.1: Command received: dbbc05 6
Command from 127.0.0.1: Command received: dbbc06 6
Command from 127.0.0.1: Command received: dbbc07 6
Command from 127.0.0.1: Command received: dbbc08 6
Command from 127.0.0.1: Command received: cont_cal=on 11
Command from 127.0.0.1: Command received: cont_cal=off 12
Command from 127.0.0.1: Command received: cont_cal=on 11
Command from 127.0.0.1: Command received: cont_cal=off 12
Command from 127.0.0.1: Command received: cont_cal=on 11
DBBC client
Time data
Settings
Time client
Local time 8/10/2012 10:34:23 AM
Server time Unknown
Difference Unknown
Roundtrip delay Unknown
Stratum Unknown
NTP version Unknown
Precision Unknown
Server last sync Unknown
Reference ID Unknown
Get time from server
About
Help
Exit
SP TimeSync
N12C2.txt
SAMSUNG

ESF
EIROPAS SOCIĀLAIS FONDS

EIROPAS SAVIENĪBA

VENTSPILS AUGSTSKOLA

VIRAC

Thank you for attention