DIGITAL BACKENDS VLBI2010

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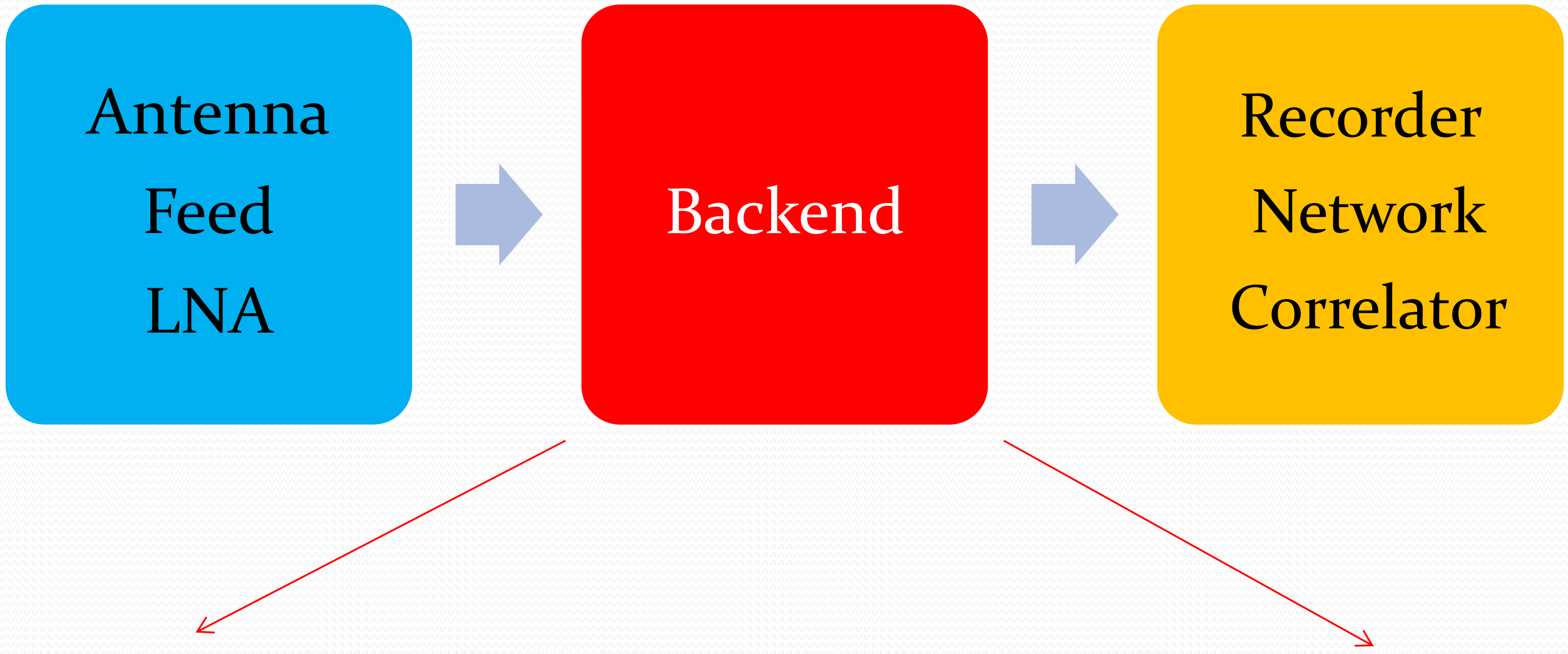
VLBI2010 Digital Backend Summary

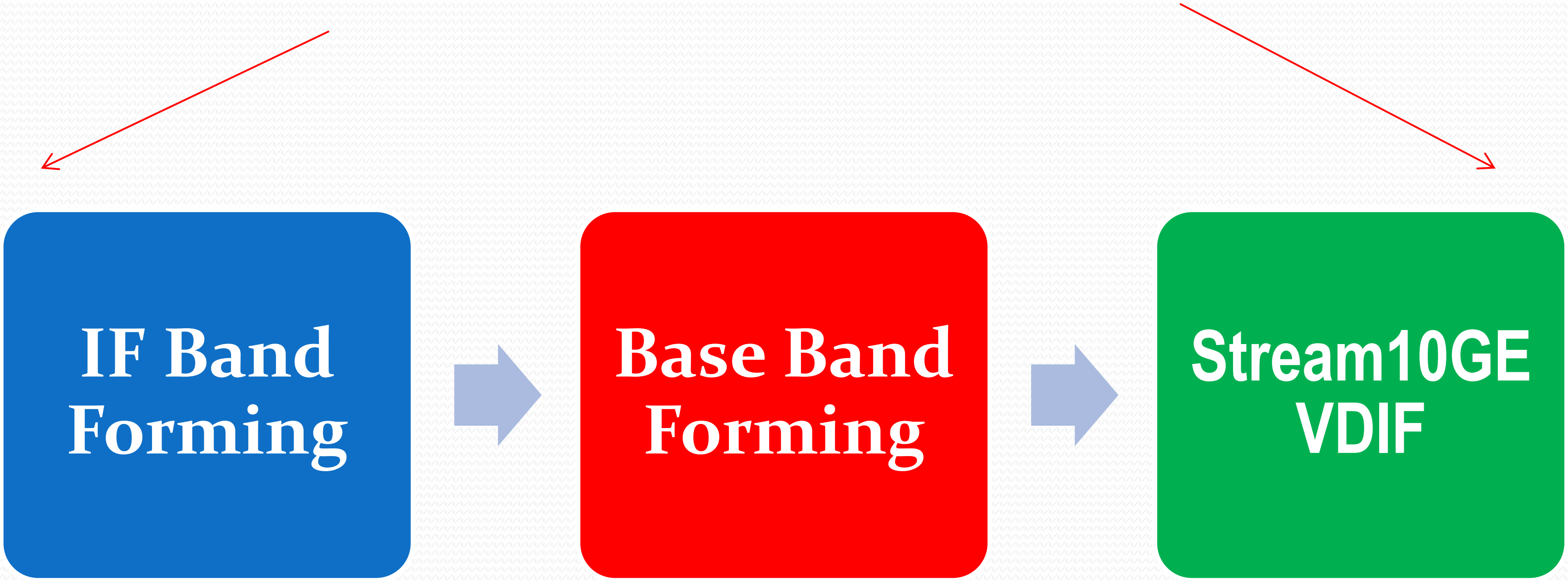
- General Functionality
- Architecture
- Specifications
- Additional Features
- Systems available/under development

General Functionality
VLBI2010 Schematic Block

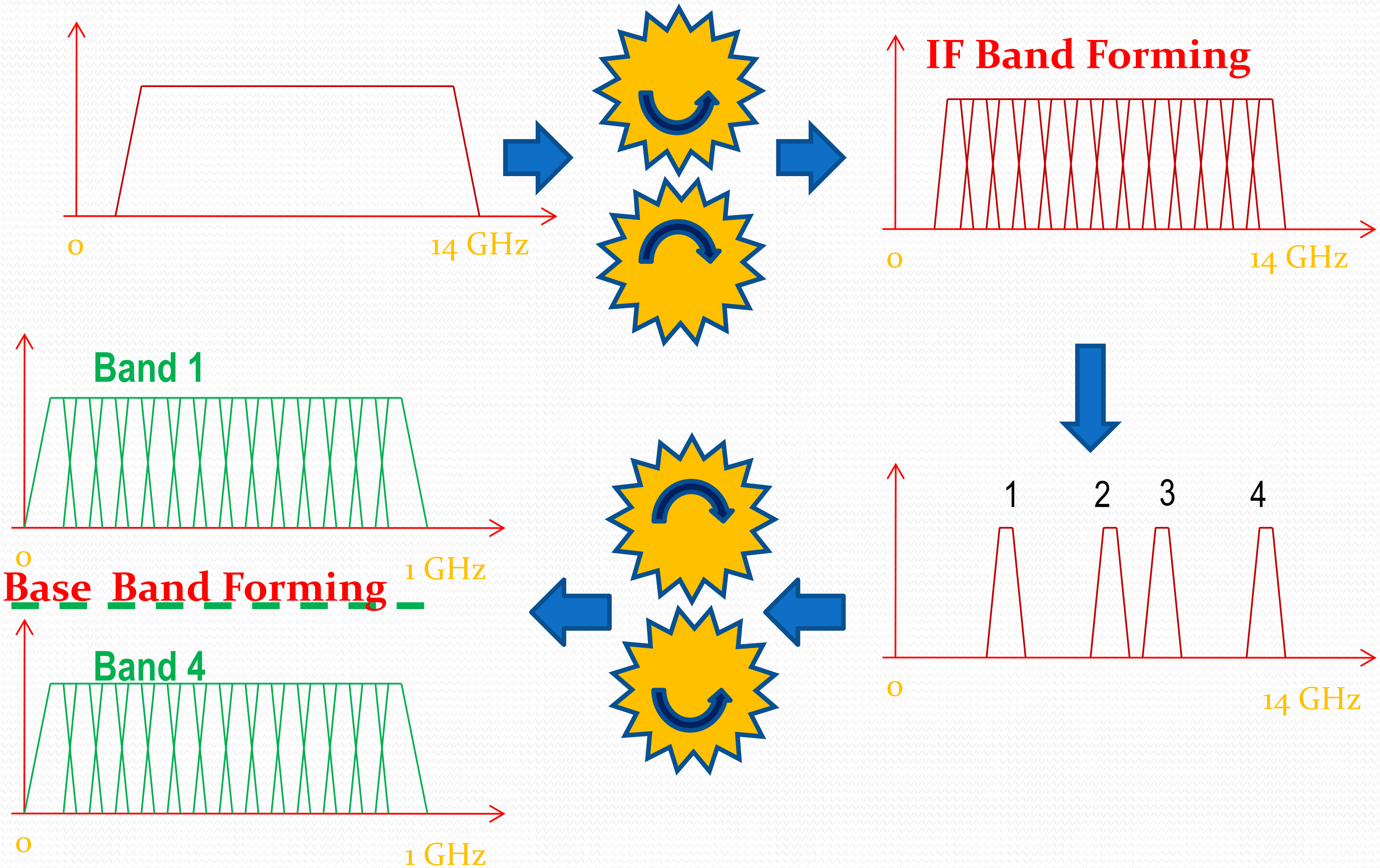


General Functionality

Backend Schematic Block



VLBI2010 Conversion Chain



VLBI2010 Backend
General Specifications

- Input RF band: 2 – 14 GHz, 2 polarizations
- IF band forming: 4 IFs x 2 polarizations = 8 IFs
- IF bandwidth: 1 GHz (single band or 512+512 MHz)
- Base Band forming:
  - real 32 x 32 MHz bwd x 2-bit = 4 Gbps/IF
  - complex 16 x 32 MHz bwd x (2+2)-bit = 4 Gbps/IF
- Output data rate <= 32 Gbps, scalable with factor 2
- Output over 10GE streams, 4-8 Gbps capable: 8-4 streams
- VDIF payload: multi-channel single-thread, single-channel multi-thread

VLBI2010 Backend
IF Band Forming

Functionality:

- **Select 4 (8) slices x 2 pol, 1 (0.5) GHz bwd, inside 2-14 GHz**

Examples:

- **UDC, analog (MIT Haystack)**
- **ADB3, digital (INAF/MPI)**
- **Other developments ?**

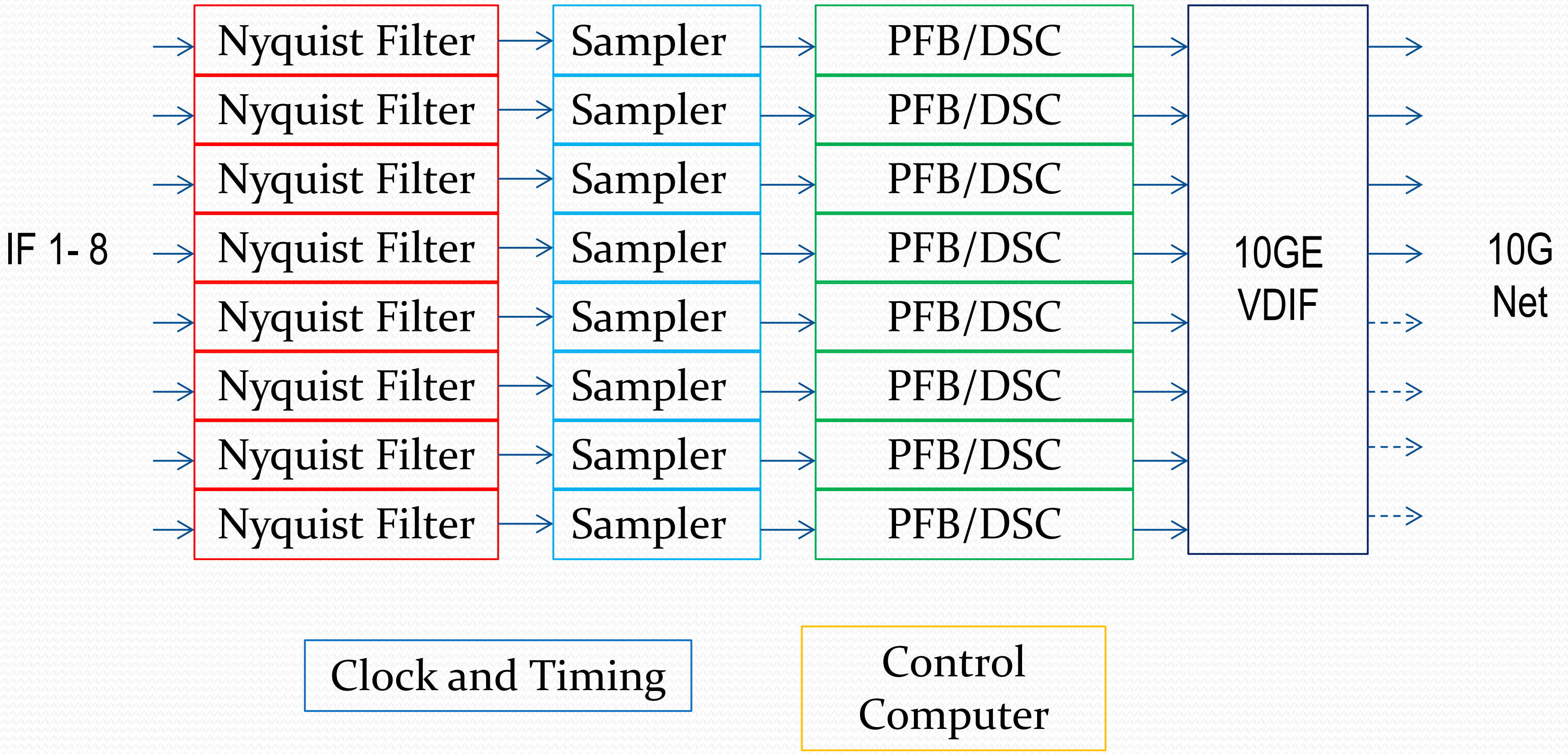
VLBI2010 Backend
Base Band Forming

Digital implementation

Functionality:

- PFB (Polyphase Filter Bank) architecture
- Produce 32 (16 +16) slices x 32 MHz bwd x 2 pol, ea. 1 (0.5+0.5) GHz bwd
- Full data rate 64MHz x 2bit x 32ch x 4 IF x 2 pol = 32 Gbps
- DSC (Direct Sampling Conversion) architecture
- Produce 4 (8) slices x 1024 MHz bwd x 2 pol, for any 1 (0.5) GHz bwd
- Full data rate 2048 MHz x 2bit x 4 IF x 2 pol = 32 Gbps
- Full data rate 1024 MHz x 2bit x 8 IF x 2 pol = 32 Gbps

Base Band Forming Schematic Block



Specification (proposal)
Clock and Timing Generation

- Sampling clock,1024 or 2048 MHz, generated by a dedicated synthesizer phase locked to the H-Maser reference frequency (5 MHz, 10 MHz, 100 MHz)
- Phase noise of the synthesizer must be optimized:
  - spurious signals (no harmonic) < - 90 dBc
  - harmonic suppression, 2^{nd} < -30 dBc, 3^{rd} < - 40 dBc
  - normalized 1/f noise @10KHz offset < -90 dBc/Hz
- 1PPS for time synchronization, phase related to the reference clock
  - 1PPSHR lasting one period of sampling clock

Specification Proposal
Clock and Timing Generation

Optional but highly recommended:

Buffered output signal as monitor of:

- Sampling clock
- Output clock
- Internal running 1PPS
- 1PPSHR

Specification (proposal)
Pre-Base Band Forming

- Before sampling the band needs to be defined to avoid aliases
- Analog IF forming requires analog filters
- Band-pass width defined by the sampling clock (Sclk/2)
- In/out band discrimination > 45 dB
- Cut-off frequency defined at about -6 dB
- High number of poles (> 9) to minimize aliasing from adjacent Nyquist zones
- Ripple minimized and phase linear in band (ex. Butterworth)
- IF Total power measurement
- Automatic gain control: full range 32 dB, steps 0.5-1 dB

Note: Digital IF forming defines band-shape in the conversion process so doesn't need analog filters

Specification (Proposal)
Base Band Samplers

- It's the main element creating the information you have to deal with (very difficult to recover if corrupted here)
- Multi-Nyquist zones capability: >=3
- Number of bits >= 8
- ENOB (overall accuracy) >= 6,6 (SNR >= 42dB)
- Digital differential multiplexed output code
- Serial output desirable
- Output known pattern for debug

Specification (Proposal)
Base Band Forming

Firmware capability in PFB mode:

- Generates an integer number of 32 MHz channels covering the entire IF
- Number of taps = n*256, n integer
- Maximum ripple in band +- 0.5 dB
- Total Power Measurement in each channel, hardware integration time =1s, software integration time 1 - 60 s
- Dynamic 2-bit representation from TP, setting time = 1s
- Fully flexible or standard defined modes output channel selection

Specification (Proposal)
Base Band Forming

Firmware capability in DSC mode:

- Generates a multiplexed version of the entire IF input band
- Maximum ripple in band is the pre-sampling filter ripple
- Total Power Measurement in each IF, hardware integration time =1s, software integration time 1 - 60 s, usable as input of the pre-sampling agc control
- Dynamic 2-bit representation from TP, setting time = 1s

Specification (Proposal)
Base Band Forming

Optional but highly desirable:

- Statistics of the states measurements in the output channels
- Multiple Cal Tone detection (as many as possible at the same time)
- PFB with 8MHz channels to help for RFI (difficult to be achieved at this stage)
- Analogue representation for a selected converted band
- Programmable input tone generator in replacement of sampler data
- Output known pattern for debug

Specification (Proposal)
10GE Output Stream

Output is a set of 10GE connections (optical or copper):

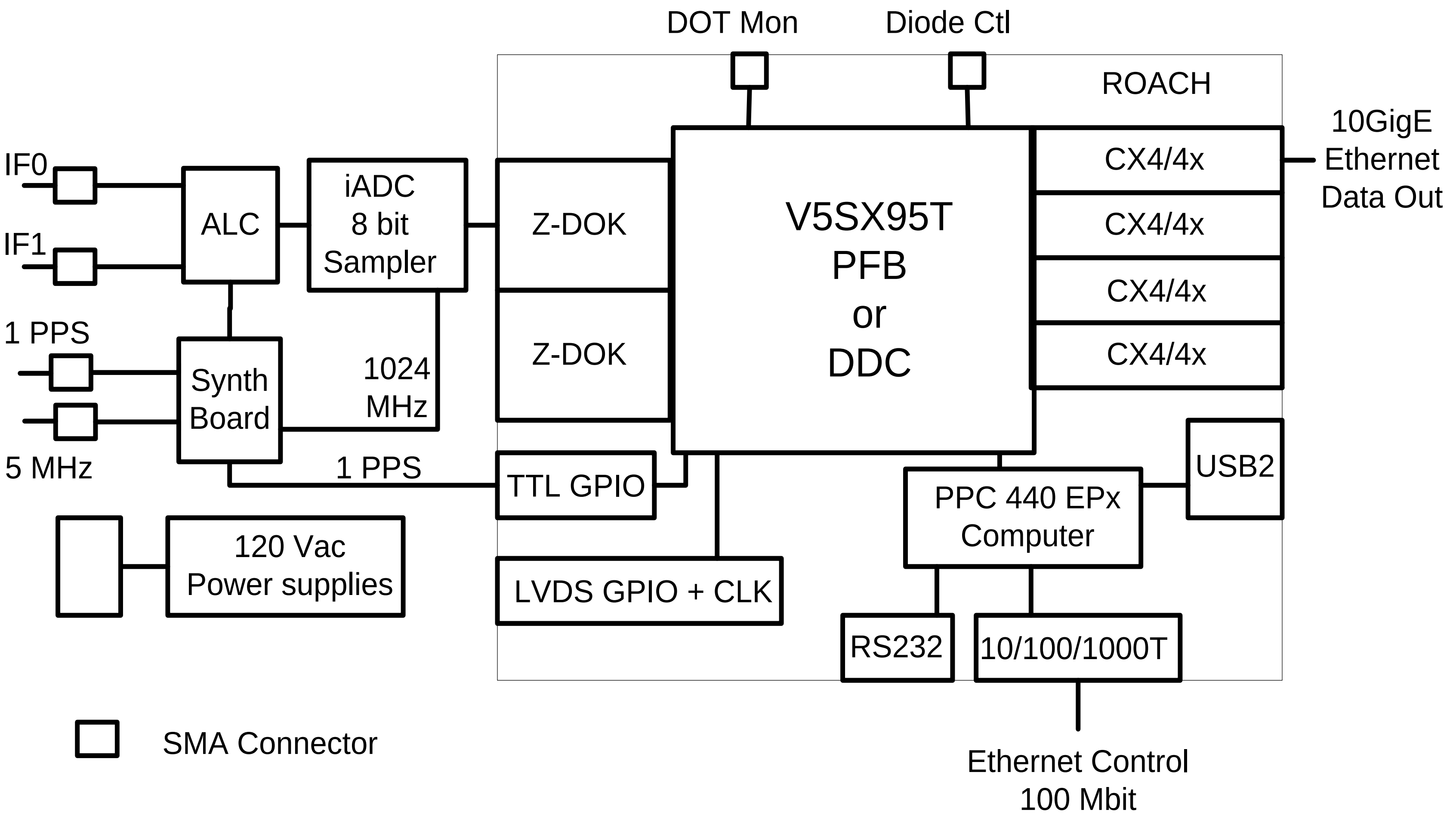
- VDIF - Multichannel single thread
- VDIF – Corner turned data with multiple threads carrying single band channels
- Multiple destination address for the multiple threads in the data streams
- Highly desirable 40GE adoption in the next few years

Digital Backend Systems Available

- RDBE Haystack
- DBBC2010 & DBBC3
- China (see poster, *Xiuzhong Zhang*)
- Japan (see poster, *Yusuke Kono et al.*)
- Russia (see poster *Marshalov and Novov*)

RDBE-H Block Diagram

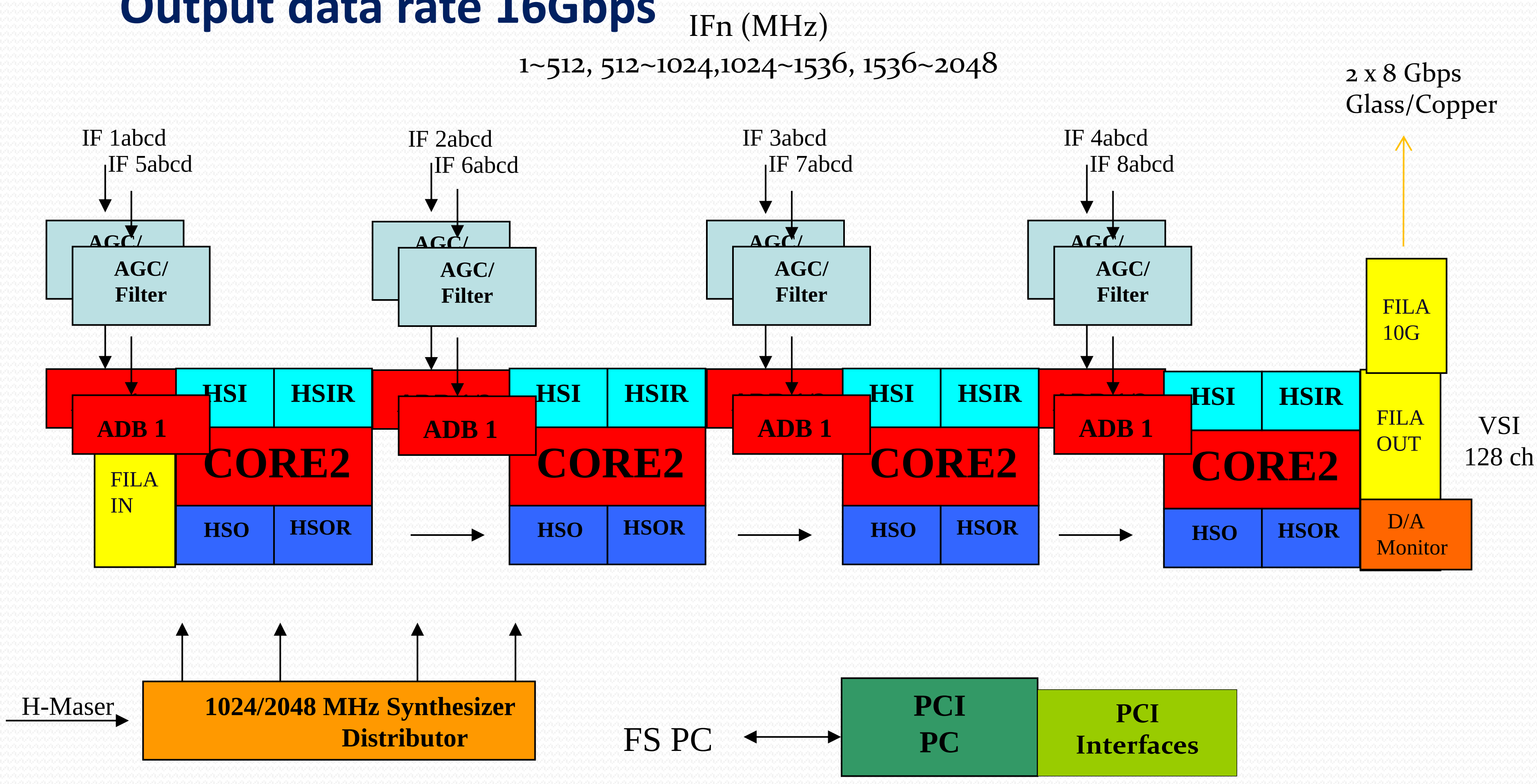
(common hardware for NRAO and Haystack)



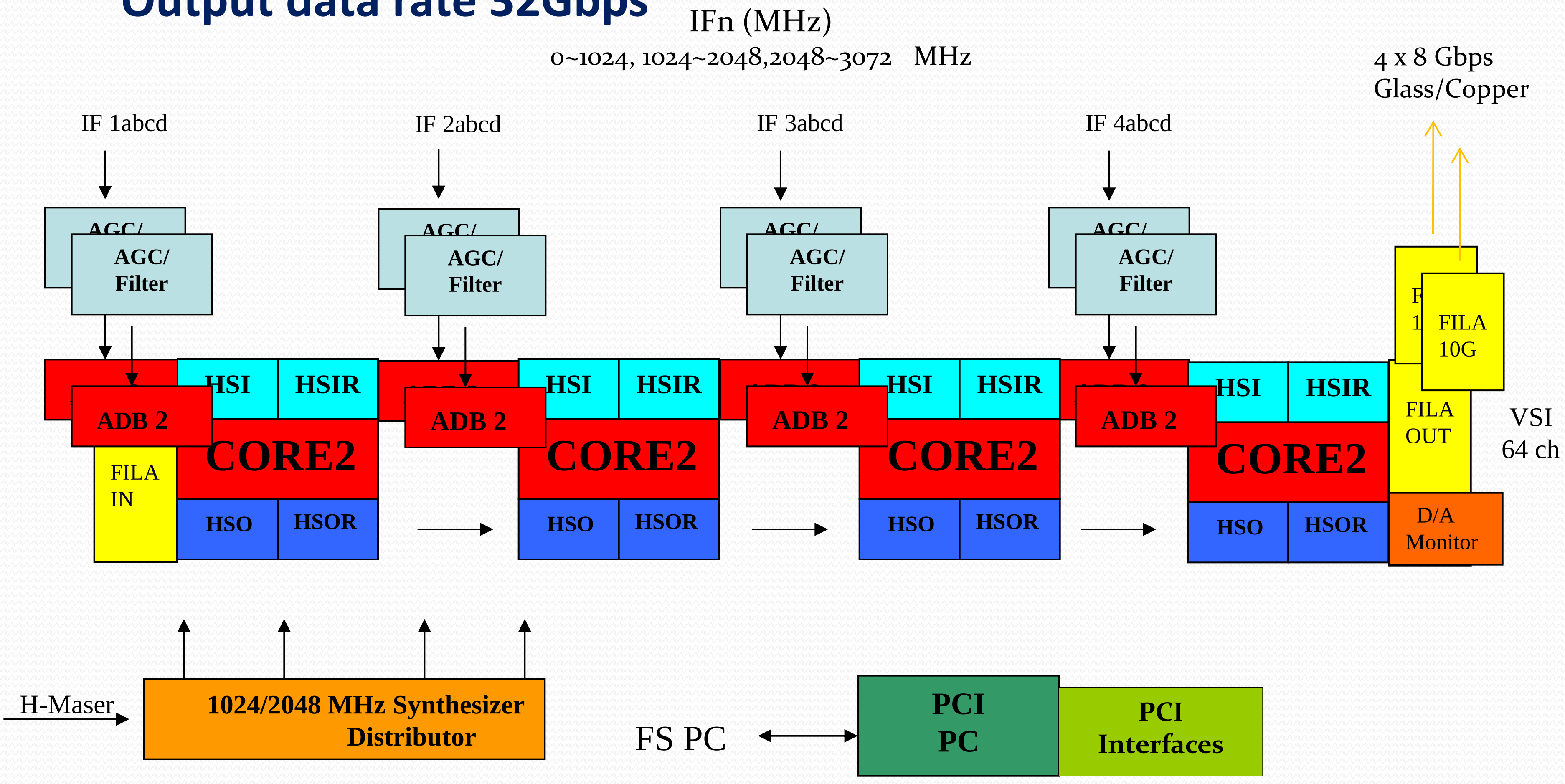
RDBE Firmware

- 3 Personality types (FPGA code)
  - Polyphase filter bank (pfbg) Version 1.4 (Haystack)
    - Input is two 512MHz IFs
    - Output is sixteen of 32 possible 32-MHz channels on one CX4
    - Output is 5008-byte packets in Mark5B format
  - Quantize only (called pfba even though no pfb) (Haystack)
    - Input is four 512 MHz IFs
    - Each input is 2-bit quantized only
    - Output is on two of the four 10Gbps CX4 interfaces
      - 4Gbps / interface
      - 8224-byte packets in VDIF format.
  - Digital down converter (ddc) (NRAO)
    - Input is two 512MHz IFs
    - Output anticipated to be eight tunable channels (two working now)
    - Bandwidths ranges down in binary steps from 64 MHz to 62.5kHz
    - Output is 5008-byte packets in Mark5B format

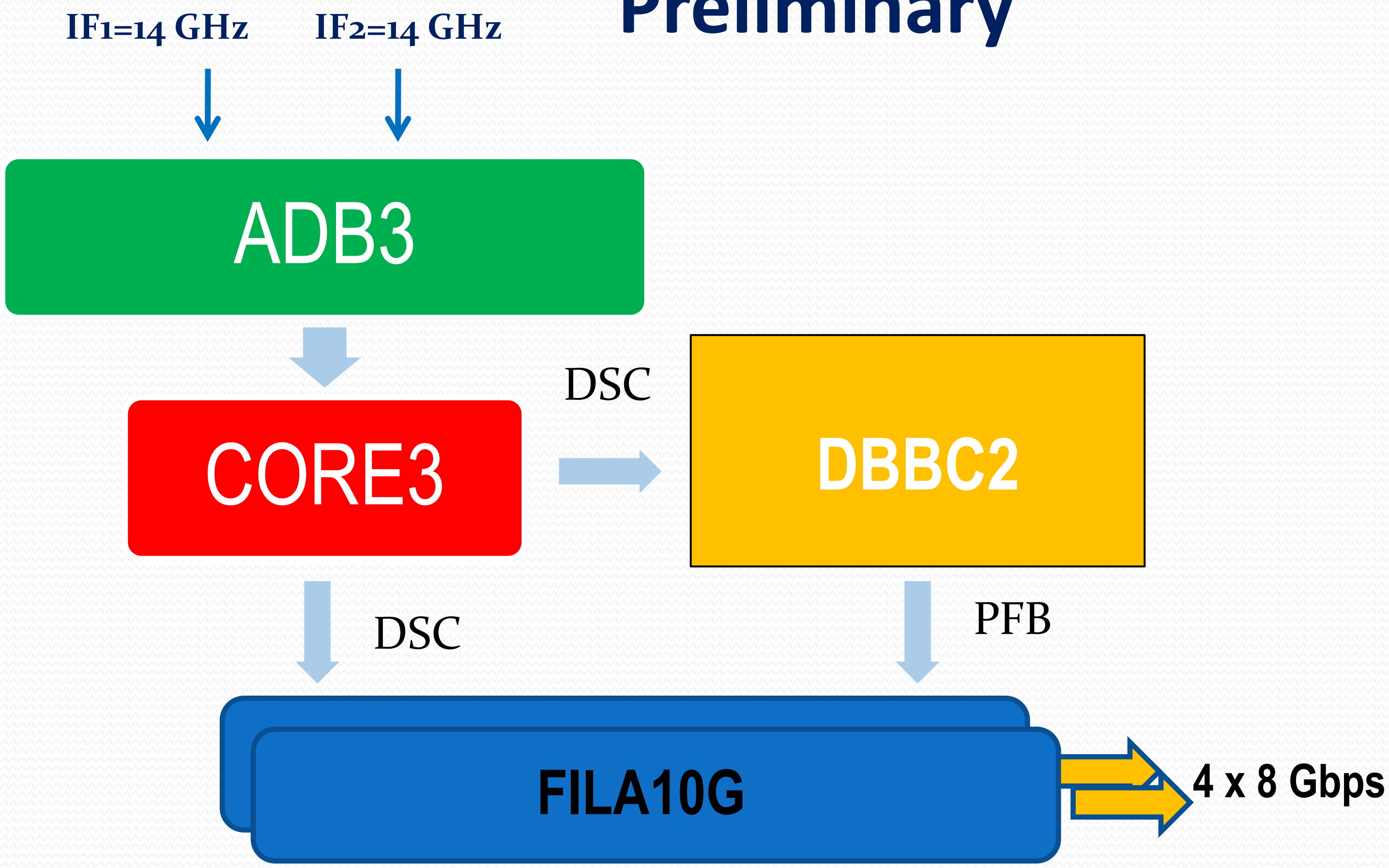
DBBC2010 Architecture A
8 IFs @ 512 MHz
Output data rate 16Gbps



DBBC2010 Architecture B
8 IFs @ 1024 MHz
Output data rate 32Gbps



DBBC2010 Architecture C Preliminary



DBBC2010

- DBBC2010 architecture A and B are available today
- HAT- Lab is the contact point
- Upgrade kits are available for systems on the field