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DBBC3 - Full digital EVN and VLBI2010 Backend, Project Progress

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Abstract DBBC3 is a project to develop the third generation of a digital backend system for VLBI and other scientific applications. The development started about ten years ago and evolved in the course of time by improving all its components, hardware, firmware and software, passing from DBBC1 to DBBC2. Now the latest and third generation will allow to fully implement digitally all the functionality required of a complete VLBI backend for the EVN and VGOS (formerly named VLBI2010), with a maximum output data rate in the range from 32 Gbps to up to 128 Gbps. The architecture and adopted methods are described.

Keywords Digital Backends, VGOS

1 Introduction

The development of the DBBC started in the first years of the new millennium (Tuccari (2004a) & Tuccari (2004b)). In the first few years ad hoc laboratory experiments and experiments with real sky signals had indeed demonstrated that it could be possible to emulate the entire functionality of the MK4 VLBI analogue terminal with a fully digital backend. In the digital process the analogue signal available as IF from the receiver is, after potential equalization and gain adjustments, immediately converted to a digital representation before any mixing or filtering stage as is required for VLBI to produce recordable sub-bands. Before this time the digital mixing/filtering stage could not be fully implemented digitally at a reasonable cost, and moreover it was a technical challenge due to the wide band and the high frequencies involved. With progressive improvements the DBBC project evolved to allow an input bandwidth of up to 4×1 GHz.

The first DBBC version (DBBC1) was a backwards compatible replacement of the existing VLBI terminal, while with the DBBC2 additional observing modes became available, which did not exist in the analogue backend. The enhanced version of the DBBC2 for VLBI2010 (Niell et al. (2005)) the DBBC2010 (2009 to date) is compatible with the proposed VGOS observing mode.

One way to increase the sensitivity of a VLBI network is to increase the observing bandwidth. With new wide-band receivers the demand for backends which can handle bandwidths of several GHz has arisen. Also the EVN has been increasing its maximum data rate from a maximum of 1 Gbps with the MK4 analogue backend to a maximum of 4 Gbps with the present DBBC2 — a data rate which is being tested in the EVN now.

In preparation for receivers and IF systems which will deliver up to 4 GHz (and later more) bandwidth to the backends, it was felt necessary to develop a system which can process an instantaneous bandwidth of 4 GHz per polarization as a minimum. The resulting output data rate for a dual polarisation receiver should be at least 32 Gbps, with the option of 64 Gbps for a system with four IFs. Such a backend is the intermediate goal of the DBBC3 project.

The specifications of VLBI2010 define a set of requirements of the receiving/backend system to achieve the goal of greatly improved geodetic measurement precision. The telescopes will operate in a single broad band ranging from 2 to 14 GHz observing in dual linear polarization. Inside this frequency range a subset

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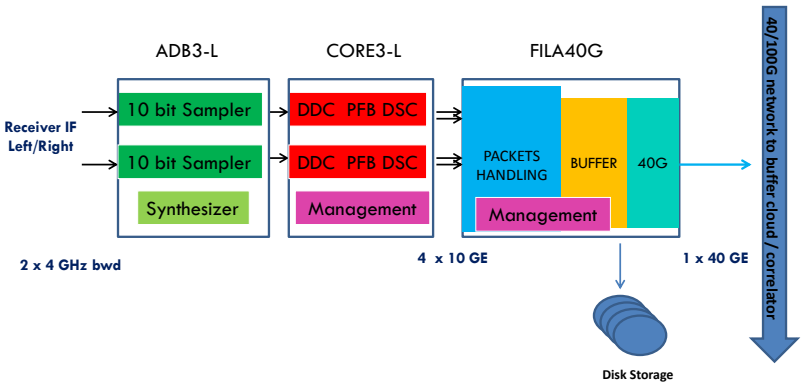

Fig. 1 DBBC3-L block diagram with sampler ADB3-L, processor CORE3-L, and FILA40G packetizer.

of four 1024 MHz wide pieces will be selected, in both polarizations, so that a total of eight portions of 1 GHz will have to be processed. This will allow bandwidth synthesis (phase slopes fitted over a wide frequency range) for a much wider portion of the spectrum than is possible with the present system.

Such a wide input band could also be of great interest for astronomy because of the significant increase in sensitivity it will offer. Being able to process an entire 14 GHz wide piece of band could be a quantum leap in the digital radio astronomy data acquisition. This goal is very ambitious and its implementation in a radio astronomy backend would be a novelty. To digitally sample and process the whole 14 GHz wide band or a number of sub-bands thereof is the final goal for the DBBC3 project.

2 DBBC3 Structure

For the DBBC3 system there are some obligatory requirements: it has to be backwards compatible with the existing backends of the previous generations and has to be able to offer the new functionality for a very wide band. In particular it should incorporate all the required functionality, for the planned goals of the EVN (min 2×4 GHz bandwidth) and VLBI2010 (2×14 GHz bandwidth). As many stations observe for both networks a single system is mandatory. Flexibility is a requirement due to the different radio telescopes and their dissimilar receivers and IF systems in terms of number and type of IFs.

To be compatible with the existing systems, the new hardware needs to be mechanically and electrically level-compatible. This aspect is useful because existing DBBC2 and DBBC2010 backends in the field could be upgraded to meet the new performance requirements by replacing some of the old components with DBBC3 hardware.

The much increased capability of the new backends requires new hardware parts, together with new firmware. A clear development path has been laid-out to minimise the risk in the project. In a first step a DBBC3-L will be developed which can be seen as a fully qualified 4 GHz DBBC, but at the same time the final goal to achieve a 14 GHz DBBC3-H is pursued.

The main features of the DBBC3-L system are:

- Maximum number of wide input IFs: 4 (typ. 2)
- Instantaneous bandwidth in each IF : 4 GHz
- Sampling representation: 10 bit
- Processing capability N × 5 TMACS (multiplication-accumulations per second), with N number of processing nodes
- Output data rate: max 64 Gbps
- Compatibility with the existing DBBC environment.

The main features of the DBBC3-H system are:

- Max number of wide input IFs: 4 (typ. 2)
- Instantaneous bandwidth in each IF: 14 GHz
- Sampling representation: 8 bit
- Processing capability N × 5 TMACS (multiplication-accumulations per second), with N number of processing nodes
- Output data rate: max. 896 Gbps
- Compatibility with the existing DBBC environment.

In figures 1 and 2 the schematic views of the DBBC3-L and DBBC3-H are shown.

The structure of the system is straightforward. Due to the very broad band to be sampled a dedicated receiver named DBBR (Digital Broad Band Receiver) is developed including the entire digital section. After initial amplification of the signal collected by the feed

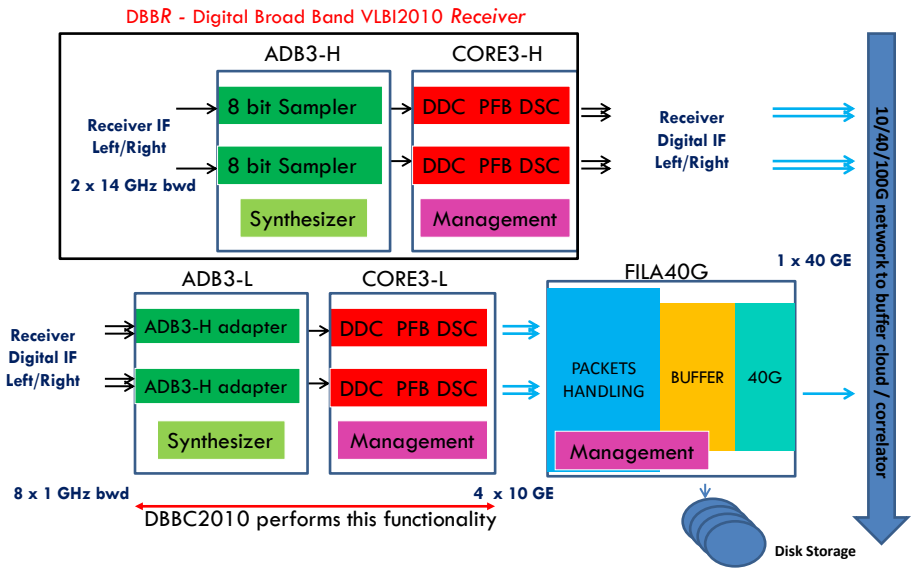

Fig. 2 Complete DBBC3 block diagram. Top: DBBC3-H as Digital Broad Band Receiver. Bottom: DBBC3-L.

in both polarizations, two IFs 14 GHz wide are sampled with 8-bit representation. Next this data is transferred to a dedicated processing node. The processor extracts from the digital data eight streams, portions of the band, in DDC (tunable digital down converter) and PFB (fixed polyphase filterbank) modes, from the entire input range. These tuned/filtered 'digital IFs' are transferred and processed in the DBBC3-L section to further extract and select portion of bands to produce VLBI-compatible output VDIF packets.

The last element of the chain is the FILA40G subunit whose function is to condense the data onto single optical fibres at a data rate of 40 Gbps and to handle the data at network packet level. A dedicated version, the FILA40G-ST, will in addition have storing capabilities.

3 ADB3-L/H components

The massive sampling is performed by a state of the art sampler chips. A single ADB3-L has four complete samplers on-board, with the possibility to arrange them for a variety of functionalities, single and multiple, real or complex sampling. For example in real mode the four samplers can be fed with a single input signal 4 GHz wide, or they can be fed with two signals of 2 GHz instantaneous bandwidth each, or finally with four signals 1 GHz bandwidth.

The ADB3-H single board sampler similarly has the capability to digitise up to four independent 14 GHz bands. Sampled data have to be transferred to the processing stage. Due to the high data rate a parallel bus cannot be implemented, because the very large number of differential lines required and the high operational frequency. Pre-processing is used to pipe this large data rate to a manageable number of serial connections for linking the Sampler with the Processing unit.

Data coming from the sampler board ADB3-L/H are routed to the processing node CORE3-L/H using the lanes of the high speed input bus. The CORE3-L/H board is capable of processing data in different ways: with DSC (Direct Sampling Conversion) resulting in one single sampled sub-band, DDC (Digital Down Converter) and PFB (Polyphase Filter Bank) personalities. Additional capabilities will allow spectroscopic and polarimetric observations.

From the pool of channels a subset is selected according to the desired output data rate defined by the observer or allowed by the recording media or the network capacity. The data is output via the high speed output bus. Additional input and output connectors are available to maintain the compatibility with the DBBC2 stack of boards.

The large DSP resources available in the FPGA chosen for the CORE3-L allows digital filters in the class of 100 dB in/out band rejection. This feature is required for the expected presence of large RFI signals in the very wide input band. This very strong discrimination together with the tuning ability should be sufficient to obtain useful and clean pieces of the down-converted observed band.

As an alternative input the CORE3-L board will be able to receive data packets from a block of ADB3-

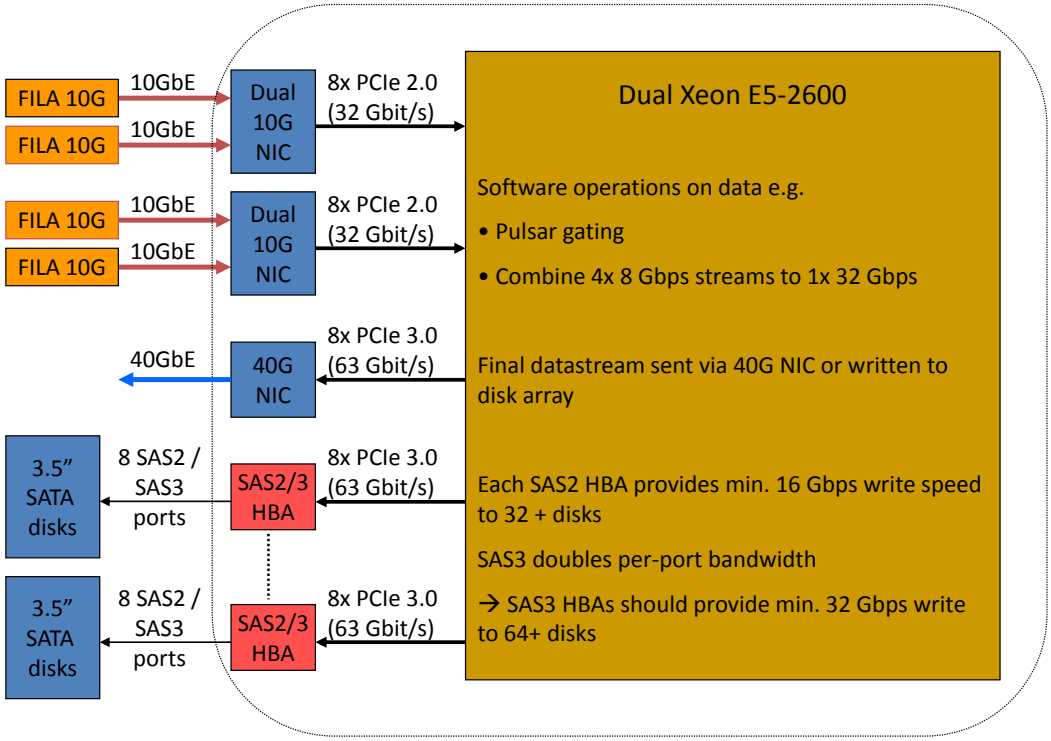

Fig. 3 Block diagram of the FILA40G unit. Input 4×1 Gb. Output: 1×40 Gb to fibre or alternatively to disks.

H/CORE3-H units to be routed to the rest of of the system for additional data processing.

Data from the converted bands are finally transferred to the network controller FILA40G as multiple 10 GE connections. The number of connections is then accumulated into a 40 GE data stream to be transferred to the final destination points. Such final points could be recorders, nodes of VLBI correlators or a buffer cloud. In addition to the 40 GE network capability the FILA40G unit will be able to manipulate the data packets in order to perform functions like corner-turning, pulsar-gating, packet filtering and routing, burst mode accumulation, and others that could be required at the packet level as soon as the VLBI methods evolve. In addition a dedicated version will be provided which can include storage elements for data buffering and recording. The FILA40G block schematic view is shown in figure 3.

Most of the data communications in the system will be implemented making use of a collection of serial point to point connections to represent the aggregate block information. In order to maintain the data block structure representing in a complete form the single band information the quantity sbit (serial bit) is defined. So the number of sbit is the number of serial links, running at the indicated data rate, necessary to fully represent the information belonging to a single information quanta like in our case is a complete sampled input band. The wide bandwidth involved in the process, and so the very high data rate necessary to represent it, is greatly simplified by this compressed definition, that we adopt and use for all the project description. The schematic block in figure 4, shows in such terms the complete system data flow.

4 Preliminary Results

The DBBC3 project is progressing as planned and the first prototypes are under development and construction. These will produce the proper information and know-how to proceed to the final version. The evaluation performed in the laboratory until now shows that the project will reach the planned goals in the scheduled time without big risks or problems, despite of the very challenging performance to be obtained.

Tests and experiments performed with the ADB3-H and ADB3-L first prototypes are available and in particular showed that direct data conversion to the digital domain for the full 14 GHz band is possible, without the need for an initial analogue down conversion.

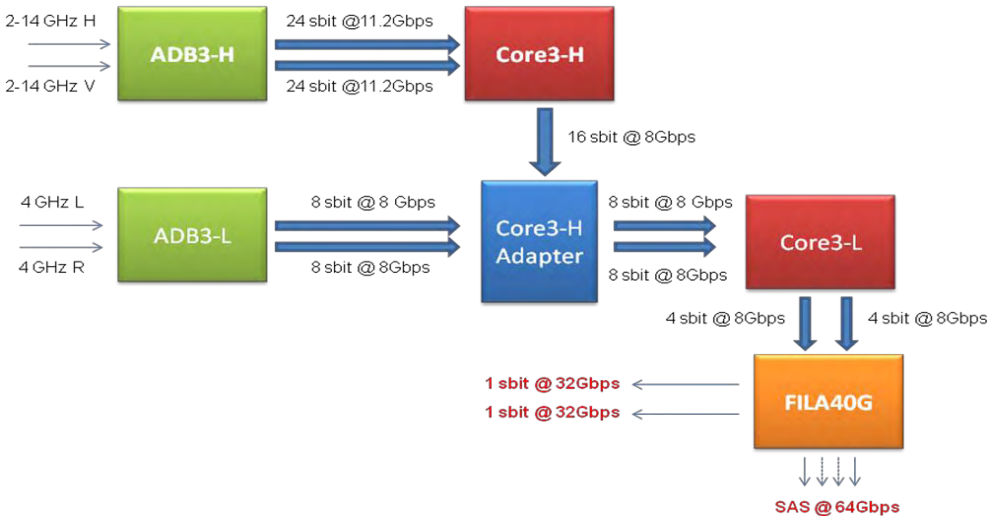

Fig. 4 DBBC3 Data flow. Data sampled and preprocessed with the H-version is fed into the data path of the L-version via an adapter.

This represents a huge challenging and intriguing step ahead in the simplification and in the improvement of the VGOS electronics which should significantly reduce the system cost.

The very challenging firmware development, for the huge data rate and very fast clocks involved, is underway on hardware platforms with the FPGA device to be used for both Core3-L and Core3-H.

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