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ORIGINAL ARTICLE

A wideband multirate FFT spectrometer with highly uniform response

Giovanni Comoretto · Andrea Melis · Gino Tuccari

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Abstract An integrating spectrometer based on a two-stage polyphase digital filter bank (PDFB) algorithm is described. The first PDFB operates on a time multiplexed wideband signal, with a bandwidth up to 1 GHz. The second PDFB is performed in parallel over couples of overlapping channels from the first filterbank. The design automatically deletes the unused portions of the first filterbank channels, providing a seamless, uniform channelization of the input band. The design has been implemented and tested on the VLBI DBBC platform, using a single Xilinx XC5VLX220 FPGA.

Keywords Radioastronomy · Spectroscopy · Polyphase FFT

1 Introduction

Radioastronomic signals have usually a very large instantaneous bandwidth, in the range of several hundred MHz to a few tens GHz.

G. Comoretto (✉)
INAF-Osservatorio Astrofisico di Arcetri, Largo E. Fermi 5, Firenze, Italy
e-mail: comore@arcetri.inaf.it

A. Melis
INAF-Osservatorio Astronomico di Cagliari, Loc. Poggio dei Pini, Strada 54, Capoterra (CA), Italy
e-mail: amelis@oa-cagliari.inaf.it

G. Tuccari
INAF-Istituto di Radioastronomia, Noto VLBI Station, Contrada Renna Bassa, 96017 Noto (SR), Italy
e-mail: g.tuccari@ira.inaf.it

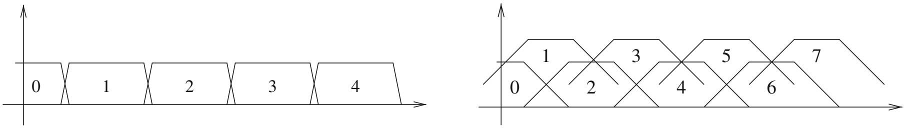

Fig. 1 Frequency channelization for a polyphase filterbank. *Left* non overlapping sub-channels. *Right* sub-channels overlapping by 50%

Digital signal processing is however limited by the maximum clock speed of large scale logic that, for systems employing Field Programmable Gate Arrays, is around a few hundred MHz. Massive parallel processing is therefore a necessity. Multiplexing in time, with several processors operating in parallel on successive samples, allows to process signals with sampling rate greater than the digital clock frequency, but the computational complexity increases quadratically with the multiplexing factor. Multiplexing in frequency, where the parallel processing is done on separate frequency bins of the input signal, is often preferable, as the computational complexity increases only linearly with the multiplexing factor, but it requires a filter bank on the input signal.

Polyphase digital filterbank (PDFB) have often been used to implement a filter bank. This algorithm (see for example Harris [2]) is a very efficient way to implement a uniformly distributed multi-channel filterbank using a Fast Fourier Transform (FFT). It combines a prototype low-pass filter and a conventional FFT engine producing equispaced translated copies of the prototype filter frequency response. The simplest implementation for this algorithm produces adjacent bands with inevitable small "holes" between them. To overcome this problem, a filterbank with overlapping bands has often been used (Fig. 1).

The overlapping causes however a waste of resources, and various techniques have been used to delete the overlapped regions from subsequent processing. In this work we describe a spectrometer composed of a two-stage polyphase filterbank, in which a second FFT is performed in parallel over couples of overlapping regions from the first FFT. The design automatically deletes the unused portions of each region, providing a seamless, uniform channelization of the input band.

The design has been implemented as part of a scanning FFT spectrometer, used for RFI monitoring at the Italian VLBI radiotelescopes. The hardware platform used is the Italian DBBC, designed for VLBI channelization and data formatting, already available at these telescopes.

2 System description

The system block schematics is shown in Fig. 2. After the analog to digital conversion (ADC) the intermediate frequency signal (IF) samples are parallelized in a deserializer. Time multiplexing factor can be either 8 or 16, for a bandwidth of 0.5 and 1 GHz respectively.

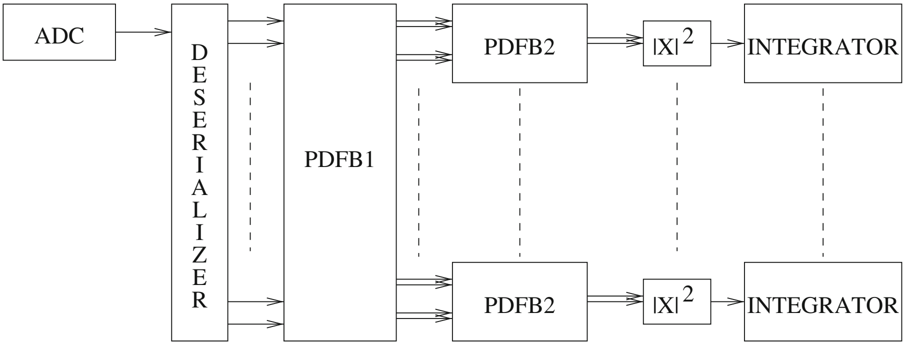

Fig. 2 Block diagram of a two stage polyphase FFT

The digital parallel data are sent to a parallel polyphase filter bank (PDFB1), that divides the input bandwidth into 16 or 32 overlapping regions, with a bandwidth of 128 MHz each and a spacing of 64 MHz. These signals are then analyzed by a serial polyphase filter bank (PDFB2) array.

The first filterbank PDFB1 uses a parallel, decimation-in-time (DIT) FFT architecture, with a FFT length of twice the multiplexing factor. In this way an overlapping of 50% between adjacent FFT outputs is obtained. Only the central half of each region is used. As shown in Fig. 1 only this part of the prototype filter needs to be flat, and the stop band begins at 150% of the Nyquist frequency for the output signal. This drastically reduces the number of taps in the FIR filter architecture.

The FFT engine has been optimized for real input signals. The first two stages of the DIT FFT do not require multipliers, and for subsequent stages multipliers for twiddle coefficients of $\exp(i\pi n/4)$ are optimized using no or two multipliers each instead of four. Outputs are not given for negative frequencies, and the number of butterflies elements in the last two stages are minimized exploiting the complex conjugate relation between positive and negative frequencies. For example, the structure of the 16 channel FFT (shown in Fig. 3) requires only 14 real multipliers. A 32 point FFT requires 54 real multipliers.

Outputs of the first PDFB are sent in couples to a serial PDFB array. Each PDFB2 block consist of a serial polyphase filter which provides the correct insulation between the spectral channels for the next serial decimation-in-frequency (DIF) FFT engine. The standard FFT algorithm is able to produce simultaneous spectra from two independent signals because the N-point spectrum of a single signal is calculated in N/2 cycles. The FFT engine provides the two spectra sequentially, with two spectral outputs computed at each clock cycle.

In a conventional PDFB the spectra of all the sub-channels are entirely processed, and at the end of the integration the *good* portions are extracted

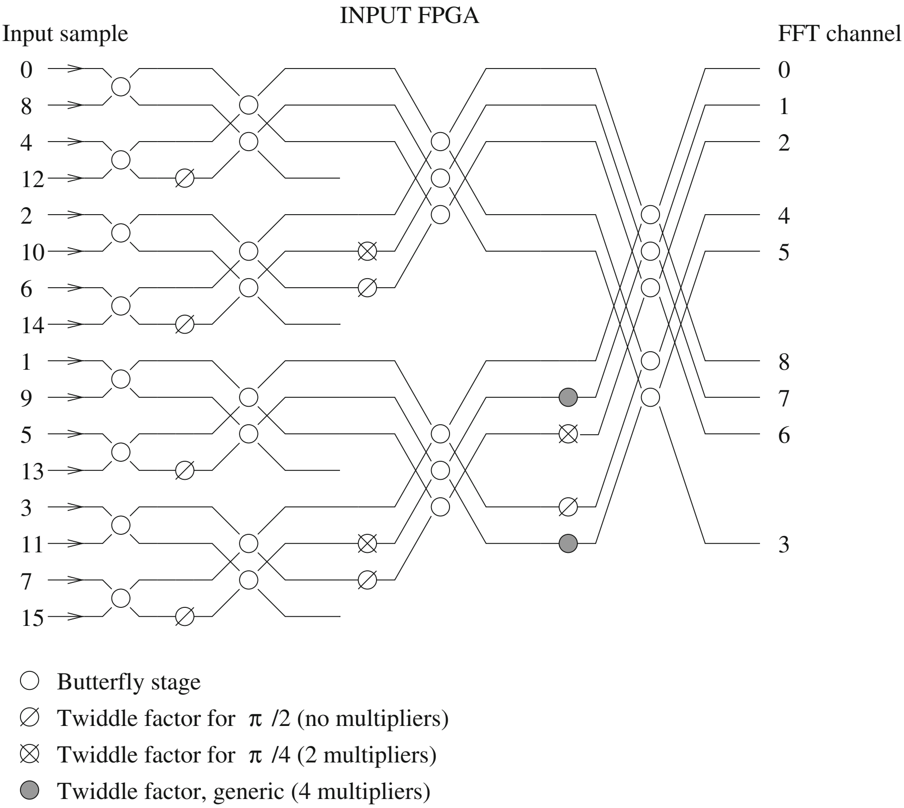

Fig. 3 Structure for a 16 point FFT with real valued inputs. Outputs 3, 6 and 7 are derived from the complex conjugated outputs 13, 10 and 9, respectively

and stitched together. This wastes a considerable amount of resources, especially memory, for information that is successively discarded. The algorithm presented in this paper exploits the parallelism of the FFT engine to discard the unused portions of the spectra as early as possible, thus saving memory and logic resources in the following data processing (correlation, integration).

The DIF FFT algorithm produces spectral points in bit reversal order. The two spectral samples computed by the FFT engine at each clock cycle are always spaced exactly by half band, and therefore we have always one sample in the central (good) portion of the spectrum and the other in the external transition band. Due to the bit reversal order, at each clock cycle the *good* samples are presented alternately on the two outputs. Therefore the selection of the good portions of the spectra is performed by processing alternately one of the two outputs of the FFT engine for every cycle and discarding the other. Figure 4 shows an example with a 8 points FFT engine. Spectral points for the second channel are shown in italics, and good points are marked bold.

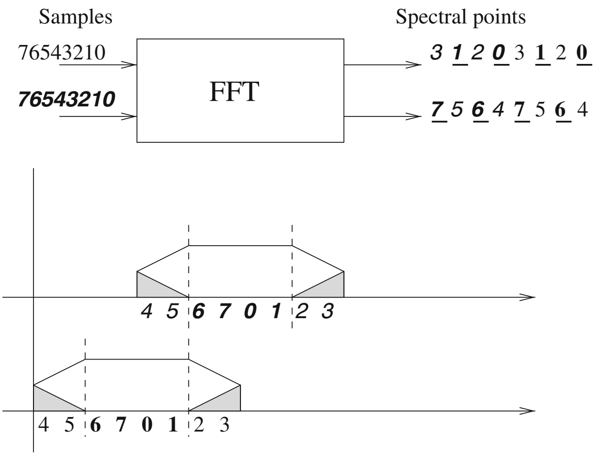

Fig. 4 Eight points FFT division-in-frequency algorithm and the spectral representation of the two signals

3 Implementation and results

The Digital Baseband Converter (DBBC) is a digital platform developed as a replacement for a VLBI Mark5 terminal [3]. The platform is modular, composed of up to 4 ADC boards with 0.5 or 1 GHz bandwidth each, and up to 16 processing (CORE2) boards, each one containing a Xilinx XC5VLX220 FPGA. A general firmware and software framework has been designed to simplify developing of different applications [1]. It takes care of time multiplexing of the ADC samples, general timing and control, and communication with a control computer. The system can be accessed by a TCP-IP port using a standard programming interface.

The system used for this application is composed of a single 1.024 GS/s sampler with 8 bit resolution and a single processing board. The sampler speed limits the input bandwidth to 500 MHz, and the amount of processing hardware limits the functionality of the system. In particular it was possible to implement just two second stage FFT processors, for a maximum instantaneous bandwidth of 256 MHz. A complete system, capable of analyzing instantaneously the input bandwidth, would require two processing boards operating in cascade. The input bandwidth is thus analyzed sequentially and reconstructed on the control computer.

The first stage PDFB provides nine separate outputs: two real, with a bandwidth of 64 MHz, and seven complex, with a bandwidth of 128 MHz. They are considered as nine complex quantities.[1] A multiplexer selects subsequent couples of regions, with the last region analyzed alone. Each region is further divided by the PDFB2 into 1,024 channels, with a channel spacing of 125 kHz,

[1]It is relatively easy to process the two real signals in a single complex FFT. For simplicity we have not introduced the possibility in our design.

for a total of 4,096 usable channels in the input bandwidth. The second stage PDFB uses a serial division-in-frequency FFT architecture.

The FFT output, after the selection of the appropriate portion of each region, is squared and stored in an integration memory. The integration is performed for an integer number of FFT cycles, and the result is then transferred to a transit memory. FFT size is limited by the number of available multipliers in the FPGA. The results can be read from an external computer using the interface developed as part of the DBBC framework architecture [1]. The memory addressing is rewired in order to transparently perform the bit-reversal operation.

3.1 Filter performances

The characteristics of the adopted implementation are summarized in Table 1.

The prototype low pass filter for the first PDFB has a cutoff frequency of 32 MHz ($f_s/32$), stop band beginning at 96 MHz ($3/32\, f_s$), stop band attenuation of 85 dB, and passband ripple of 0.07 dB peak-to-peak. The filter is composed of 64 symmetric taps divided into 16 parallel branches. Twiddle coeffcients are quantized to 18 bit values. The 18×8 bit fixed coefficient multipliers are implemented with general logic.

The polyphase filter for the second PDFB has a length of 4 times the FFT length, requiring eight multipliers for each complex signal. The filter coefficients have been computed by numeric optimization using as a starting guess a shorter filter obtained with the Remez algorithm, interpolated to the final size. Filter response has been chosen in order to obtain a strong uniform stopband rejection of 87–88 dB, starting at ± 1.35 FFT channels from the nominal center frequency. Response is roughly trapezoidal, with a flat region (0.05 dB ripple) 1 channel wide, and two transition regions of 0.6 channels on each side. The line profile has been measured up to the radiometer noise level,

Table 1 System characteristics

Input bandwidth	512 MHz	
Input quantization	8 bits	
Instantaneous analyzed BW	256 MHz	
Spectral points	4,096	
Total multipliers used	120	
1st PDFB	Channels	8
	Isolation	85 dB
	In-band ripple	0.07 dB
	Internal signal precision	26 bits (filter), 18 bits (FFT)
2nd PDFB	Channels	1,024 (512 used)
	Isolation	87 dB
	In-band ripple	0.05 dB
	Internal signal precision	36 bits (filter), 18 bits (FFT)
Spectral resolution	@3 dB	0.17 MHz (1.4 ch)
	@20 dB	0.27 MHz (2.1 ch)
	@87 dB	0.35 MHz (2.7 ch)

around −60 dBc for an integration time of 10 s (Fig. 5). Insulation in excess of 70 dB has been verified with saturated lines.

3.2 Signal level

The typical astronomic signal is composed of a Gaussian noise, possibly contaminated by non-Gaussian RFI. If the total power is dominated by the noise it can be shown that the optimum SNR is obtained for a signal RMS level of 5–13% of the total digital range. For 8 bit quantization the optimum RMS level corresponds to 0.12 times the total quantization range, i.e 32 ADC units (ADU), with a quantization noise of 10^{-4} the radiometer noise. The quantization noise remains negligible (less than $5\,10^{-4}$) for a RMS noise level greater than 13 ADUs, and nominal input level is thus set around 20 ADUs. Total dynamic range is determined by the radiometer and computational noises, and by imperfect filtering of the out-of-band RFI component.

To reduce computational noise, signal is processed in each block (filter, FFT, total power detector, integrator) with full precision arithmetics and is rescaled only between blocks. Multiplications are performed with 18 bit arithmetics, and the signal is rescaled between each filter block and the corresponding FFT block in order to prevent overflows. Since multipliers have fixed size, and memory usage is modest, precision is kept constant through the FFT processor, leaving enough space at FFT input for signal growth. The overall gain of each PDFB for a monochromatic line and for white noise is $g_n = s\sum t_i$ and $g_l = s\sqrt{\sum t_i^2}$ respectively, where t_i are the FIR filter tap coefficients and s is the rescaling factor. Actual values for these parameters for the two PDFB are shown in Table 2.

Rescaling between filter and FFT introduces a small quantization noise and may reduce the insulation between the PDFB channels. This has been tested using numeric simulation, demonstrating that the extra quantization noise is always below 10^{-4}, and that additional insulation degradation is below -90 dB,

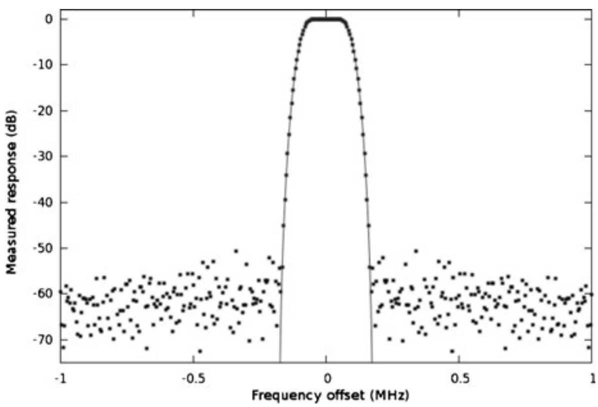

Fig. 5 *Points* measured PDFB2 channel response, up to the noise level. *Line* filter design response

Table 2 Signal level, in digital units, at the output of the main blocks, both for a white noise of typical RMS amplitude and for a monochromatic line at the maximum amplitude before FFT overflow

Stage	Rescaling factor s	Noise gain g_n	Noise RMS	Line gain g_l	Line amplit.
ADC	–	–	20	–	8
PDFB1 out	2^{-11}	90	1,800	290	1,500
PDFB2 out	2^{-21}	138	2,800	$1.4\ 10^4$	10^5
Total power out	2^{-15}	–	230	–	$4\ 10^5$

The rescaling factor is applied between PDFB filter and FFT blocks, and after total power detection

i.e. better than the filter stopband rejection, if the RMS level of the rescaled noise is kept above $\approx$ 50 units.

The signal is rescaled by 2^{-11} between the first PDFB filter and FFT blocks, resulting in a typical signal amplitude around 2,000 units, and by 2^{-21} between the second PDFB filter and FFT blocks. Output of the second polyphase filter bank is thus around 3000 units for white noise input (Table 2), leaving ample space for strong spectral features in the adopted 18 bit representation. The maximum monochromatic signal amplitude before FFT overflow occurs is around 8 ADUs.

Other 15 bits are discarded after total power computation. The integrator width is 36 bits, and the FFT cycle time is 8 μs, allowing an integration time of a few seconds even when strong monochromatic signals are present.

3.3 Laboratory tests

Spectrometer performance has been measured in laboratory using a signal composed of white noise and a monochromatic line. Difference spectra have been obtained subtracting spectra with and without the line. The current software does not allow for long integration times, resulting in a radiometer noise level of 50 to 60 dB below the line amplitude. An example spectrum is shown in Fig. 6. The spectrum is composed of eight regions acquired sequentially in two separate integrations and joined together, for a total of 3,840 spectral points (480 MHz).

The spectrum shows a line at −25 dBm (2 ADUs peak) on white noise at −17 dBm (3.5 ADUs RMS), with an integration time of 10 s. The power density in each spectral channel, normalized to the line, is −28 dB. The noise level is lower than its optimum level in order to allow detection of weaker signals in the relatively short integration time. No discontinuities are present anywhere in the reconstructed spectrum. No spurious line is present up to the noise level of −50 dBc.

If the line level is increased above the level at which FFT overflow occurs spectral degradation is limited at the PDFB1 channels containing the interfering

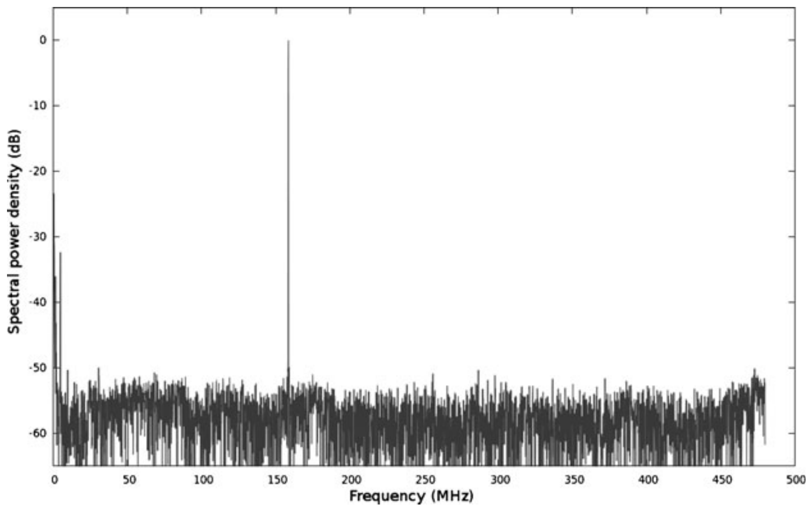

Fig. 6 Example spectrum. Signal is white Gaussian noise (N) plus a monochromatic tone (S), and the difference spectrum $(S + N) - (N)$ is shown. $S = -25$dBm, $N = -17$ dBm. *Horizontal scale* in MHz, *vertical scale* in dB, normalized to the line

signal. This has been tested using a line level of −5 dBm (20 ADUs). Apart from an evident distortion in the saturated portion of the spectrum, no other spurious images are present up to −65 dBc. In particular no line is visible at the aliased frequencies in the other PDFB1 channels. Dynamic rescaling of the PDFB1 outputs can be employed to completely avoid saturation even in this case.

4 Conclusions

The proposed design can be used to implement a wideband spectrometer, or a wideband F stage in a FX correlator, with excellent characteristics of spectral uniformity and channel-to-channel insulation. Resources usage is comparable to that of a single stage PDFB architecture, with increased flexibility. The two stage architecture allows to analyze just a portion of the input band, with corresponding reduced resource usage, and has an excellent dynamic range even when a spurious signal produces saturation in one of the first stage channels.

The design has been implemented and tested in the smallest configuration for the DBBC architecture, using a 1 GS/s ADC and a single CORE2 board. In this configuration the design has a total instantaneous bandwidth of 256 MHz and up to 4096 spectral points over the input band (50% time efficiency). Using two processing boards the whole bandwidth can be observed, with a spectral resolution of up to 8192 spectral points.

References

1. Comoretto, G., Tuccari, G.: Reference design for the Digital BBC Architecture. Arcetri internal report 2/2008 (2008). http://www.arcetri.astro.it/pubblicazioni/Reports/08/testi/2_2008.pdf
2. Harris, F.J.: Multirate Signal Processing for Communication Systems, p. 228. Prentice Hall (2008)
3. Tuccari, G.: DBBC—a Wide Band Digital Base Band Converter. In: IVS 2004 General Meeting Proceedings, p. 234 (2004). ftp://ivscc.gsfc.nasa.gov/pub/general-meeting/2004/pdf/tuccari3.pdf