DBBC3 – EVN and VGOS All-Inclusive VLBI System

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1 INAF-IRA, 2 MPIfR, 3 OSO

The Project

- Supported by EU Radionet3
- DIVA – Task2
- Partner:

  INAF – Italy

  MPIfR - Germany

  OSO – Sweden

DBBC3 Project is oriented to:

- **EVN wide-band VLBI backend**
- **VGOS ultra-wide-band VLBI system**

For EVN: DBBC3-L
General Performance

- Max number of RF/IF in one system: **8 (std. 2)**
- Instantaneous bandwidth ea. sampler: **4 GHz**
- Sampling representation: **10 bit**
- Processing capability: **max 24 TMACS** (multiplication-accumulation per second)
- Output: **VDIF 40GE packets, max 32/64Gbps**
- Compatibility with existing DBBC environment

DBBC3-L

- Stand-alone or back-end part of the full digital receiver implementation
- Includes broad-band samplers and/or input digital IF
- Basic Input: 4/8 GHz bwd in 0 – 16 GHz analogue range, in 4/2 pre-filtered Nyquist zones
- Output : full band or a selection DDC and PFB channels
- Output format: 10GE, 40GE, VDIF single and multi-thread
- Output data rate: 32 Gbps, today optimised for a ‘full compatible’ VGOS

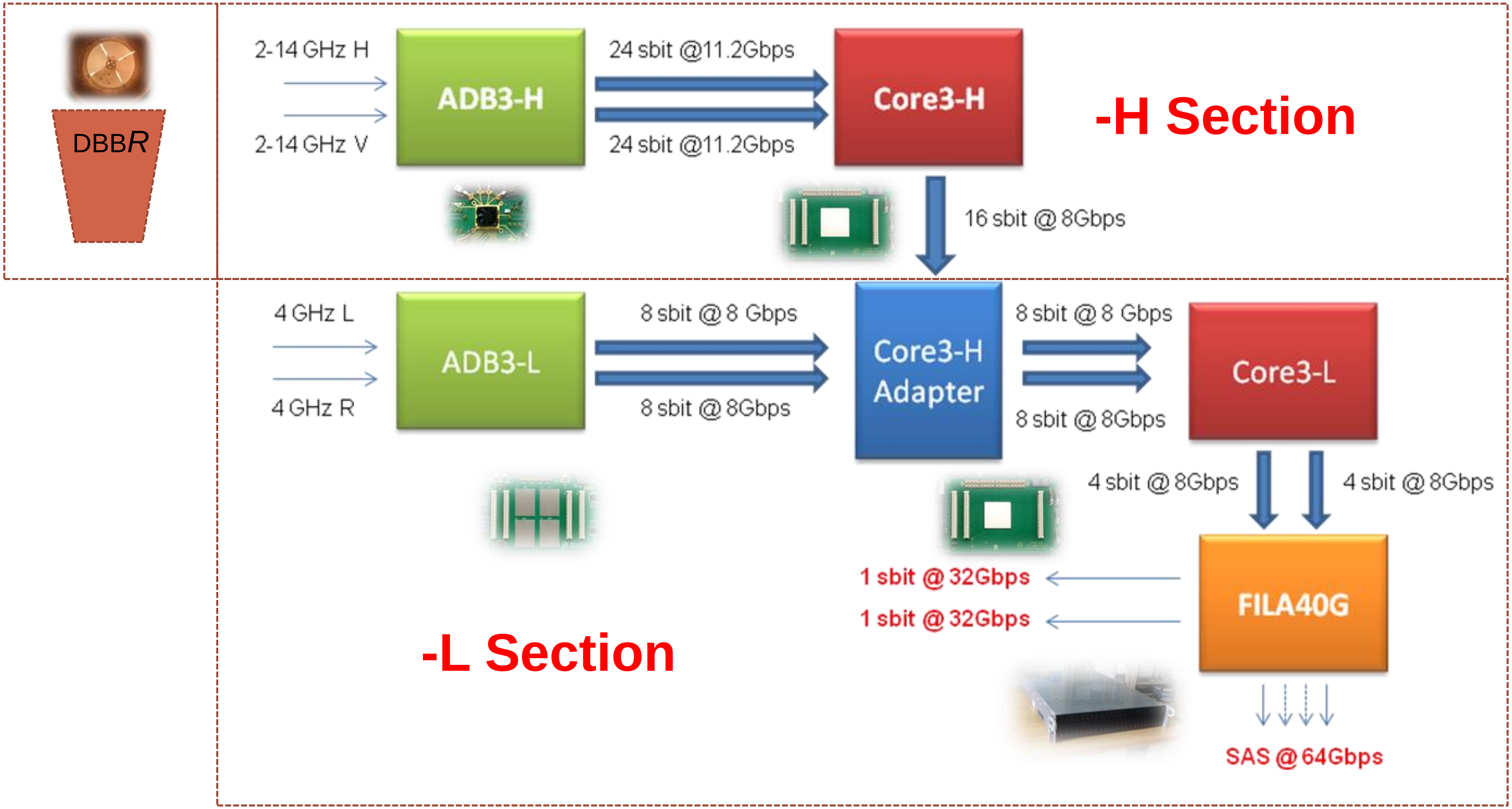
For VGOS: additionally DBBC3-H
General Performance

- Number of Input RF/IF per unit: **4**
- Instantaneous bandwidth ea. RF: **2-14 GHz**
- Sampling representation: **8 bit**
- Processing capability: **max 12 TMACS** (multiplication-accumulation per second)
- Output: **VDIF n x 10GE packets**
- Compatibility with existing DBBC environment

DBBC3-H

- Front-end part of the full digital receiver implementation
- Includes broad-band samplers and IF digital formation
- Basic Input: 1 – 16 GHz analogue, max 4 RF bands in a physical unit
- Basic Output: full band or a selection of 8 IF/band, 1 GHz bwd ea.
- Today optimized for VGOS range 2-14 GHz

DBBC3 Architecture Data Flow



THE CURRENT STATUS

DBB*R* Receiver
Horn

- Deeply modified from an original project for telecommunication
  and re-named as ‘quad ridge in resonant chamber ’
- Dual linear polarization, 1 LNA/pol
- Full range 1 – 16 GHz
- Radiation pattern vs frequency optimized for 3-14 GHz:
  40 - 20 degrees @ -3dB
- Antenna factor vs frequency optimized for 3-14 GHz:
  33 - 40 dB/m
- Optimized for cryogenic use (dewar shield is active part)
- Entirely in copper
- Custom cryogenic filters integration in the antenna body
- Complete performance still in definition, waiting for broadband LNAs

ADB3H - Sampler board

- Number of IFs: **1 - 4**
- Equivalent Sample Rate for full IF: **28/32 GSps**
- Instantaneous bandwidth: **14/16 GHz**
- Sampling representation: **8 bit**
- Real sampling
- Compatibility with existing DBBC environment
- Status: commercial samples today available only in large numbers for sharing production cost: additional funds required, additional projects required (SKA option)

CORE3H - Processing board

- Number of I/O: **max 54 serial links 12.5Gbps**
- Number of Output: **max 32 serial links 11.2Gbps**
- Input Sampling Representation: **8-10 bit**
- Processing capability: **max 3 TMACS**

  (multiplication-accumulation per second)
- Processing capability: **WB-DDC, WB-PFB, DCS**
- Output: **VDIF 10GE packets**
- Compatibility with existing DBBC environment
- Status: **Prototype ready**

GCoMo (GigaConditioningModule for –L version)

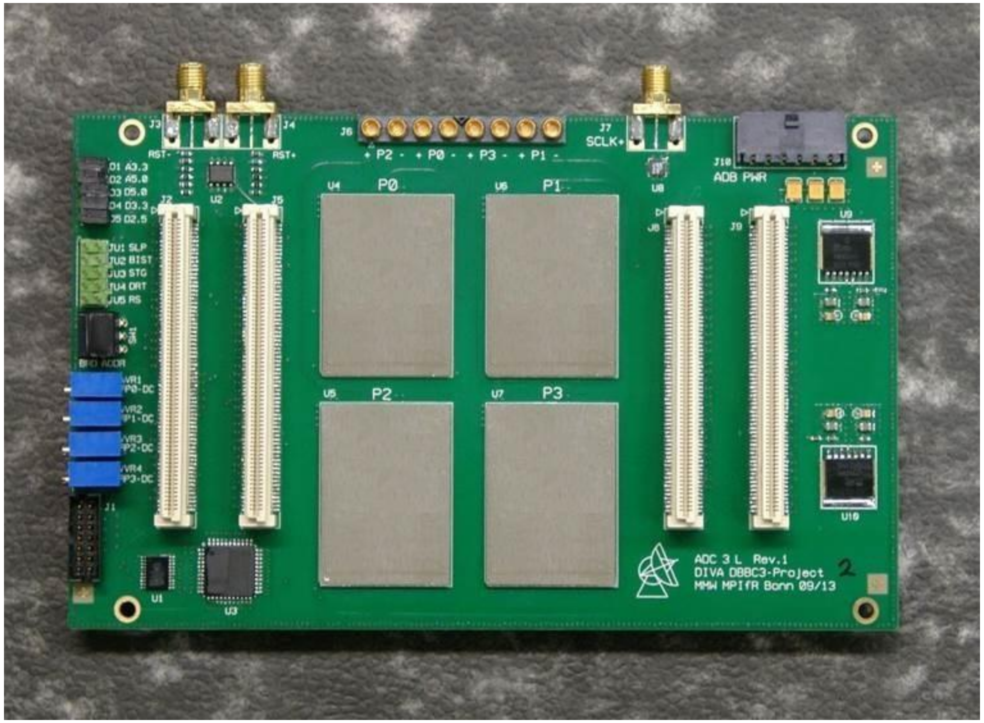
- Input: in real mode 4 pre-filtered 4GHz Nyquist bands
  in complex mode 2 pre-filtered 8GHz bands
- Total power detectors independent in all the Nyquist zones
- Modular construction: any zone can be included or not
- Power level control in agc and manual mode
- Compatibility with existing DBBC environment
- Status: **First units available**

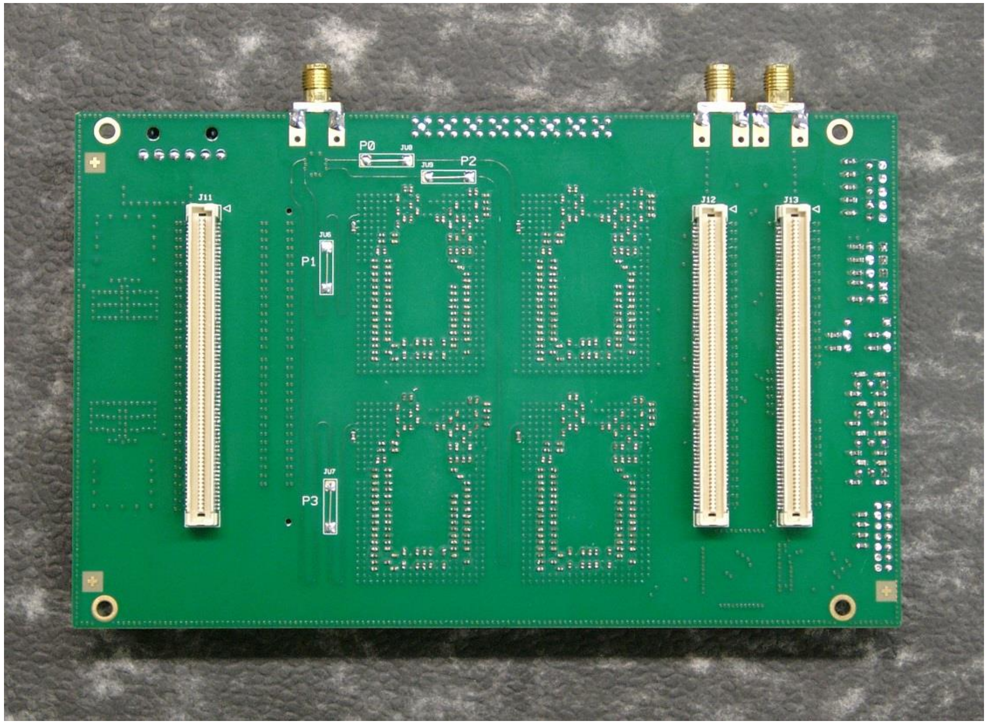
ADB3L - Sampler board

- Number of IFs: **1 - 4**
- Equivalent Sample Rate for full IF: **8 GSps**
- Instantaneous bandwidth: **4 GHz**
- Sampling representation: **10 bit**
- Real/Complex Sampling
- Compatibility with existing DBBC environment

Status ADB3L

Ready



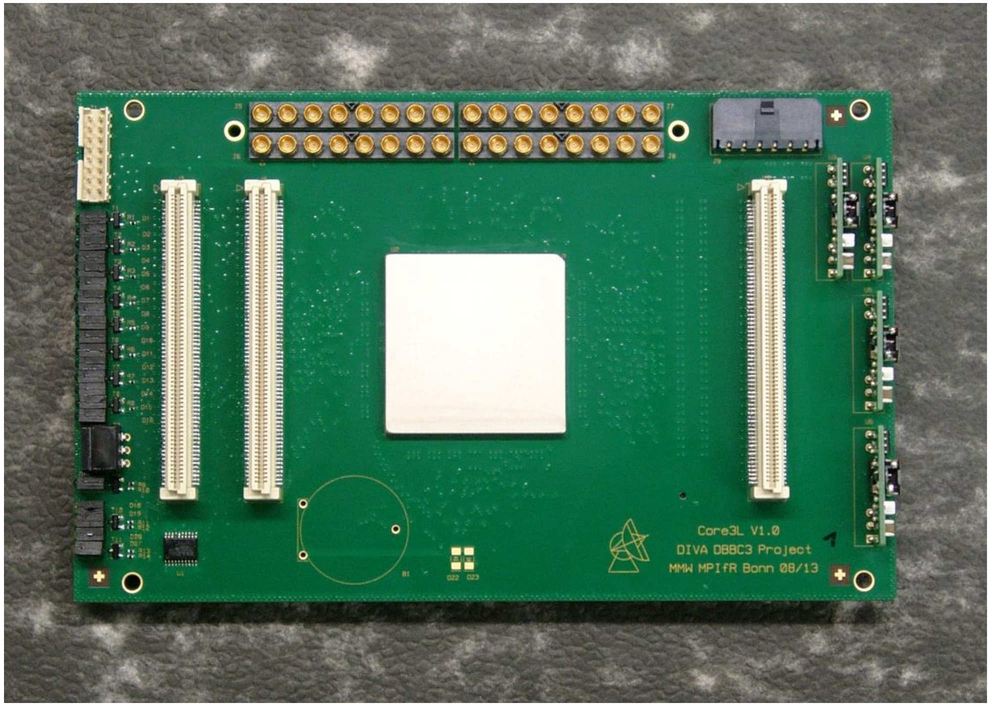


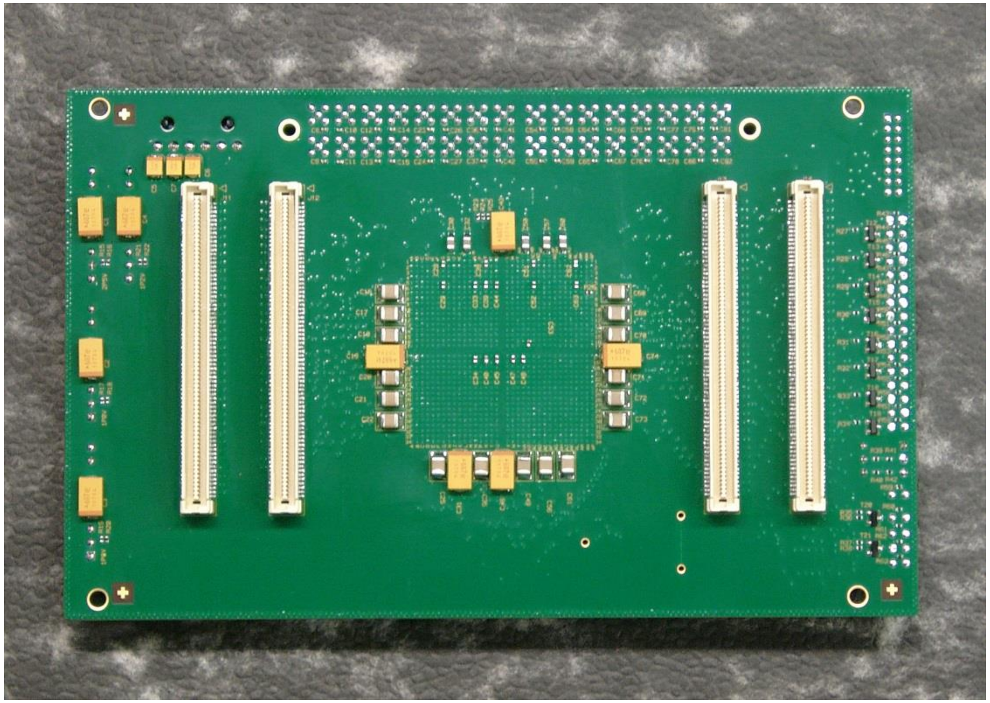
CORE3L - Processing board

- Number of I/O: **max 40 serial links 12.5Gbps**
- Number of Output: **max 32 serial links 11.2Gbps**
- Input Sampling Representation: **8-10 bit**
- Processing capability: **max 3 TMACS** (multiplication-accumulation per second)
- Processing capability: **WB-DDC, WB-PFB, DCS**
- Output: **VDIF 10GE packets**
- Compatibility with existing DBBC environment

Status CORE3L

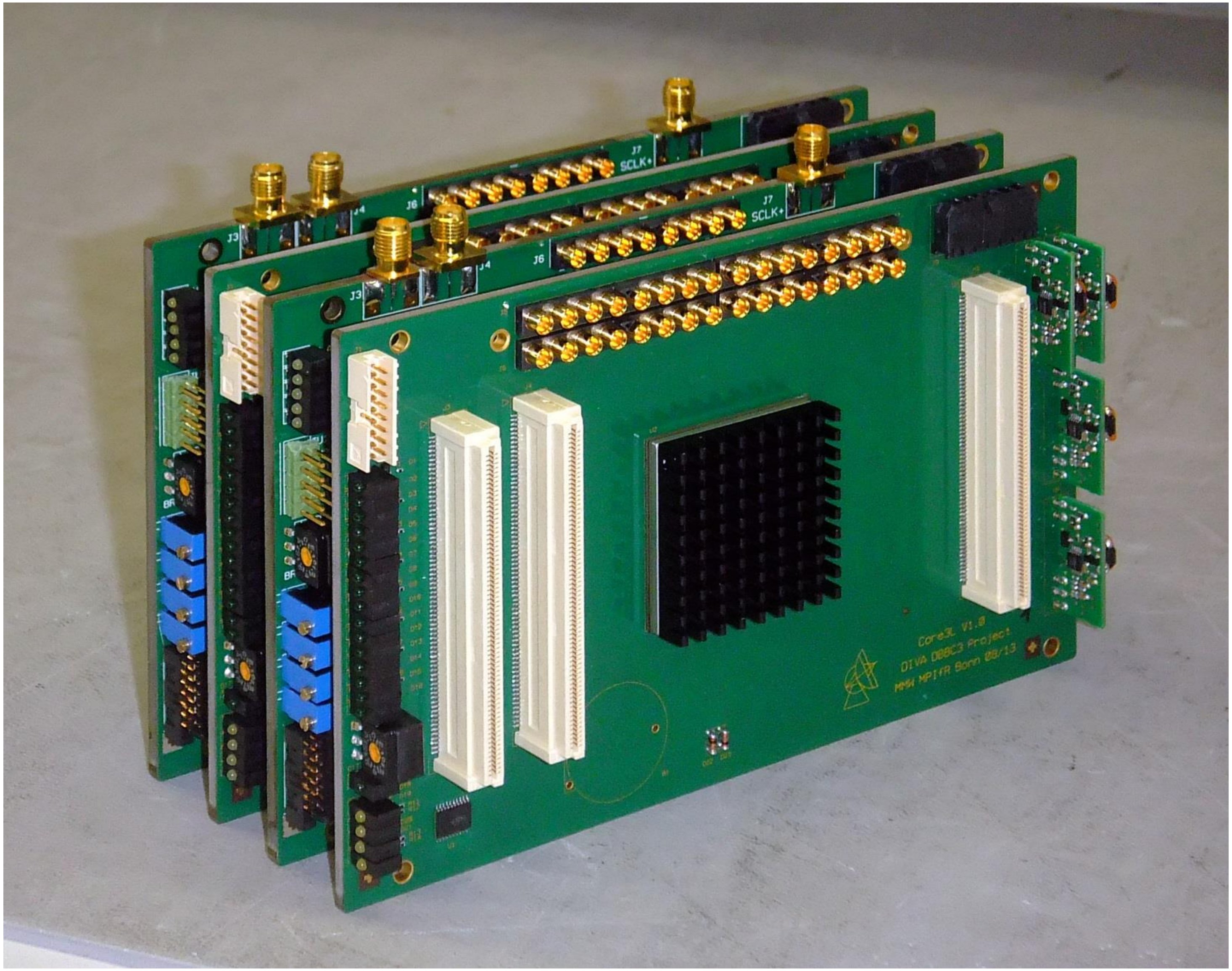
Ready





Stack with 2 ADB3L and 2 CORE3L

4 GHz bwd real dual pol / 8GHz bwd complex single pol



10GE Communication skills available

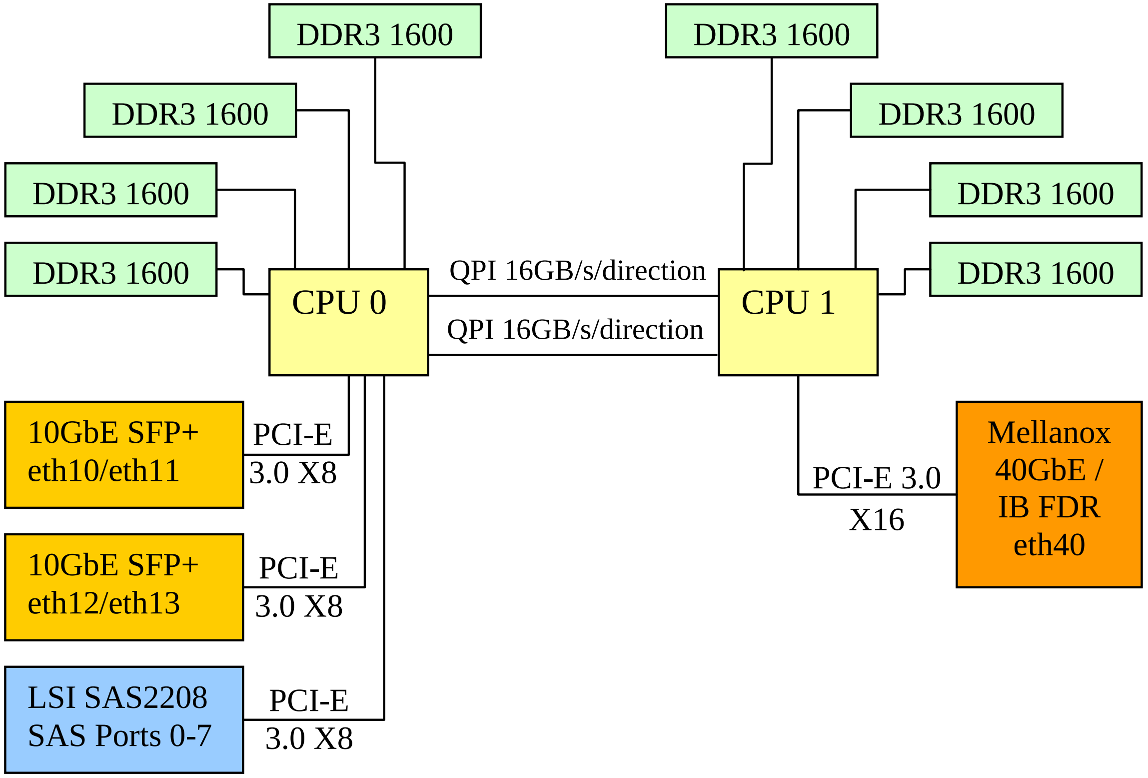
- MK5B up to 4 Gbps (native is 2Gbps)
- VDIF Single Thread up to 8Gbps
- VDIF Multiple Threads up to 8Gbps
- RAW (no headers) up to 8Gbps
- Threads can be fed by a selection of data channels eventually corner-turned
- The 10G Ethernet ports are independent in the destination address in VDIF-ST and MK5B
- The 10G Ethernet ports in multi-thread mode support an independent block of destination addresses coupled with the thread content selection
- Decimation and bit-mask are selectable at this level

FILA40G General Key features

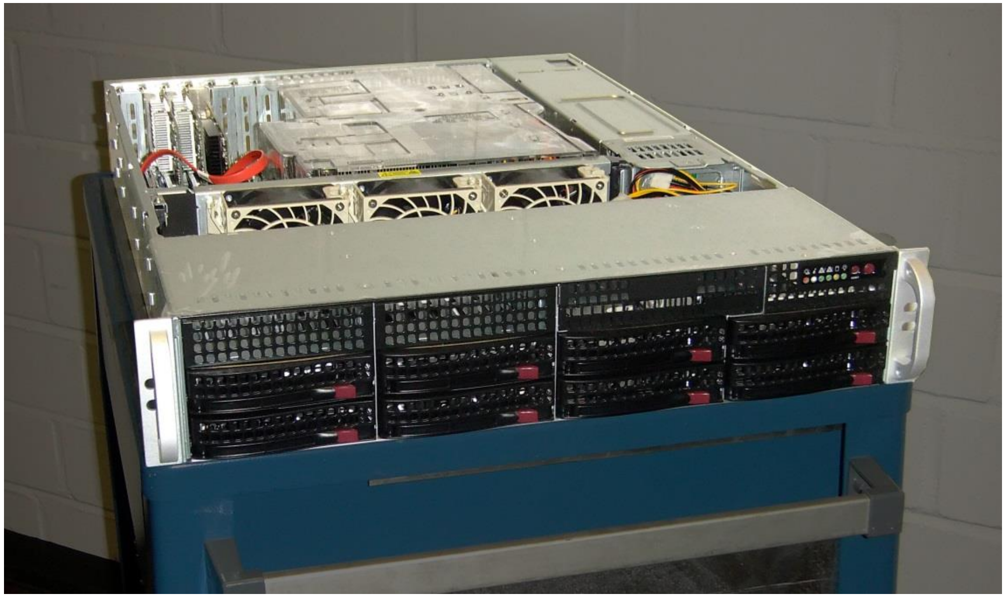
- 8 x 10GE Inputs
- 2 x 40GE Output
- Optional disk storage
  - Expected to record at 32Gbps sustained in half configuration mode
  - Compatibilty with Mark6 disk packs/chassis being investigated
- Stream aggregation
- Format conversion/VDIF threading
- Packet filtering
- Pulsar gating
- Timekeeping via NTP and/or GPS module
  - Propagates UTC to other connected devices via DBBC Local Network (DLN)

FILA40G Architecture for 32 Gbps

- 2 x Intel Xeon E5-2670
  - 8 core 2.60 GHz
- 8 x 8GB DDR3 1600
- 8 Onboard SAS2 ports
- 4 free PCI 3.0 x8 slots
  - To be used to add extra SAS2/3 ports



<u>Status FILA40G</u> 3 systems assembled + 40G Protocol Analyzer available (MPI)



THE FIRST OBSERVATIONS

First unit to be tested during 2014 in Noto including:

- DBB*R* receiver
  - dewar available
  - feed available (still to be validated in full)
  - LNA in order from LNF
  - lower chain available
  - Nyquist filters under development
  - superconducting cryo-filter in development to cut 2095 - 2185 MHz

- DBBC3-L in real mode with 4 bands 4 Nyquist zones / pol
  (0 - 4096, 4096 - 8192, 8192 -12288, 12288 - 16384 MHz)
  in complex mode with 2 bands 4 Nyquist zones / pol
  (0 - 8192, 8192 - 16384 MHz)
  - GCoMo available - to be replicated
  - ADB3-L available - to be replicated
  - CORE3-L available - to be replicated

- FILA40G
  - hardware available
  - disk space available - to be replicated

Additional DBBC3-L units planned for Effelsberg and Onsala

THANKS