DBBC3 - Full digital EVN and VLBI2010 Backend, Project Progress

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DBBC3 Project

- Project supported by EU Radionet3
- Partners:

  INAF – Italy

  MPIfR - Germany

  OSO – Sweden
- Starting date July 2012, duration 3 years

Twofold implementation

- Astronomic VLBI: 32Gbps EVN, mmVLBI
- Geodetic VLBI: VLBI2010

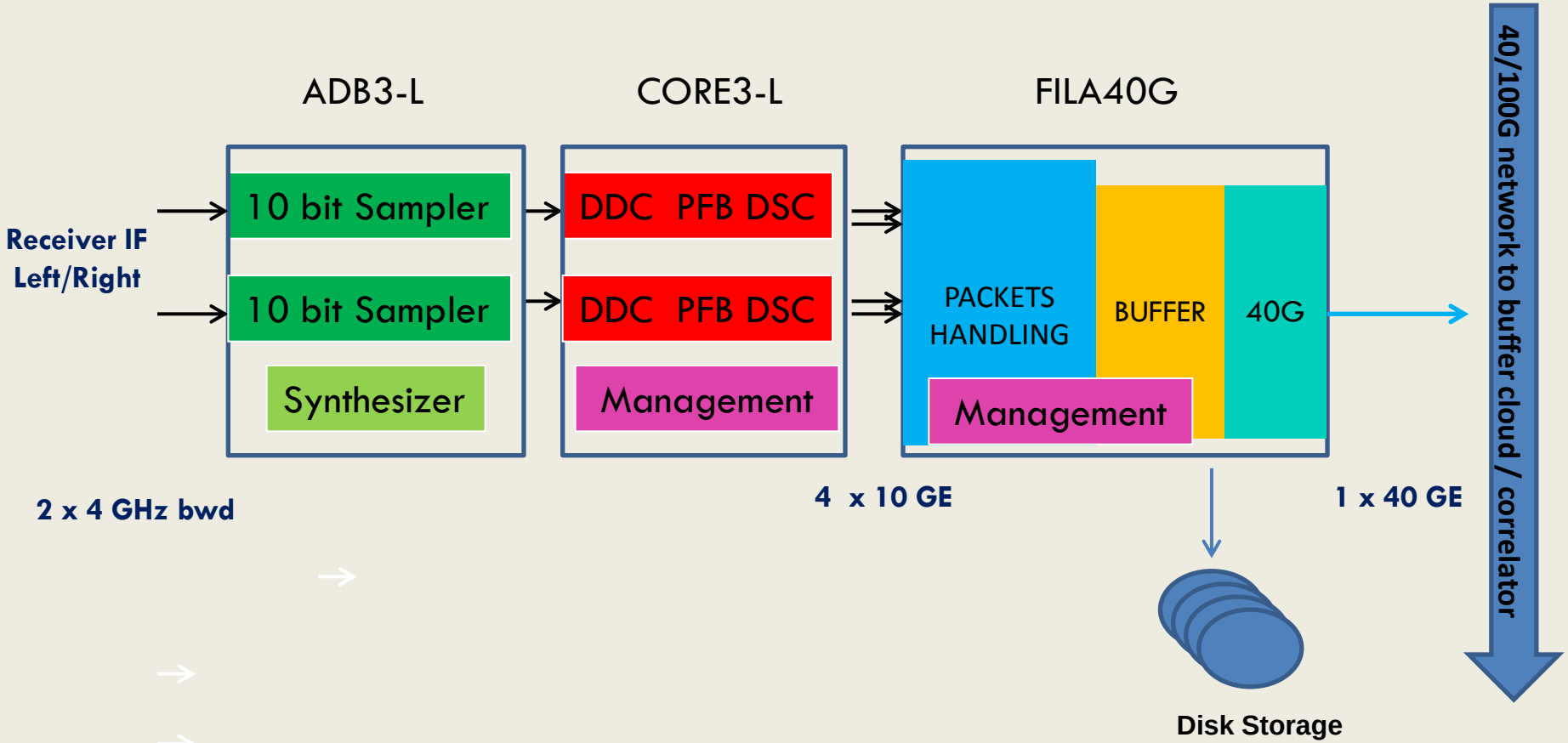
DBBC3 General Performance for EVN

- Number of Input IF: **1 - 4**
- Instantaneous bandwidth ea. RF: **>=4 GHz**
- Sampling representation: **10 bit**
- Processing capability: max **10 TMACS** (multiplication-accumulation per second)
- Output: **VDIF Ethernet packets, >=32Gbps**
- Compatibility with existing DBBC environment

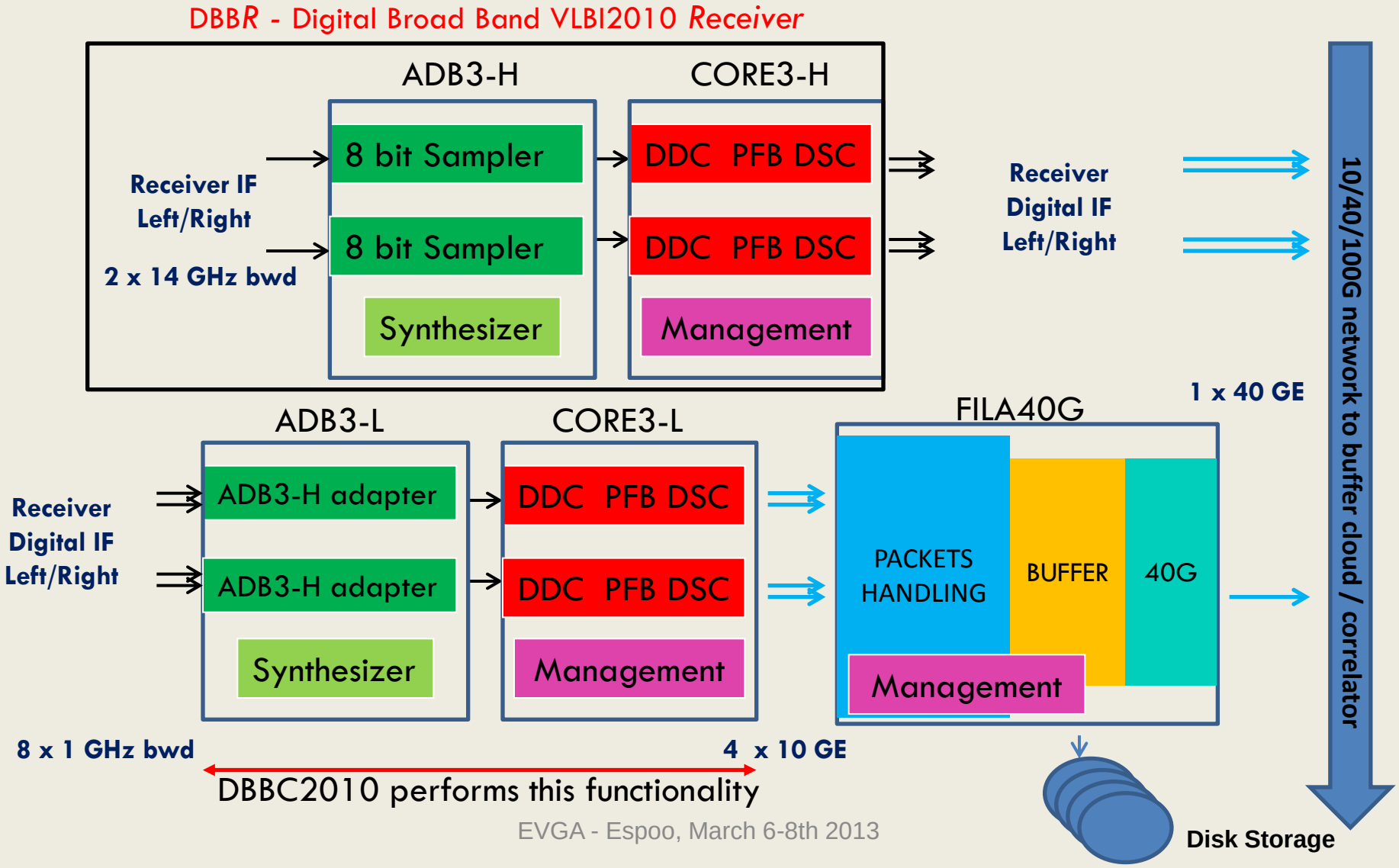
DBBC3 General Performance for VLBI2010

- Number of Input IF: **1 - 4**
- Instantaneous bandwidth ea. RF: =**14-16 GHz**
- Sampling representation: **8 bit**
- Processing capability: max **10 TMACS** (multiplication-accumulation per second)
- Output: **VDIF Ethernet packets, >=64Gbps**
- Compatibility with existing DBBC environment

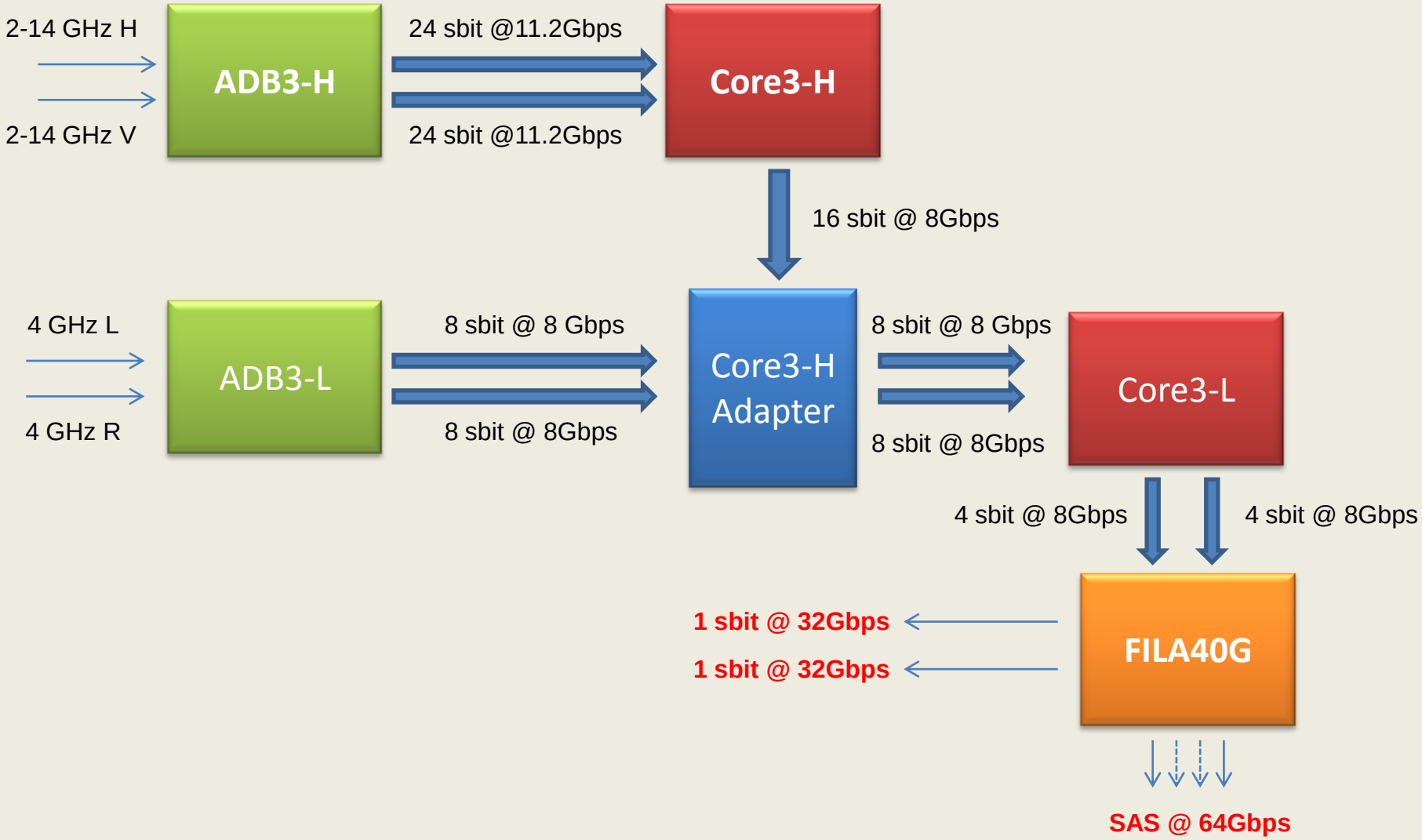
Typical DBBC3 Architecture for EVN



Typical DBBC3 Architecture for VLBI2010



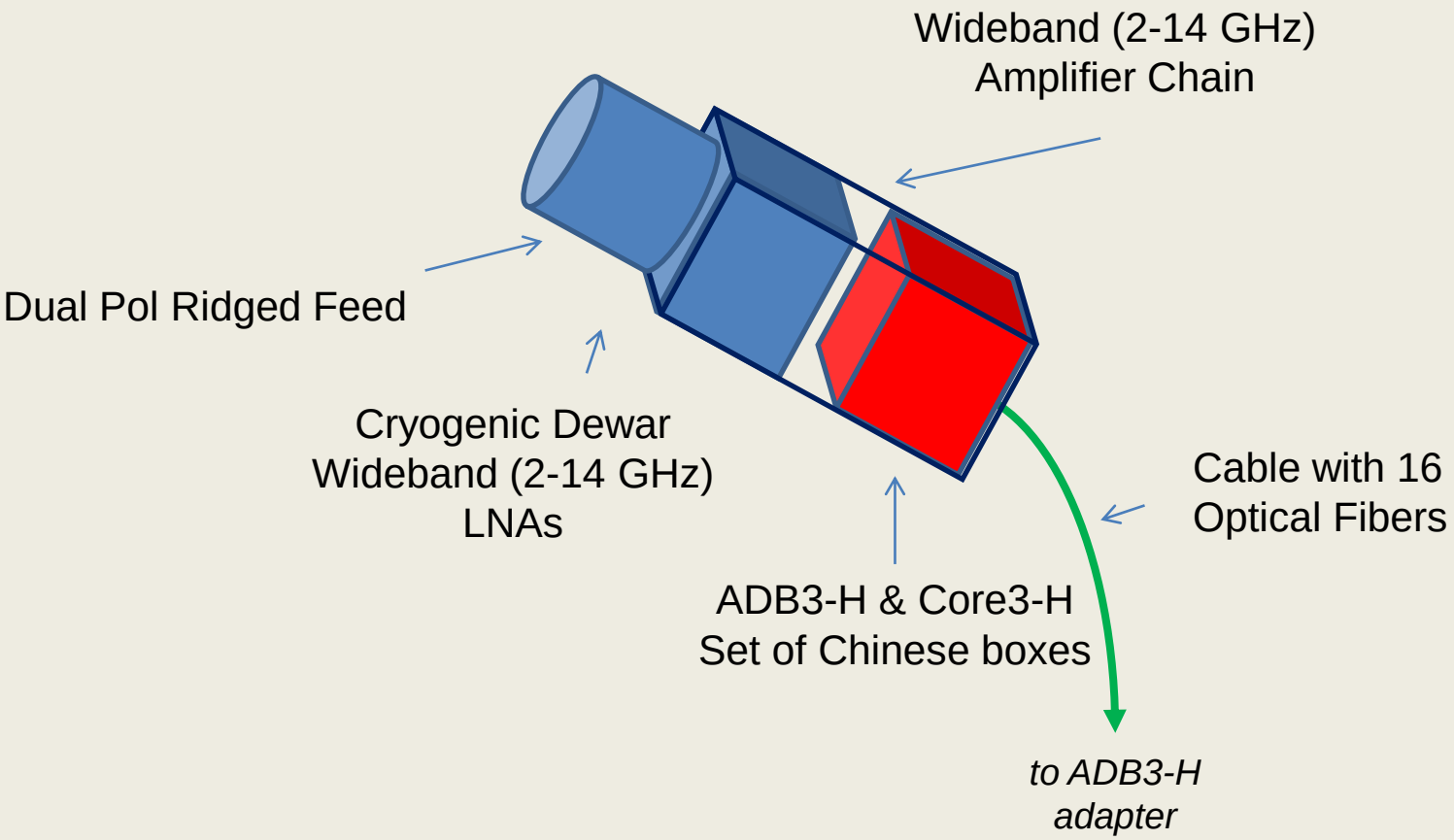
DBBC3 Architecture Data Flow



DBB*R* – Digital Broad Band *R*eceiver

- Fully digital receiver at sky frequency **(project complete)**
- Feed developed in Italy **(under validation)**
- Feed and LNA at cryogenic temperature **(dewar ready)**
- Sky frequency sampling
- Digital down conversion
- Output based on Digital Optical Link

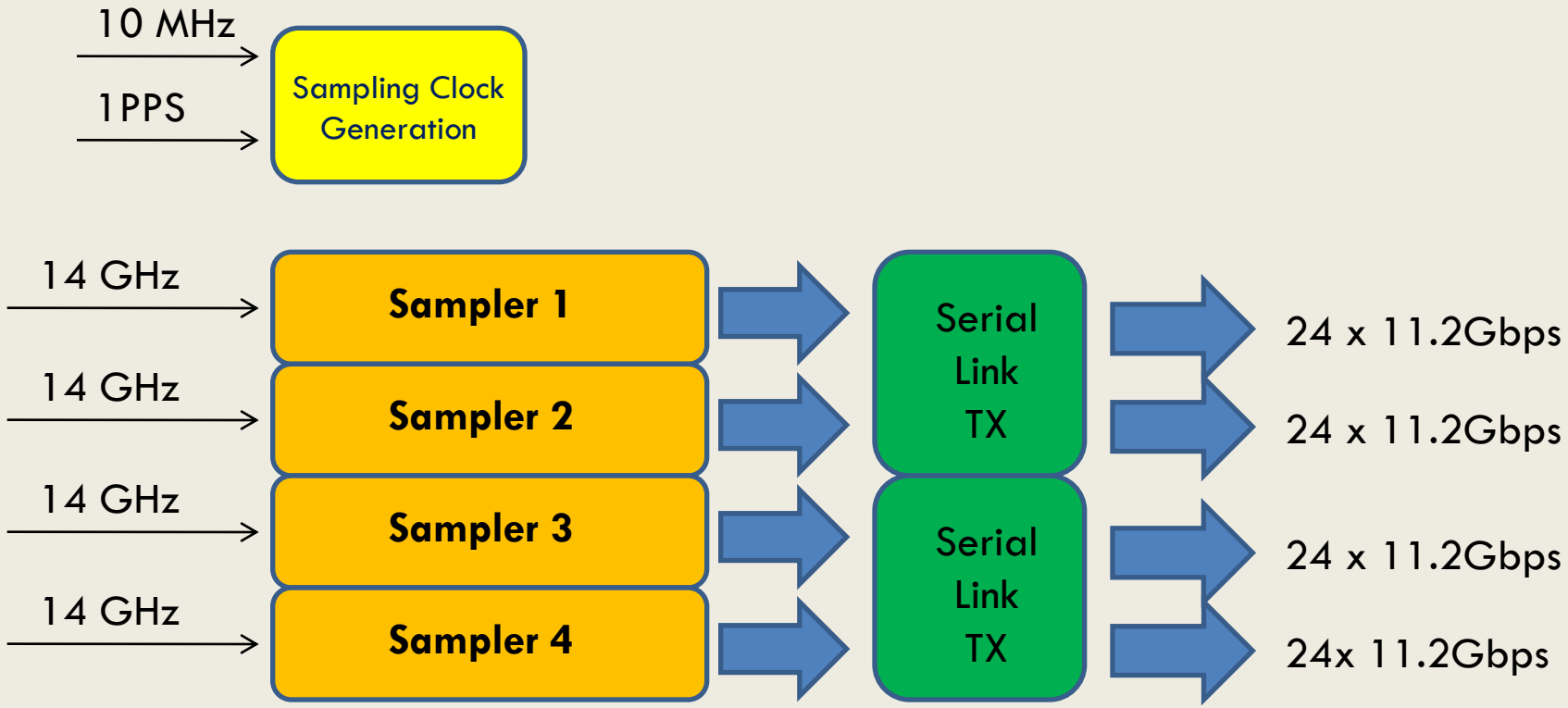
DBB*R*


Wideband (2-14 GHz)
Amplifier Chain
Dual Pol Ridged Feed
Cryogenic Dewar
Wideband (2-14 GHz)
LNAs
Cable with 16
Optical Fibers
ADB3-H & Core3-H
Set of Chinese boxes
to ADB3-H
adapter

ADB3-H General Performance

- **ADB3-H:**
  - Number of IFs: **4**
  - Equivalent Sample Rate ea. IF: **28.672 GSps**
  - Instantaneous bandwidth ea. IF: **14.336 GHz**
  - Sampling representation: **8 bit**
- Real Sampling
- Compatibility with existing DBBC environment
- **Engineers samples available, commercial devices expected in summer 2013**

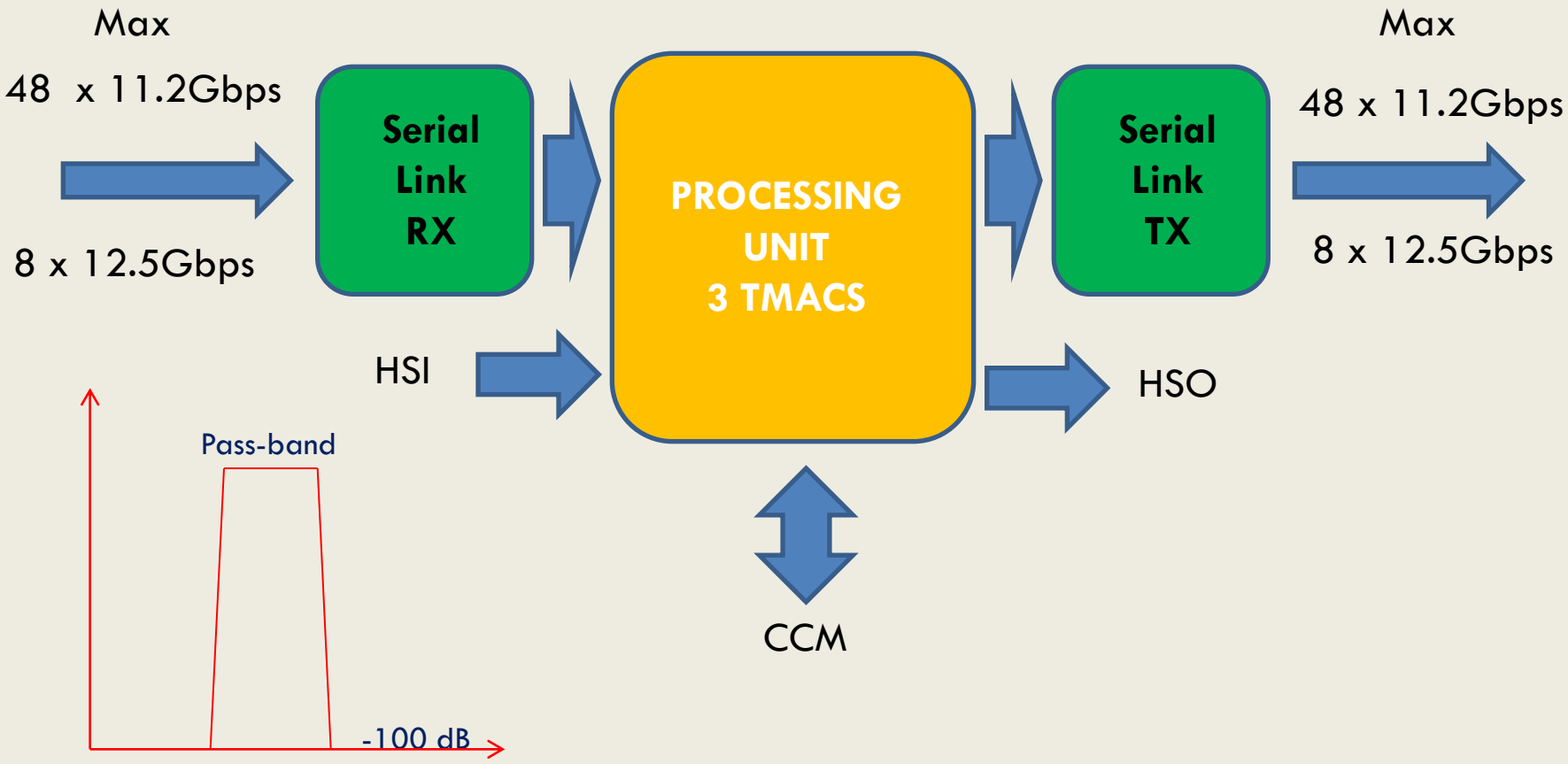
ADB3-H Sampler



CORE3-H General Performance

- **Core3-H**
- Number of Input: **max 48 serial links 11.2Gbps**
- Number of Output: **max 48 serial links 11.2Gbps**
- Input Sampling Representation: **8-10 bit**
- Processing capability: **max 5 TMACS** (multiplication-accumulation per second)
- Processing capability: **WB-DDC, WB-PFB, DCS**
- Output: **VDIF Ethernet packets, >=32Gbps**
- Compatibility with existing DBBC environment
- **DDC Firmware under development on prototype board (device identified)**

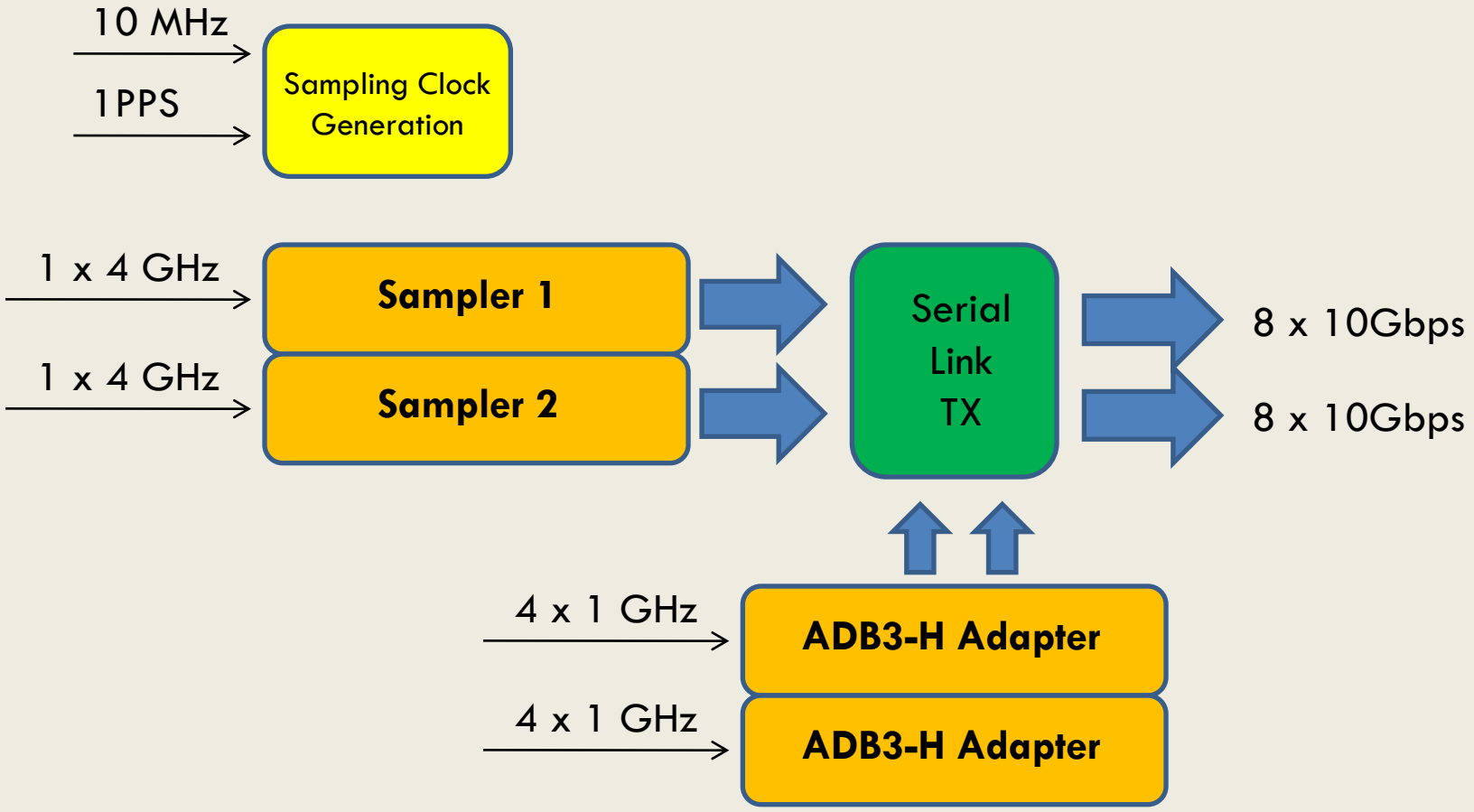
CORE3-H


Max
48 x 11.2Gbps
8 x 12.5Gbps
Serial Link RX
PROCESSING UNIT 3 TMACS
Serial Link TX
Max
48 x 11.2Gbps
8 x 12.5Gbps
HSI
HSO
CCM
Pass-band
-100 dB

ADB3-L General Performance

- **ADB3-L:**
  - Number of IFs: **2**
  - Equivalent Sample Rate ea. IF: **8 GSps**
  - Instantaneous bandwidth ea. IF: **4 GHz**
  - Sampling representation: **10 bit**
- Real/Complex Sampling
- Compatibility with existing DBBC environment
- **First prototype successfully tested, device identified, pcb project of the module ready**

ADB3-L Sampler

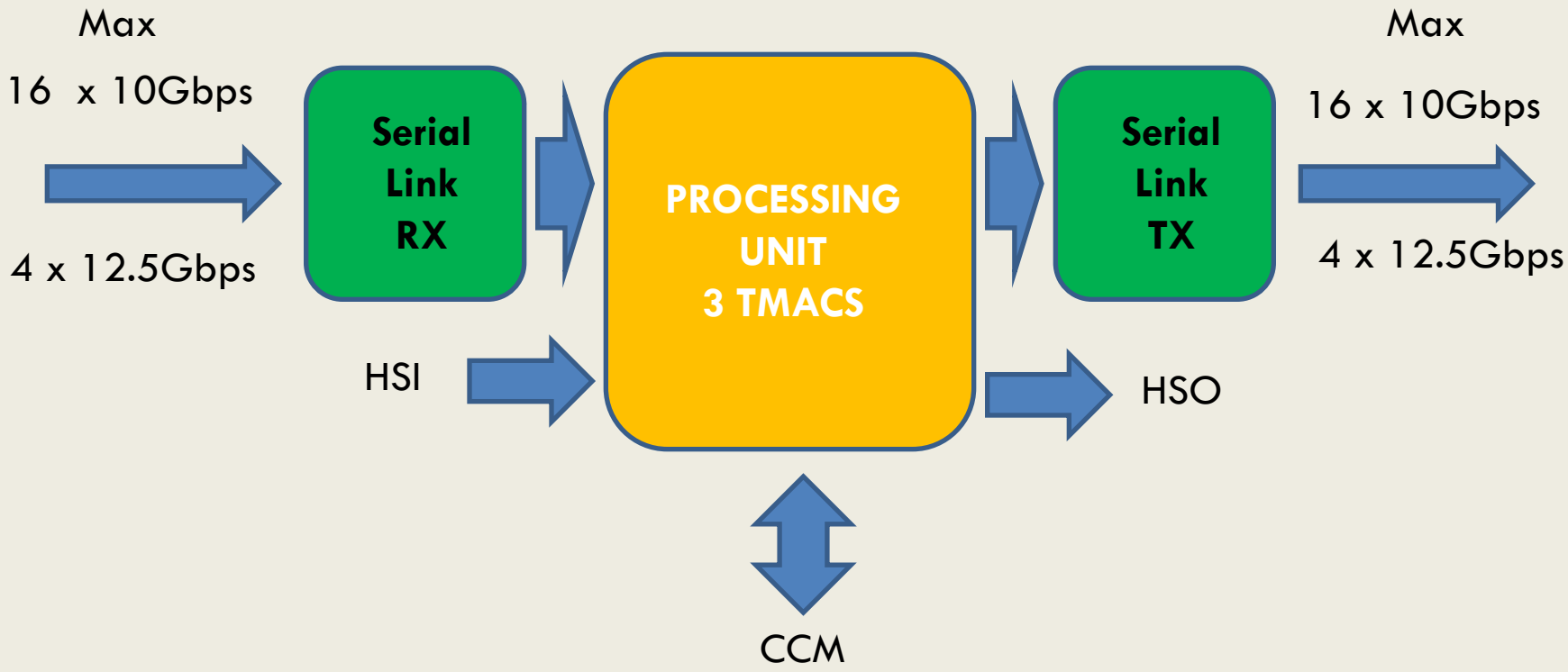


CORE3-L General Performance

- **Core3-L**
  - Number of Input: **max 16 serial links 10Gbps**
  - Number of Output: **max 16 serial links 10Gbps**
  - Input Sampling Representation: **8-10 bit**
  - Processing capability: **max 3 TMACS**
    (multiplication-accumulation per second)
  - Processing capability: **WB*-DDC, WB*-PFB, DCS**
  - Output: **VDIF Ethernet packets, >=32Gbps**
  - Compatibility with existing DBBC environment
- **Same device of Core3-H in reduced pin-out version**
- **DDC and PFB Firmware to be derived from the current DBBC2**

* Wide band

CORE3-L

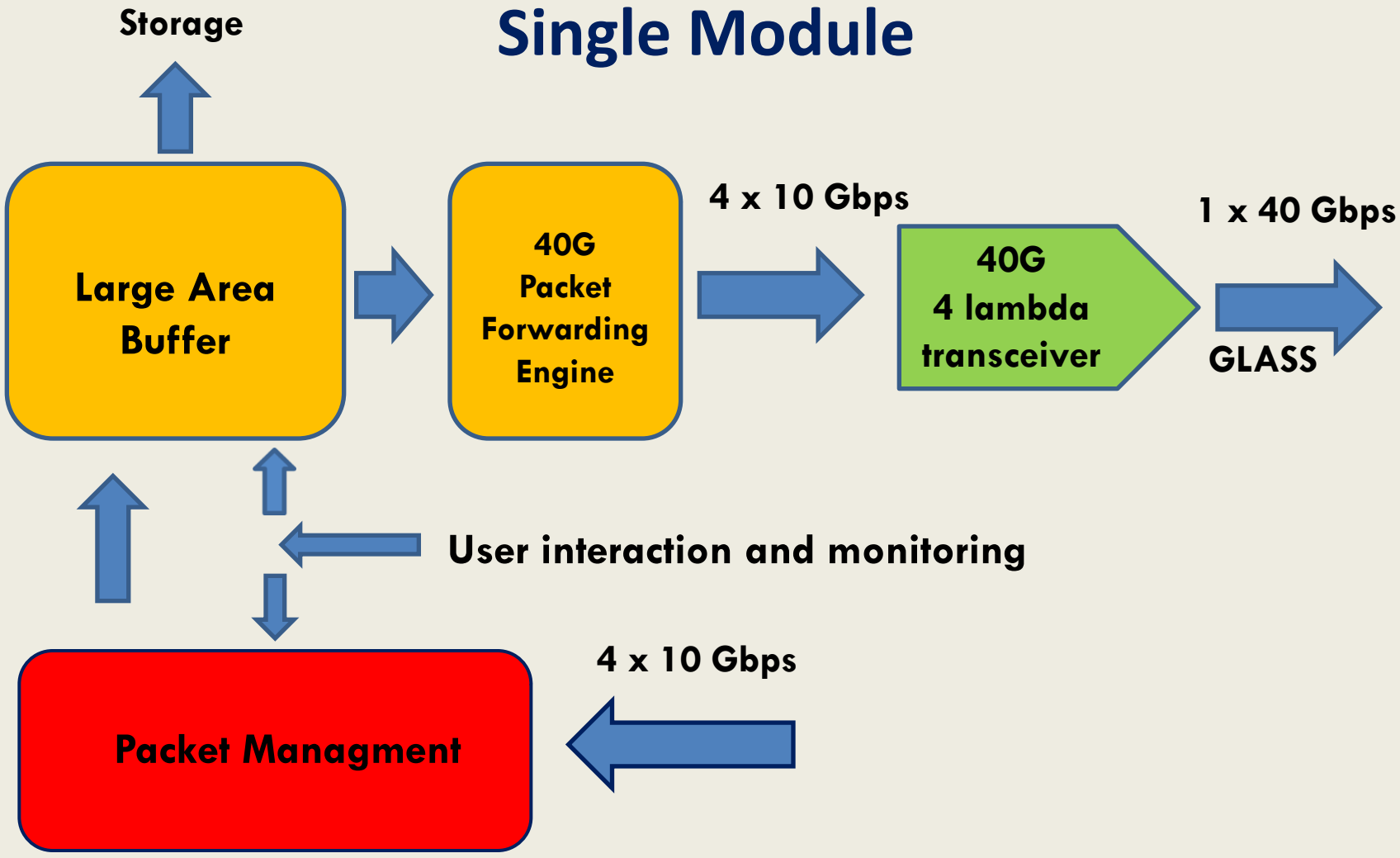

Max
16 x 10Gbps
4 x 12.5Gbps
Serial Link RX
PROCESSING UNIT 3 TMACS
Serial Link TX
Max
16 x 10Gbps
4 x 12.5Gbps
HSI
HSO
CCM

FILA40G Single Module General Performance

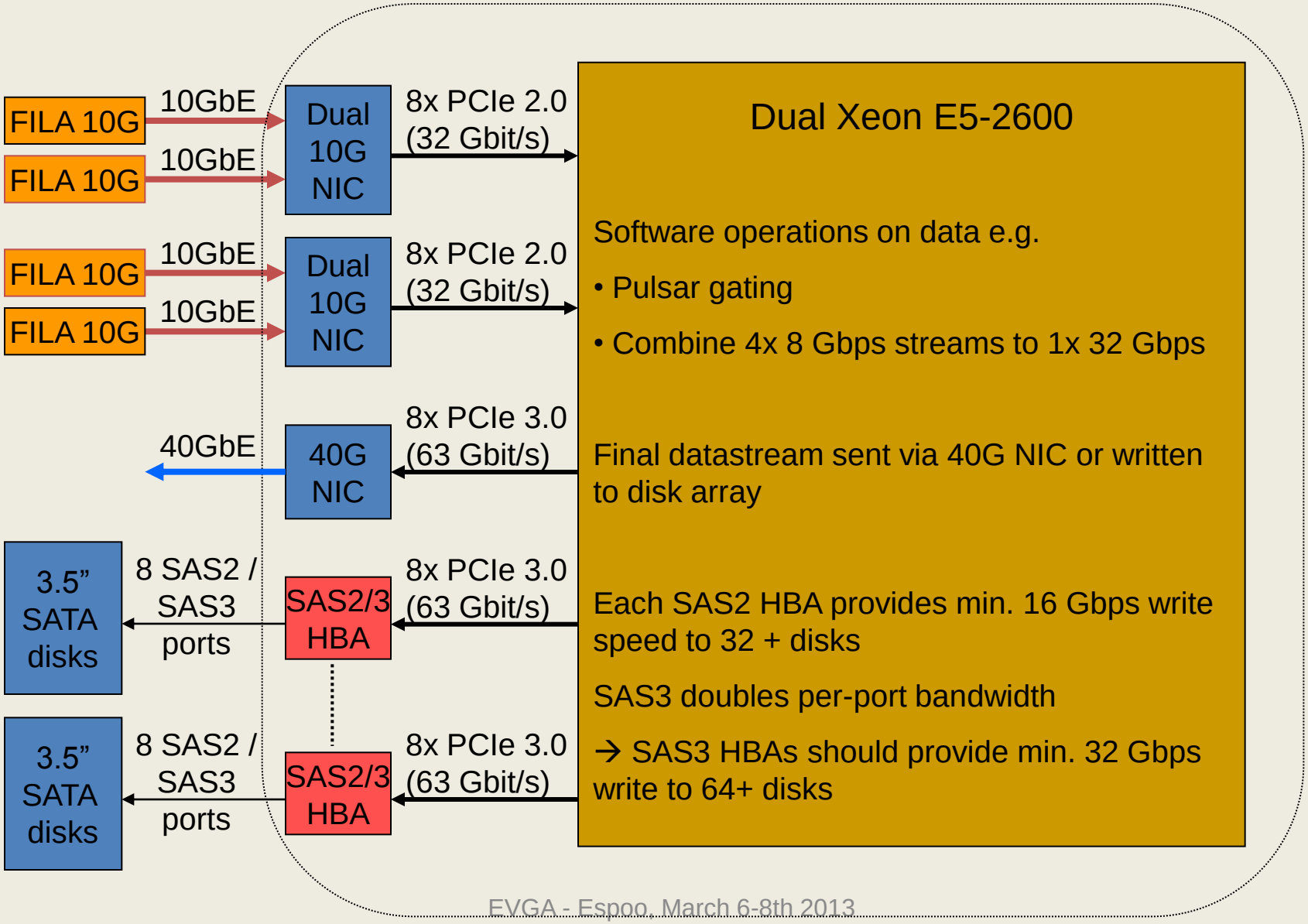
- Serial Link Input: = **4 x 10Gbps**
- Serial Link Output: = **1 x 40Gbps**
- Packets manipulating capability (filtering, pulsar gating, burst mode, etc.)
- Packets forwarding capability (different correlator nodes, different correlator sites, etc)
- Packets monitoring capability
- SAS ports for storage
- **Project under definition**

FILA40 Architecture

Single Module



FILA 40G Single Module



Questions?