DBBC2

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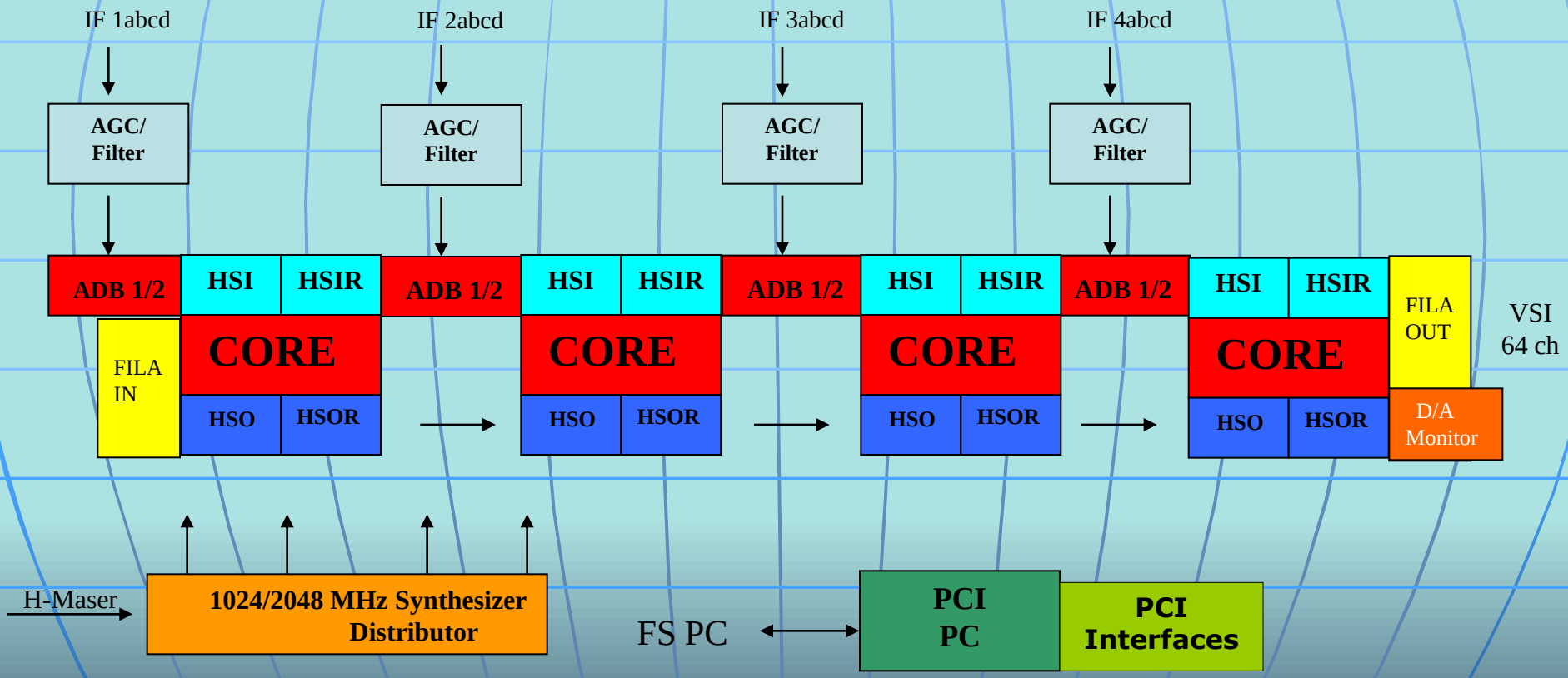
DBBC2 Architecture

IFn (MHz)
1~512, 512~1024,1024~1536, 1536~2048
or
1~1024, 1024~2048 MHz

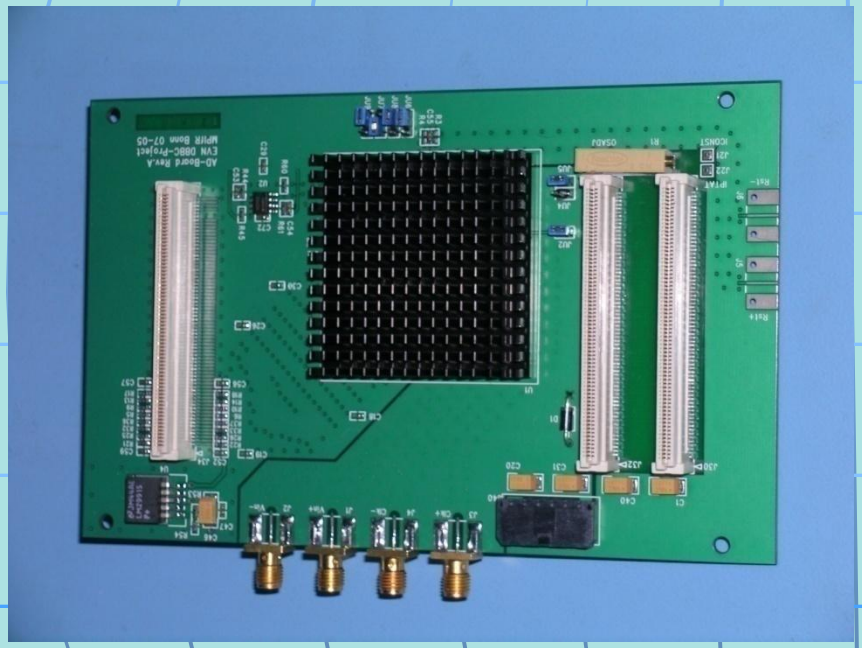


Review of the System Components

- Analog Conditioning Module
- Analog-Digital Converter (ADBoard1 - ADBoard2)
- Data Processing (CoreBoard2)
- Connection and Service (FiLaIN/OUT – FiLa10G)
- Timing and Clock (CaT1/2 – Clock and Timing Boards)
- Computer Control (PCSet)

ADBoard1

Analog to Digital Converter



Analog input: 0 - 2.2 GHz

Max Sampling clock single board: 1.5 GHz

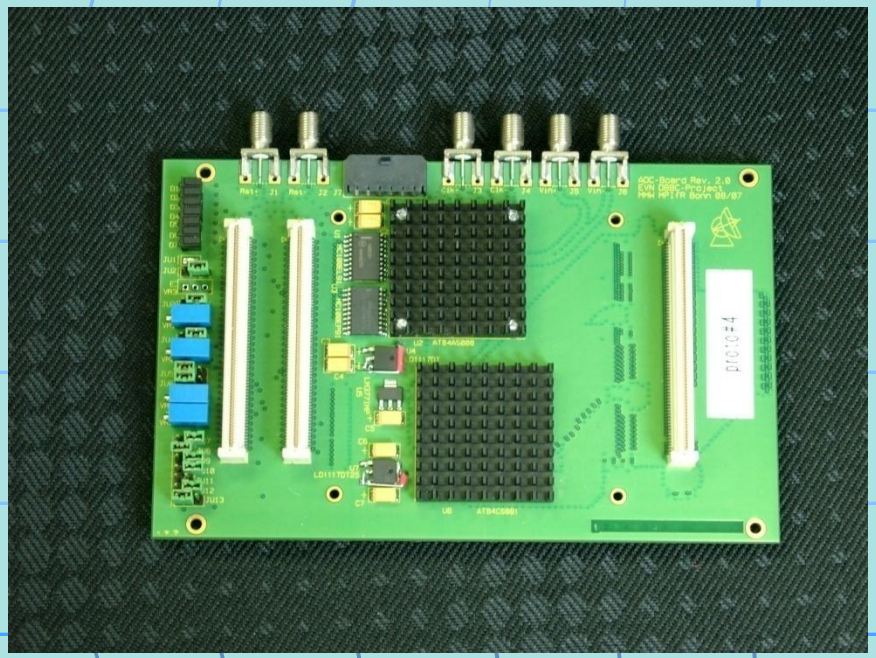
Max Istantaneous Bandwidth in Real Mode: 750 MHz

Max Istantaneous Bandwidth in Complex Mode: 1.5 GHz

Output Data: 2 x 8-bit @ ¼ SClk DDR

ADBoard2

Analog to Digital Converter



Analog input: 0 – 3.5 GHz

Max Sampling clock single board: 2.2 GHz

Max Istantaneous Bandwidth in Real Mode: 1.1 GHz

Max Istantaneous Bandwidth in Complex Mode: 2.2 GHz

Output Data: 2 x 8-bit @ ¼ SClk DDR
4 x 8-bit @ 1/8 SClk DDR

Piggy-back module support for 10-bit output and connection with FiLa10G board.

Core2

Basic processing unit

Input Rate:
(4 IFs x 2 bus x 8 bit x SClk/4 DDR) b/s
(2 IFs x 4 bus x 8 bit x SClk/8 DDR) b/s
More…

Typical Output Rate:
(64 ch x 32-64-128) Mb/s

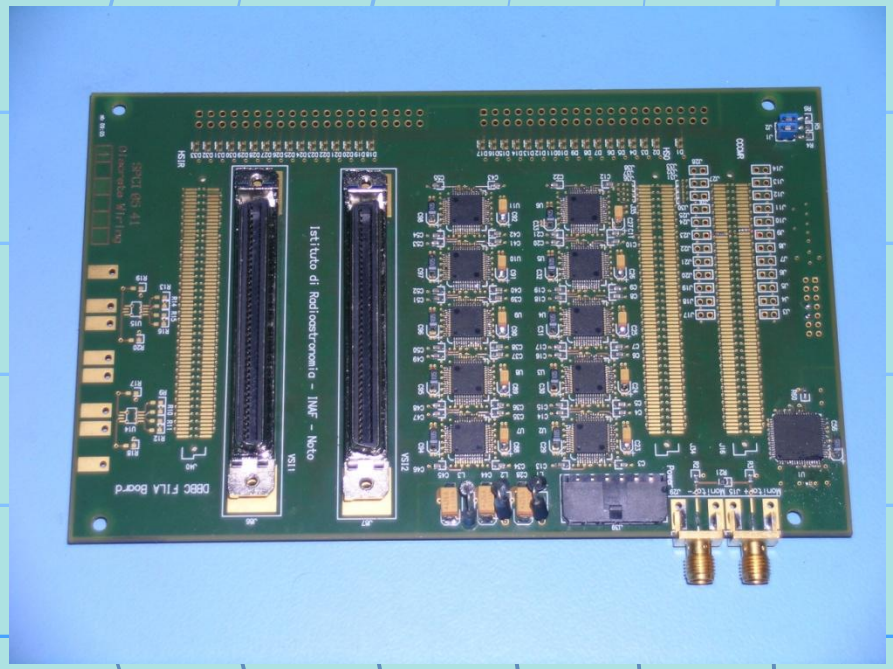
Programmable architecture

Es. Digital Down Converter:
1 CoreBoard2 = 4 BBC

Max Input/Output Data Rate 32.768 Gbps

FiLa Board

Connection and Service



First and Last board in the stack

First:
- Communication Interface
- JTAG Programming Channel
- 1PPS Input

Last:
- 2 VSI Interfaces
- DA Converter

1PPS Monitor Out

80Hz Continuous Cal Out

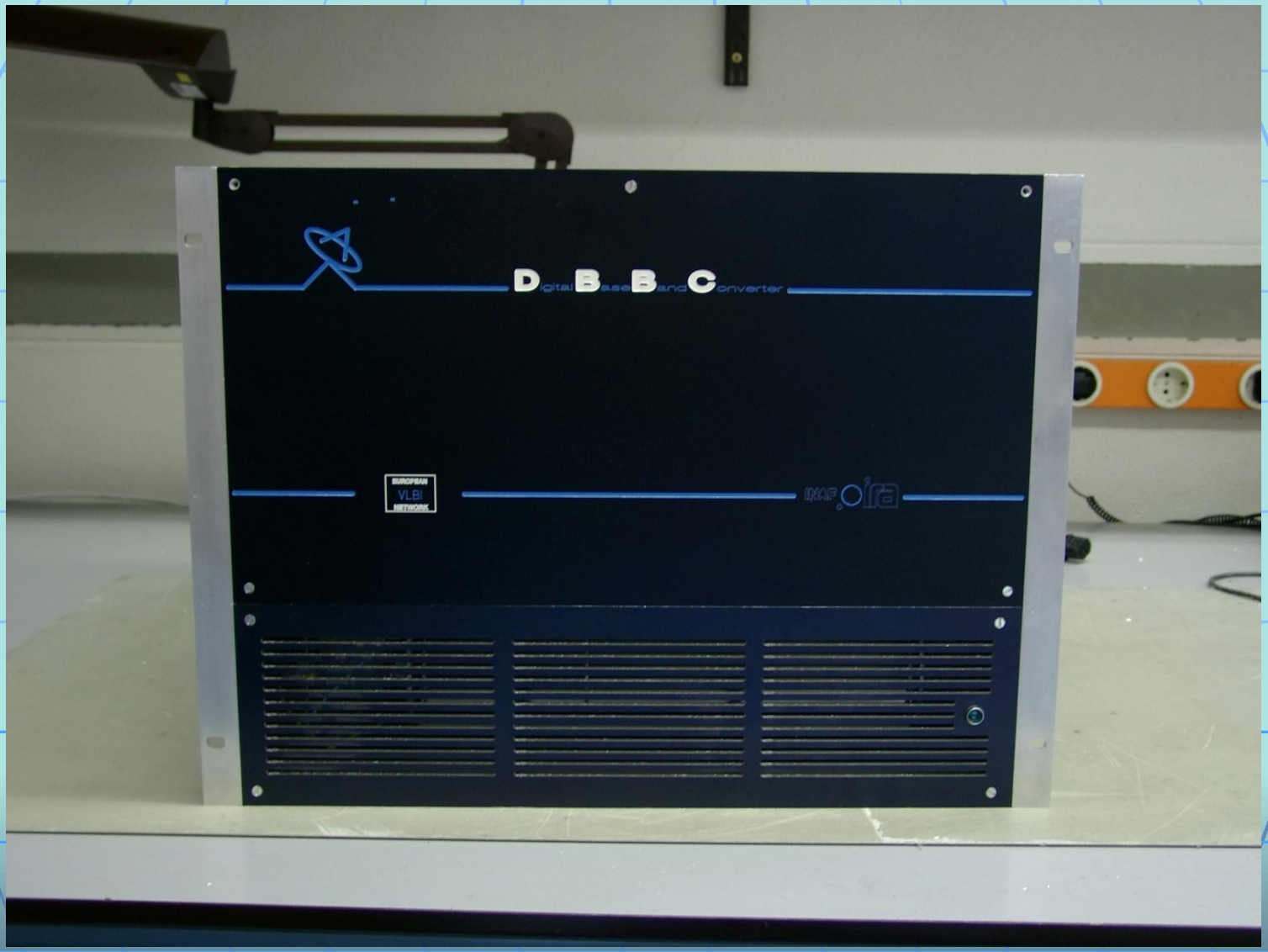
PCSet

FPGA device configuration through USB – JTAG interface

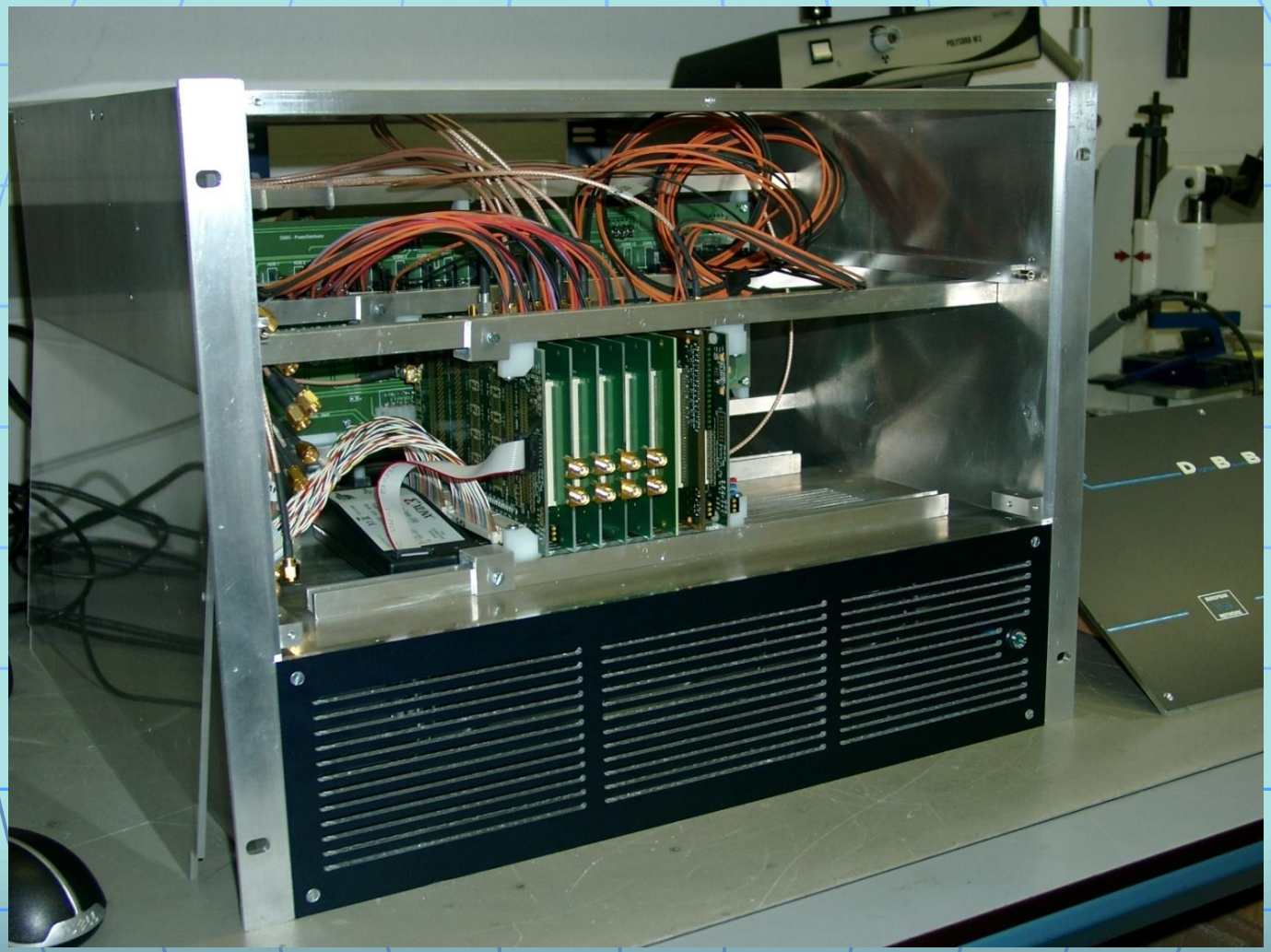
Communication with 32-bit bus for CoreBoards register setting,
total power measurement,
statistics of the state,
single channel automatic gain control, etc.

Communication with Conditioning Modules for IF total power measure, automatic gain control, registers control

Field System interface through a network connection


DBBC
Digital Base Band Converter
EUROPEAN
VLBI
NETWORK
IRAM
ira

TOW May 2011




10 MHz In
10 MHz out
1 PPS In
1 PPS out
Analog Mon.
1 PPS Mon.
SYS LL OUT
RF 4
RF 3
RF 2
RF 1
Main Power
FRAGILE

TOW May 2011

Different Functionalities Available

- Digital Down Converter (DDC)
- Polyphase Filter Bandpass converter(PFB)
- Spectrometers

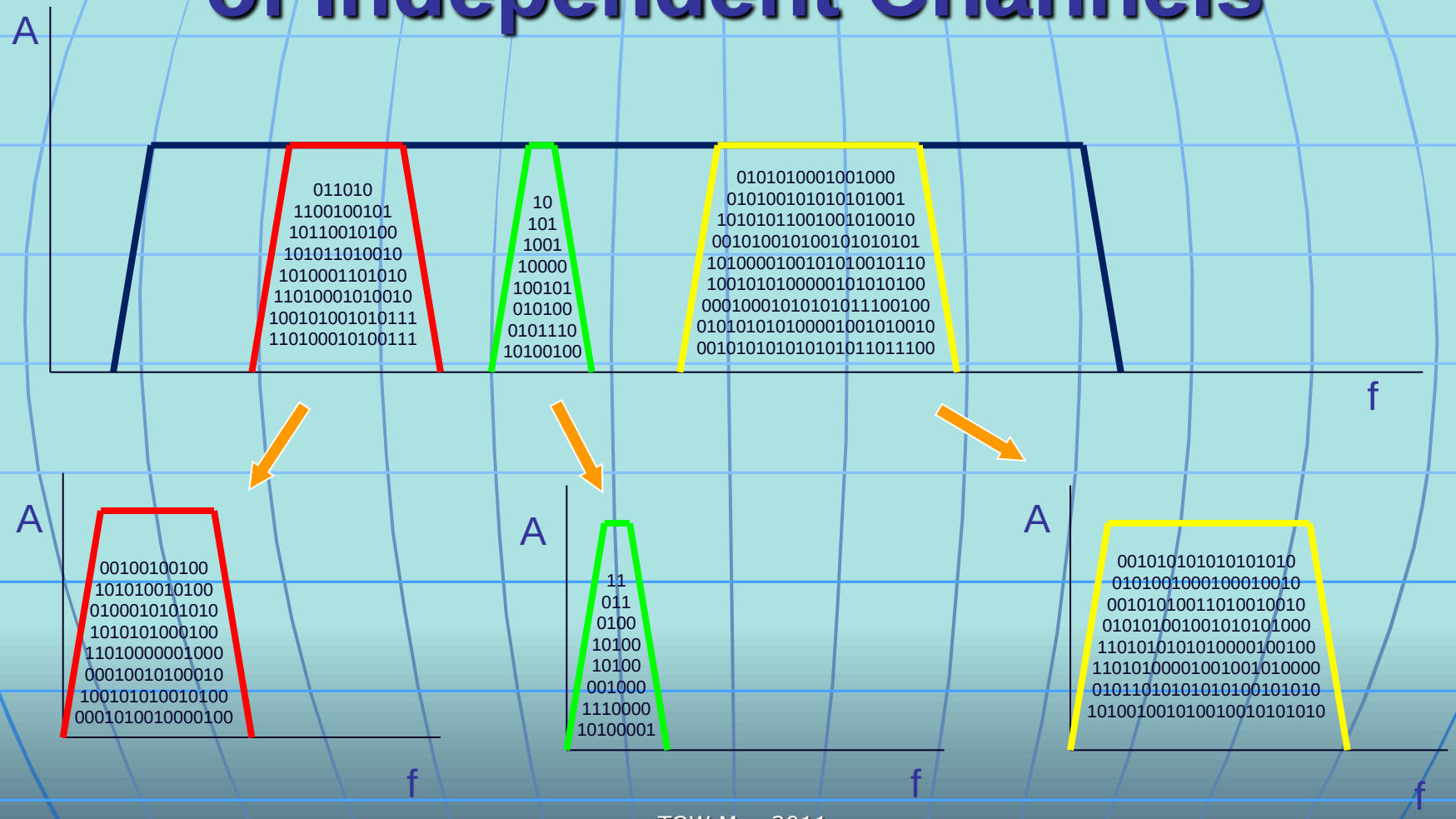
General Features

- 4 RF/IF Input from 16 (4x4) in a range up to 2.2 (3.5) GHz
- Four polarizations or bands available for a single group of 64 output data channel selection (2 VSI output connectors with 1 or 2 Gb/s each)
- Output from the stack to FiLa10G ethernet card as 4x2Gbps
- 1024/2048 MHz sampling clock frequency
- DDC: tunable, channel bandwidth between 1 MHz and 16 MHz, U&L, Continuous cal with 80 Hz synchronization, mode 'astro', 'geo', w-astro',' test'

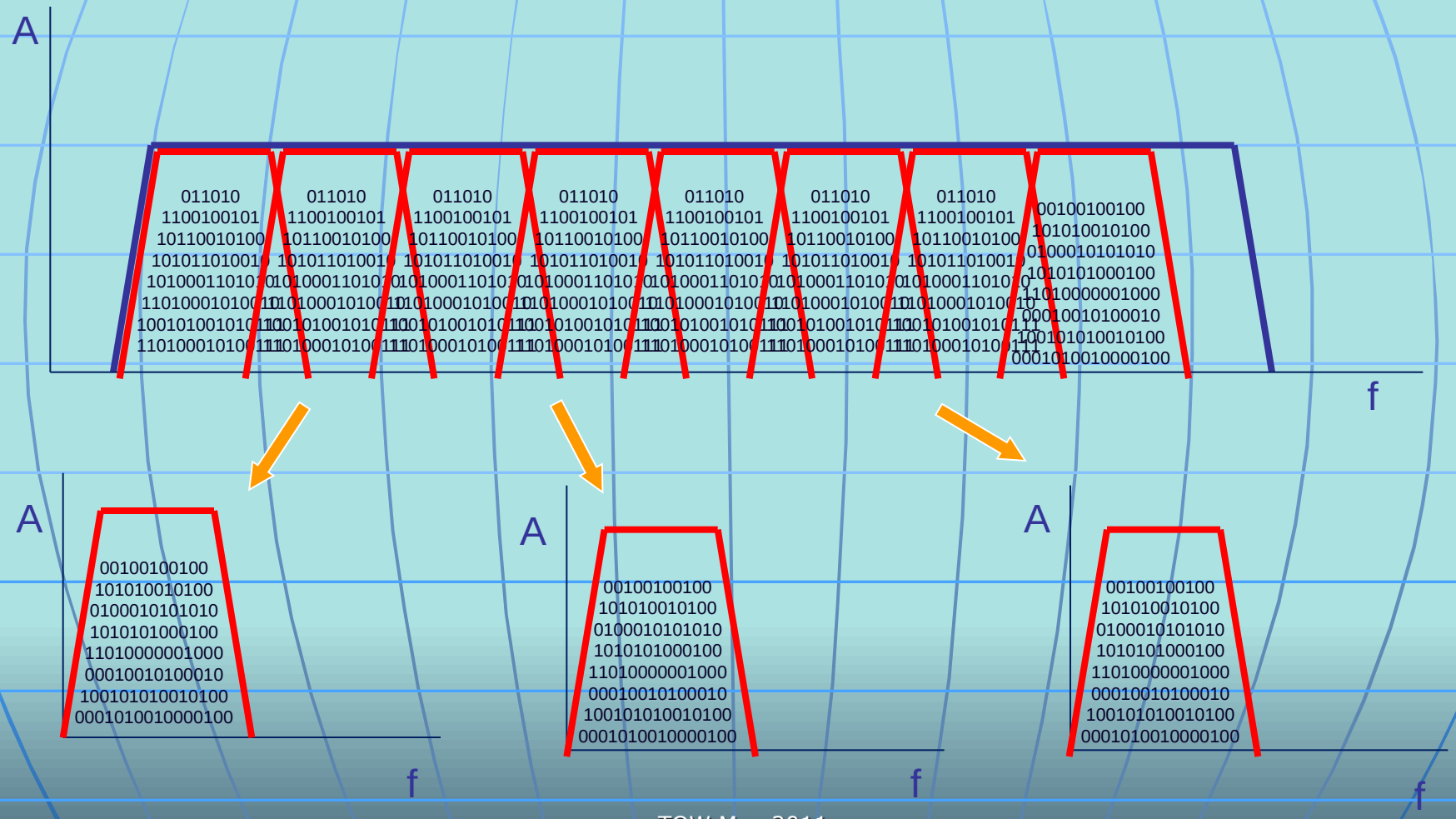
(on VSI binary counter pattern, next revision added MK5 TVG injection)

- PFB: fixed tuning, channel bandwidth 32 MHz, all U or L depending on the Nyquist zone, (next revision VSI test mode injection)
- Additional Instrumentation (spectrometers)

Digital Down Conversion to Base Band of Independent Channels



PFB
Conversion to Base Band



FiLa10G

10G Optical Fiber Ethernet Board

- Triangle connection between HSI (DBBC fast sampled data bus) – VSI – 10Gb link
- It can be placed either at the beginning of the chain or at the end -→ MK5C
- Piggy-back board for ADB2

Connection examples

- 2 x VSI --> MK5C

- 2 x VSI --> MK5C & MK5B

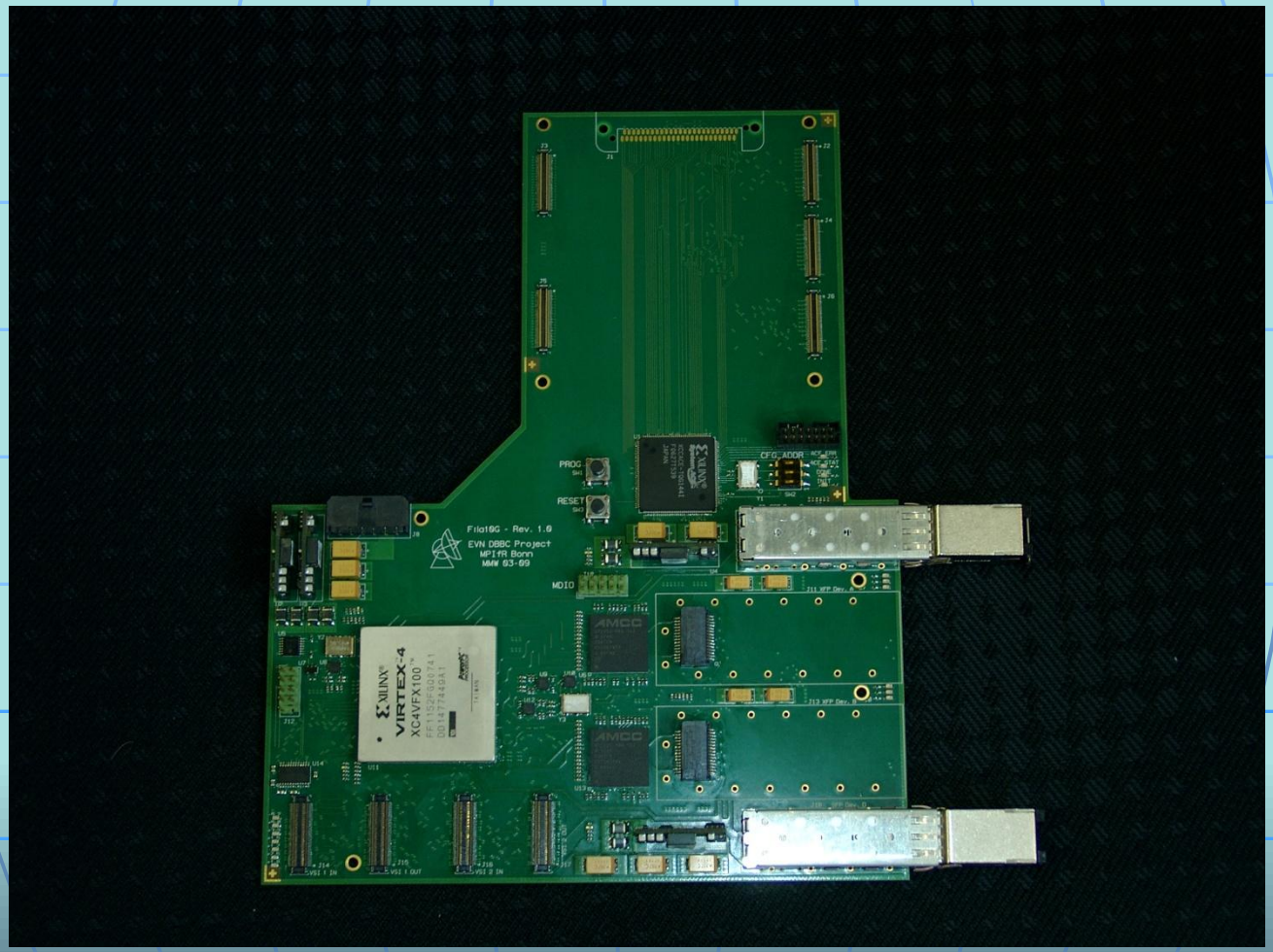
Connection examples

- 2 x VSI --> Network

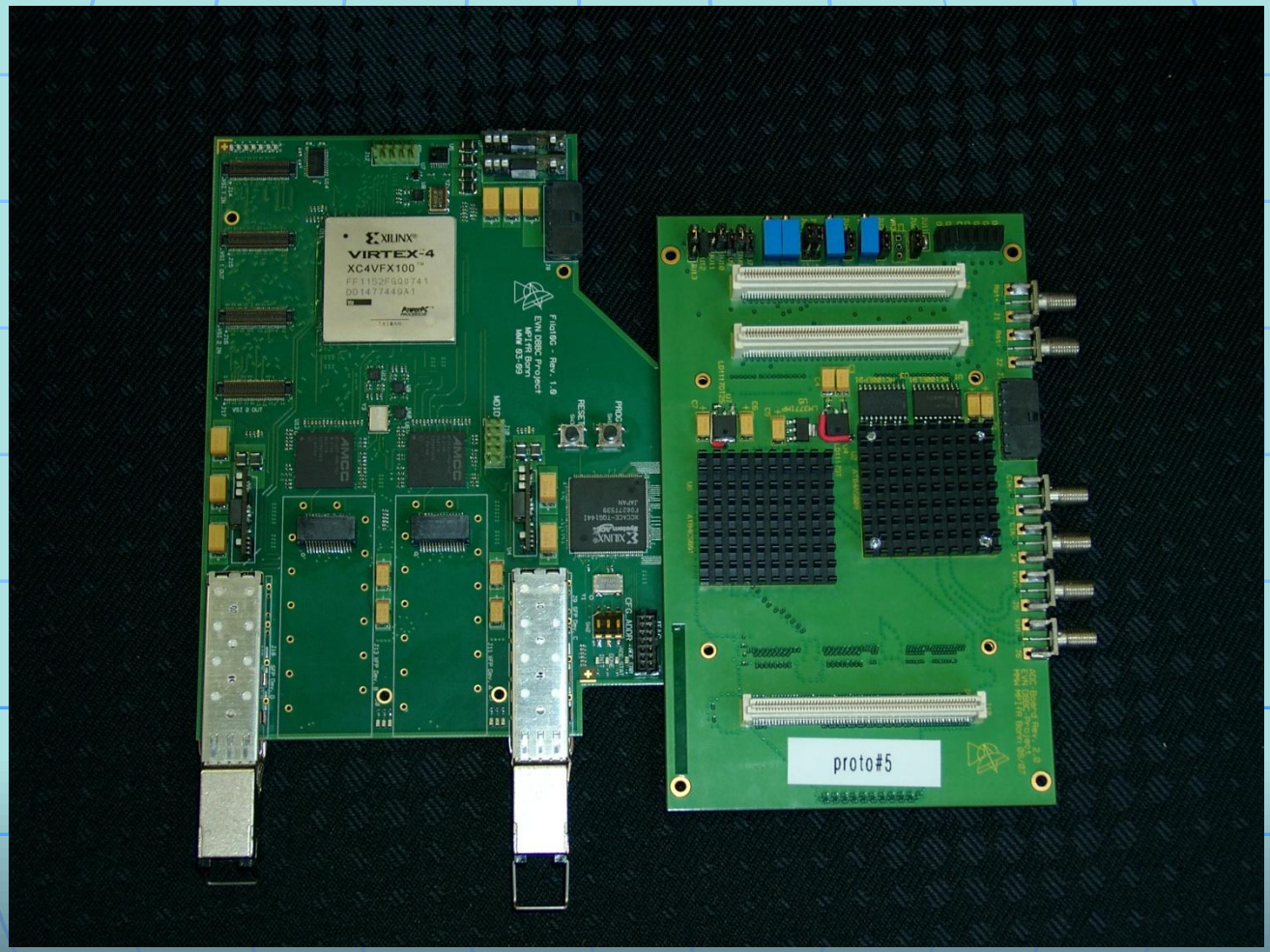
1/2xVSI → FILA10G - - - → 10 Gbps Network

DBBC → FILA10G - - - → 2 - 4 -8 - 16 Gbps e-VLBI

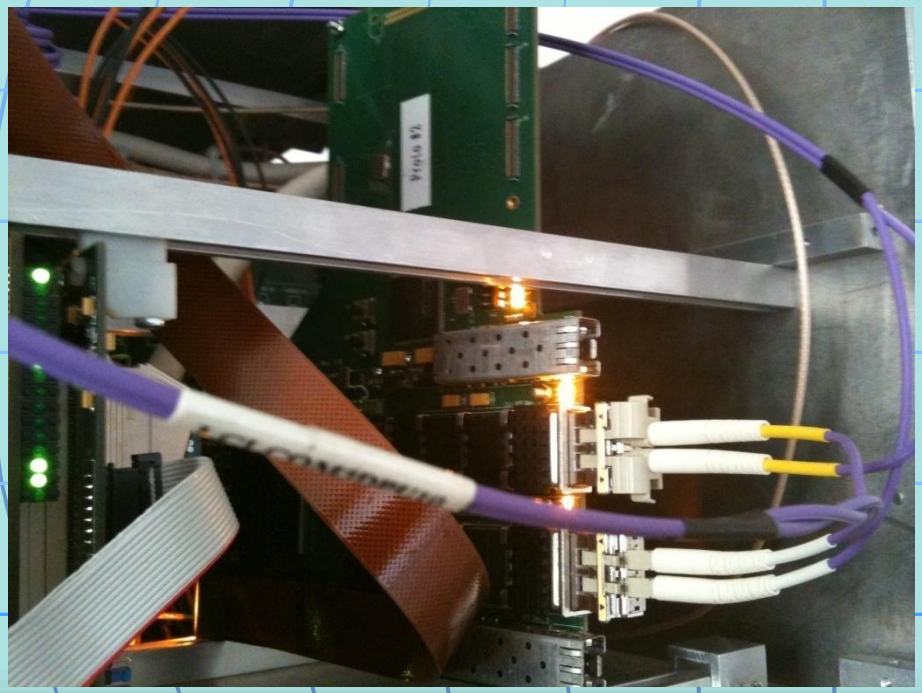
FILA10G

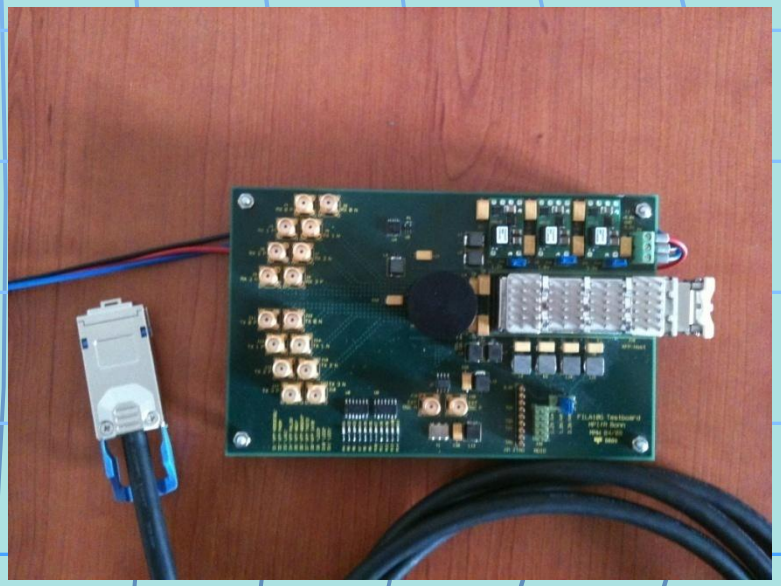

Fila10G - Rev. 1.0
EVN DBBC Project
MPIfR Bonn
MAY 03-09
PROG
RESET
MDIO
CFG_ADDR
XILINX
VIRTEX-4
XC4VFX100
AMCC
AMCC

FILA10G and ADB2



FILA10G and GLAPPER





Software

- **General: c:\DBBC\bin\clock1024.exe (CAT2 1024)**
  c:\DBBC\bin\clock2048.exe (CAT2 2048)
  c:\DBBC\bin\ad9858.exe (CAT1)
  c:\DBBC\bin\DBBC client.exe

- **DDC : c:\DBBC\bin\DBBC Control.exe**
- **c:\DBBC_conf\dbbc_config_file.txt**
  c:\DBBC_conf\FilesDBBC\dbbc2.bit

- **PFB: c:\DBBC\bin\DBBC poly16 complete.exe**
- **c:\DBBC_conf\dbbc_poly_config_file.txt**
  c:\DBBC_conf\FilesDBBC\poly_dbbc.bit

Software on socket

- **DDC : c:\DBBC\bin\DBBC Control net.exe (server)**
  c:\DBBC_conf\dbbc_config_file.txt
  c:\DBBC_conf\FilesDBBC\dbbc2.bit

- **PFB: c:\DBBC\bin\DBBC Control poly16 net.exe (server)**
  c:\DBBC_conf\dbbc_poly_config_file.txt
  c:\DBBC_conf\FilesDBBC\poly_dbbc.bit

In development

- 512 MHz DDC out tunable 32MHz
- 1 GHz DDC out tunable 32MHz
- 1 GHz Parallel Polyphase Filterbank (31ch x 32 MHz)
- 512 MHz SB (single band 16tr@64MHz 2bit)
- 1 GHz SB (single band 32tr@64MHz 2bit)
- Spectrometer 4x512MHz, 32768 total # bin
- Spectropolarimeter

DBBC2 DDC Command Set (ver 06. 04.11)

Description

This document describes the basic commands the DBBC is able to recognize with the control console. The structure and the meaning of the different commands is Field System based, so to simplify the dialogue with the FS and minimize efforts on the FS side. Any commands sent to the interpreter from the DBBC console is then similar to the command sent from the Field System environment. Similarly output information issued by any command are reported in FS style.

Syntax check included

DDC Standard commands

DBBCnn = freq, IF, bwdU, bwdL

where

nn => 01, .. ,16 indicates the number of bbc;

freq => is the base band frequency in MHz, in the range 0010.000000 - 2,200.000000;

IF => A or B or C or D. Any Core2 is connected to a band in the standard communication so this value is only informative.

bwdU => band width of the upper side, in MHz;

bwdL => band width of the lower side, in MHz;

bwdL and bwdU are always the same in a single bbc.

DBBCnn

reports the setting of the bbc nn,

DBBCnn/freq,IF,bwdU,bwdL,tpint, gainctrl, gainU, gainL, tpU/calon, tpL/calon, tpUcaloff, tpLcaloff

freq => is the base band frequency in MHz, in the range 0010.000000 - 2,200.000000;

IF => A or B or C or D. Any Core2 is connected to a band in the standard communication so this value is only informative.

bwdU => band width of the upper side, in MHz;

bwdL => band width of the lower side, in MHz;

tpint => tp integration time, always 1s

gainctrl => agc | man, manual is set with ‘dbbcgain’ command

gainU => USB gain;

gainL => LSB gain;

tpU/calon => USB total power, if cal is on during the ‘on’ period;

tpL/calon => LSB total power, if cal is on during the ‘on’ period;

tpUcaloff => USB total power, when cal is on during the ‘off’ period, otherwise 0;

tpLcaloff => LSB total power, when cal is on during the ‘off’ period, otherwise 0;

DBBCIF(A,B,C,D) = input_ch, attenuation, filter

where

input_ch => input channel of the four possible (1,2,3,4) .

attenuation => the gain of the channel is set in manual mode if a number is indicated in the range 0 - 32 dB, step 0.5 dB. If AGC is indicated the gain is automatically set so to satisfy the optimal level for the analog to digital converter. If MAN is indicated automatic gain control is stopped.

filter=> 2 (10-512 MHz), 1 (512-1024 MHz), 3 (ext 1), 4 (ext 2)

DBBCIF

reports the settings of the IF x module.

DBBCIFx/ input_ch, gain, attenuation, gainctrl, filter

input_ch => input channel of the four possible (1,2,3,4) ;

attenuation => in the range 0 - 32 dB
gainctrl => agc | man;

filter=> 2 (10-512 MHz), 1 (512-1024 MHz), 3 (ext 1), 4 (ext 2)

DBBCFORM = VSI mode

VSImode => is the mapping of the 64 channels in the VSI1/2 interfaces. Possible predefined values are: GEO, ASTRO,WASTRO,TEST. If TEST is indicated an addition parameter is needed: 0 all VSI output are set to 0, 1 all VSI output are set to 1, tvg VSI output contain mk5b test vector, bin VSI output contain binary counter

DBBCFORM

reports the settings of the VSI output mapping.

VSImode => astro | geo.

DBBCMON= bnn[u|l]

set the Digital to Analog Channel source.

nn => 01,02,..,16   indicates the number of bbc;
u/l => upper or lower side band

DBBCMON

reports the Digital to Analog Channel source.

PPS_SYNC

Synchronize to the external 1pps

DBBCGAIN=dbbcnn,gainU,gainL

Set the gain level

dbbcnn => 1, 2, .., 16
gainU => 0, 1, .., 255, step 1
gainL => 0,1, .., 255, step 1

DBBCGAIN

Reports the gain settings.

CONT_CAL = status

Continuous calibration noise diode activation at 80 Hz rate.

status => on| off

CONT_CAL

Reports the status of the continuous calibration noise diode activation

RECONF

System reconfiguration.

LOGFILE = mode

If activated the command generates a log file in C:\ with a name reporting the activation time containing gain control and total power of the entire set of bbcs and IF modules.

LOGFILE

Reports log file activation status and name.

LOAD = filename.txt (beta version)

Load data settings.

Service Commands

MAG_THR =channel,[correction]

Magnitude threshold correction factor. It's set by default at 0.042 for 16 and 32 MHz bands and 0.0605 for the other bands. It can be slightly redefined for a finest correction.

correction => any real number, it's effective in a narrow range around the default value.

Reports the magnitude threshold correction factor settings for the channel specified.

DBBCSTAT = bbcn, bit

Statistics of the high states expressed in hex with respect to 0x7A12.

bbcn => bbc number, 1,2, , 16

bit => s | m, sign or magnitude bit selection.

CALIBRATION
Start calibration process and create output file in C:\YYYY-doyTHHMMSS-calib.txt

VERSION
Print program version.

END_SERVER
End client and server programs.

EXIT
End client program.

DBBC2 PFB Command Set (ver 06. 04.11)

Syntax check included

PFB Standard commands

power = nn

total power reading for a bank of 15 adjacent channels as produced by a single Core2 board.

nn => 1, .. ,4 indicates the board number;

Reports the total power values for a PFB.
reports the setting of the bbc nn,

if(a|b|c|d)= input_ch, attenuation, filter

where

input_ch => input channel of the four possible (0,1,2,3) .

attenuation => the gain of the channel is set in manual mode if a number is indicated in the range 0 - 63 dB, step 0.5 dB. If ‘agc’ is indicated the gain is automatically set so to satisfy the optimal level for the analog to digital converter. If ‘man’ is indicated automatic gain control is stopped.

filter=> 1 (10-512 MHz), 0 (512-1024 MHz), 2 (ext 1), 3 (ext 2)

threshold=on|off

Set thresholds

on	start automatic control
off	stop automatic control

mon= nn,ch

set the Digital to Analog Channel source.

nn => 1,2,3,4 board number
ch => 1,2,..,15 channel number

sync

Synchronize to the external 1pps

cont_cal = status (to be implemented)

Continuous calibration noise diode activation at 80 Hz rate.

status => on| off

configure

System reconfiguration.

calibration

Start calibration process and create output file in C:\YYYY-doyTHHMMSS-calib.txt

version

Print program version.

reset

DCM reset

reg_read=board,reg

Read register

board 1,..,4 board number
reg register

reg_write=board,reg,value

Write register

board	1,..,4	board number
reg		register
value		value to write

end_server

End client and server programs.

exit

End client program.