



**DBBC3**

# **DEVELOPMENT OF A 32 GBPS DIGITAL BACKEND**

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**IVTW HAYSTACK 2012**



# DBBC3

- Project supported by EU Radionet3
- Partner:
  - INAF – Italy
  - MPIfR - Germany
  - OSO – Sweden
- Starting date July 2012, 3 years

# Background

- Astronomic VLBI requires improvement in the overall sensitivity (4Gbps EVN, mmVLBI, 32Gbps EVN)
- Geodetic VLBI requires improvement in delay determination (VLBI2010)
- Current state of the art technologies offers every day new opportunities
- Two generation of the DBBC system represent a reasonable starting platform to develop a higher data rate backend

# DBBC Evolution

## **DBBC1** 2004 - 2008

in: 4 x IF-512MHz

out: **DDC** 16xbbc(1-2-4-8-16MHz)@32MHz

**0.512/1.024Gbps**

## **DBBC2** 2007 – to date

in: 4 x IF-512/1024MHz

out: **DDC** 16xbbc(1-2-4-8-16MHz)@32MHz

**PFB** 4 x 16 x 32MHz@64MHz

**4.096/8.192Gbps**

## **DBBC2010** 2009 – to date

in: 8 x IF – 512/1024MHz

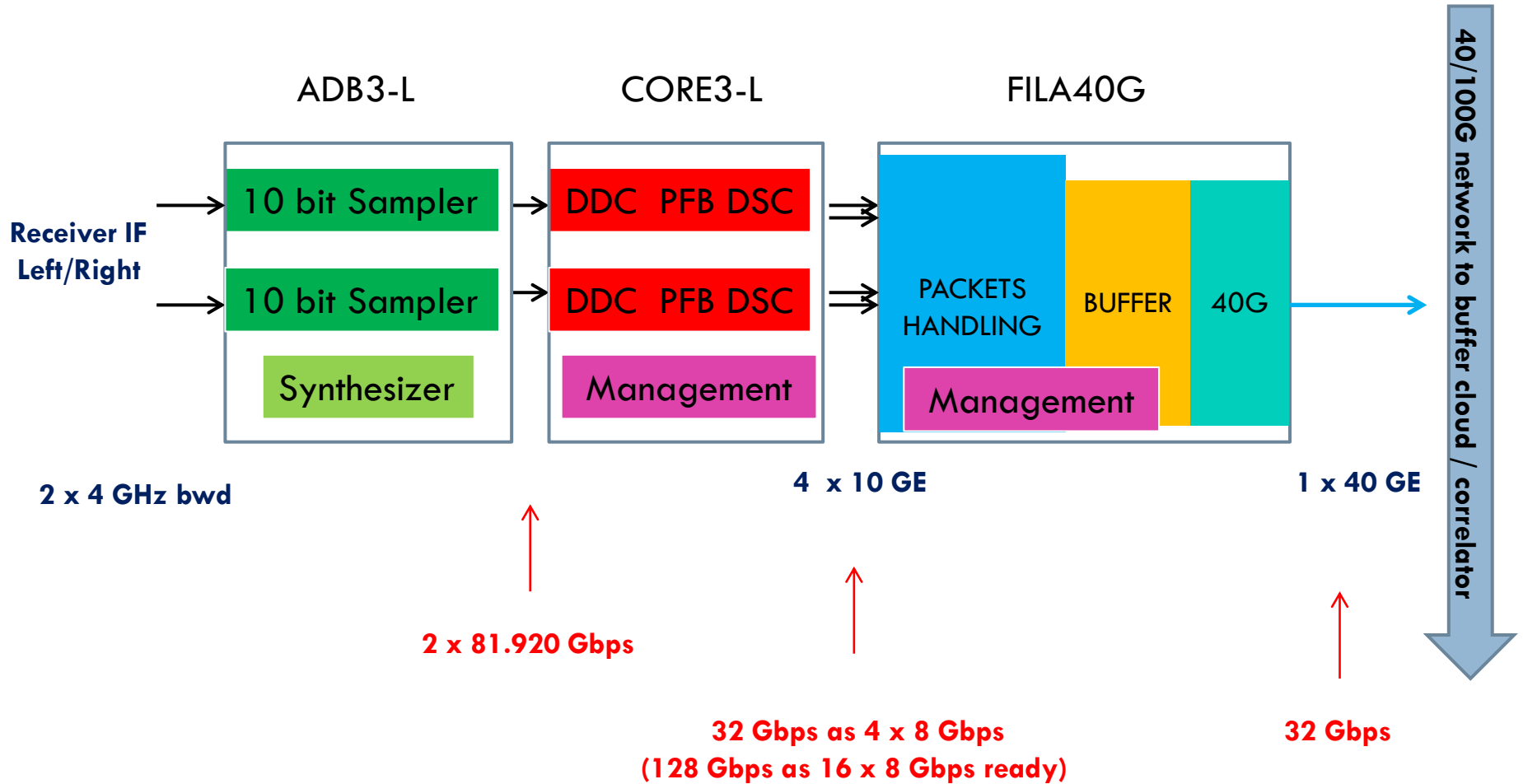
out: **PFB / DSC**

**16.384/32.768Gbps**

# DBBC3 General Performance for EVN

- Number of Input IF: **1 - 4**
- Instantaneous bandwidth ea. RF:  **$\geq 4$  GHz**
- Sampling representation: **8-10 bit**
- Processing capability: **able to support wide band DDC, PFB, DSC and more (pulsar, polarimetry, spectroscopy, holography, etc.)**
- Output: **VDIF Ethernet packets,  $\geq 32$ Gbps**
- Compatibility with the existing DBBC environment

# DBBC3 Architecture for EVN



# ADB3-L General Performance

## □ ADB3-L:

Number of IFs: **2**

Equivalent Sample Rate ea. IF: **8.192 GSps**

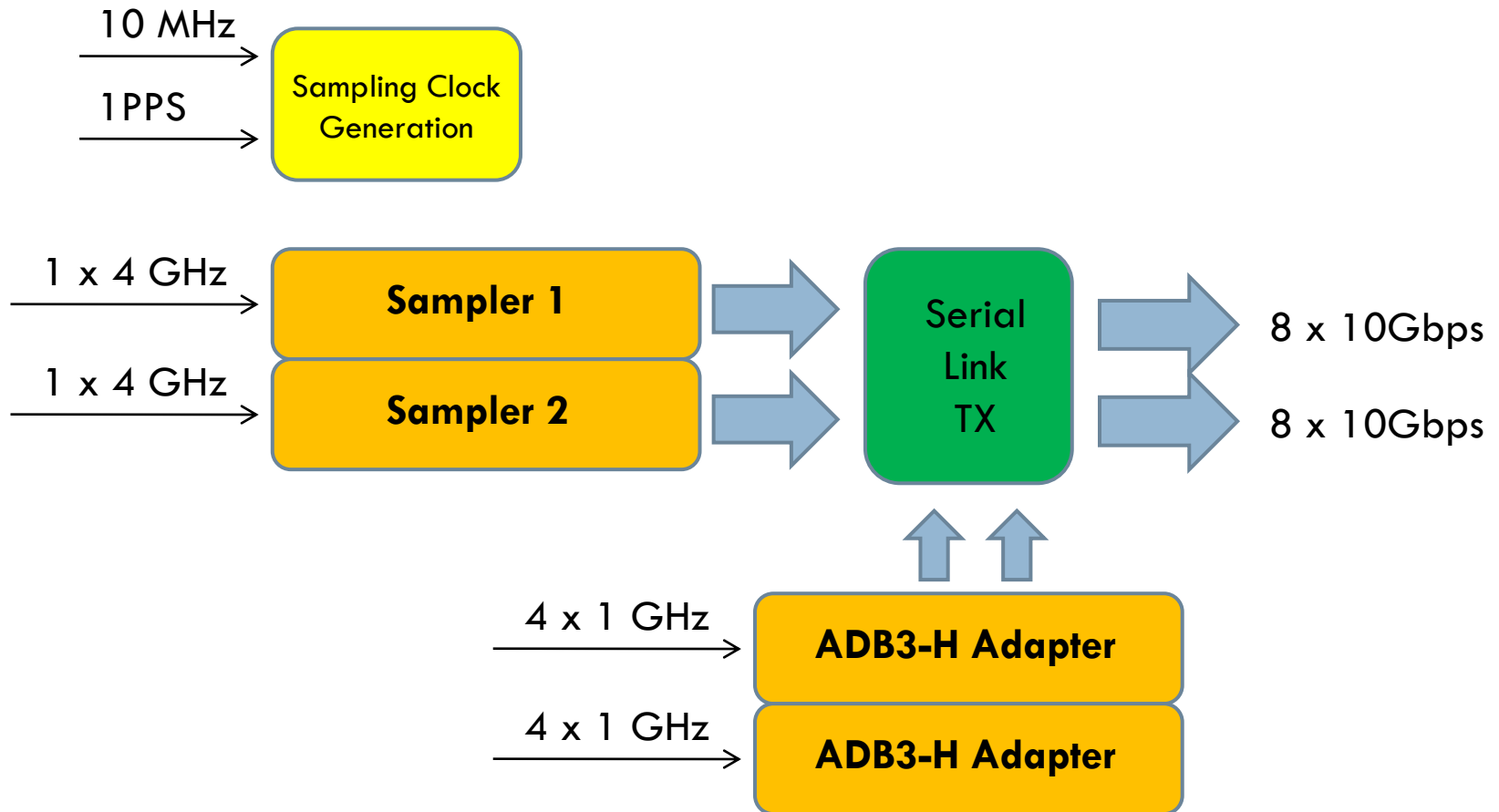
Instantaneous bandwidth ea. IF: **4 GHz**

Internal Sampling representation ea. : **10 bit**

□ Real/Complex Sampling

□ Compatibility with the existing DBBC environment

# ADB3-L Sampler





# CORE3-L General Performance

## □ Core3-L

Number of Input: **max 16 serial links 10Gbps**

Number of Output: **max 16 serial links 10Gbps**

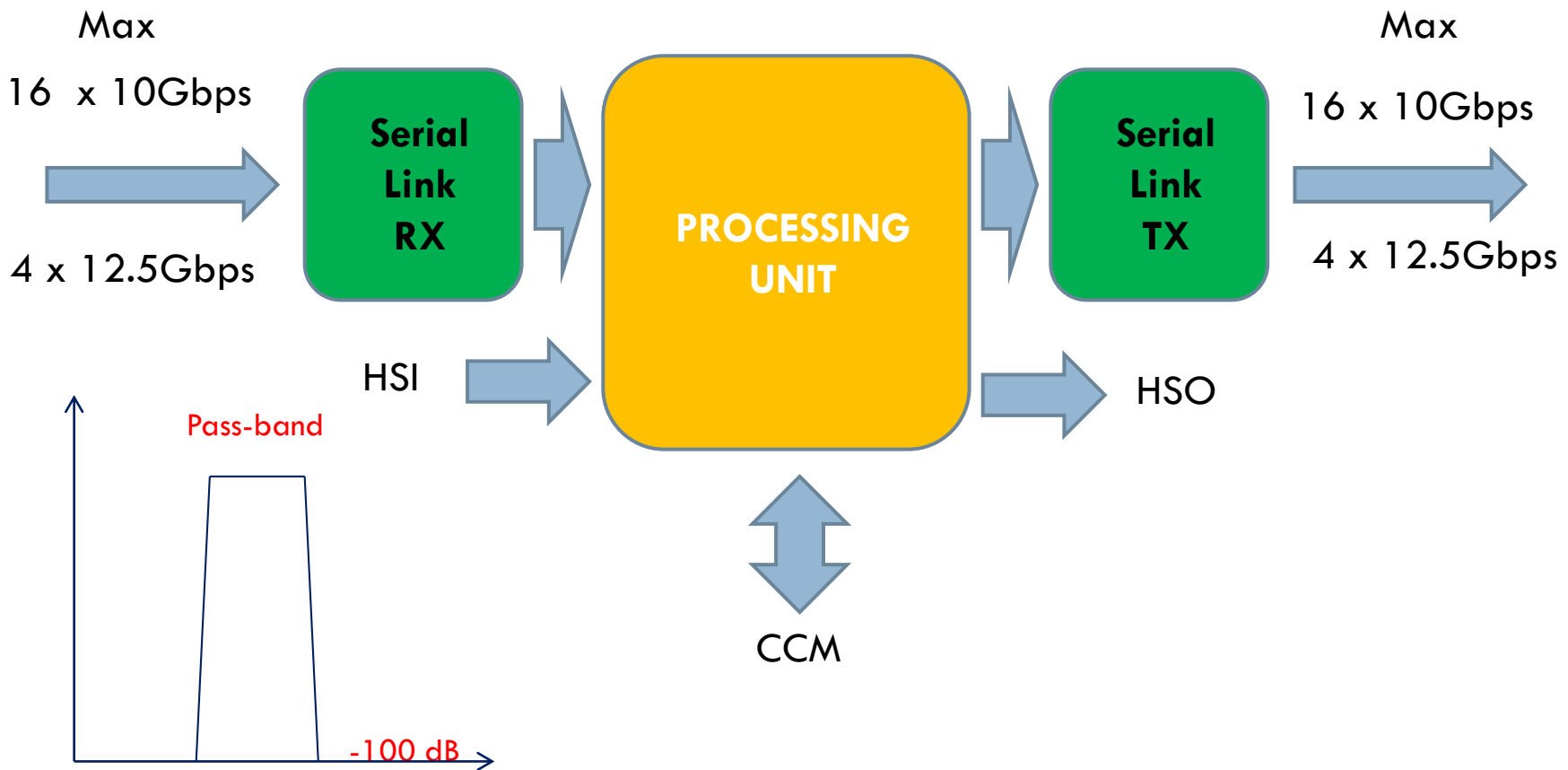
Input Sampling Representation: **8 -10 bit**

Processing capability: **DDC, PFB, DCS**

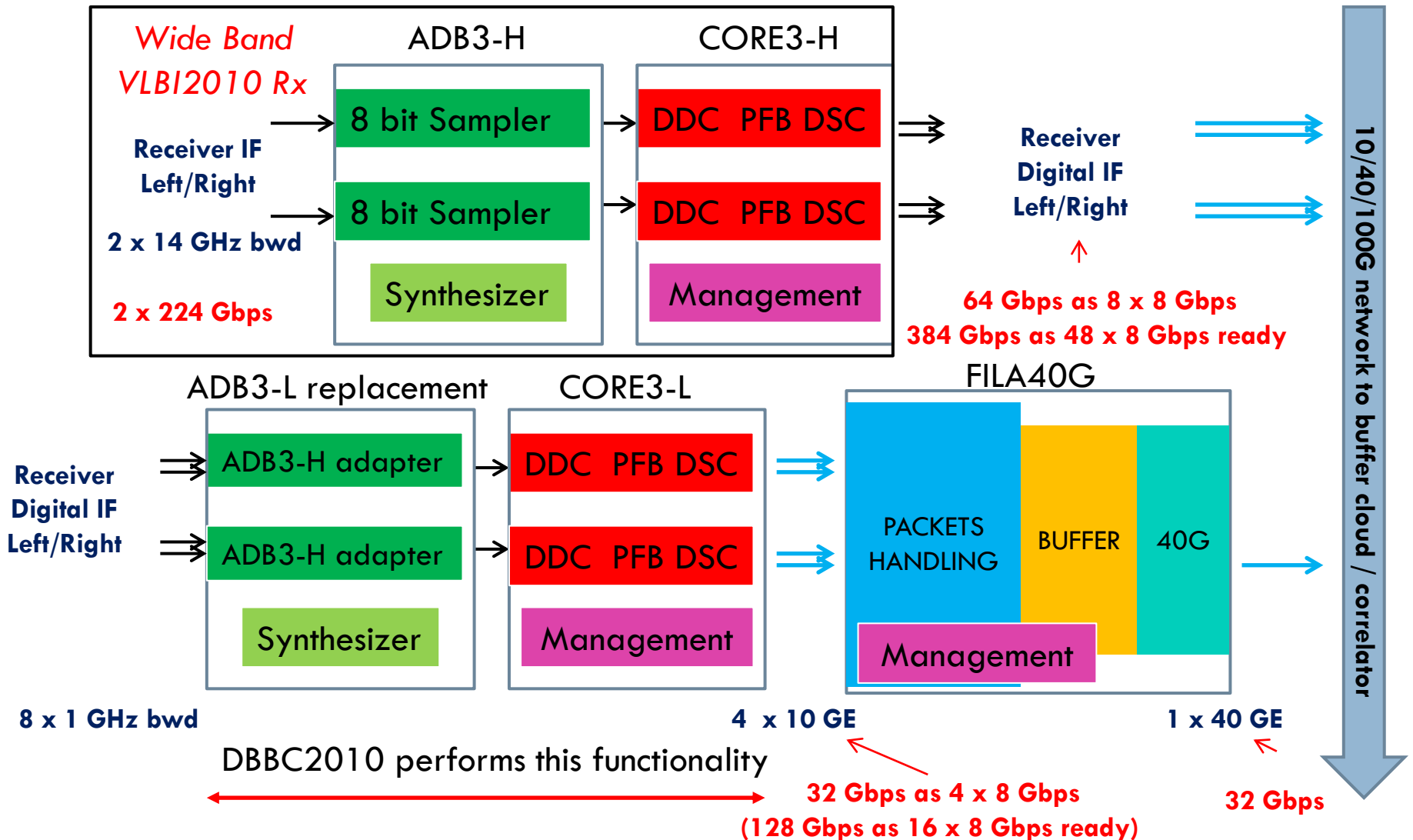
Output: **VDIF Ethernet packets,  $\geq 32$ Gbps**

Compatibility with the existing DBBC environment

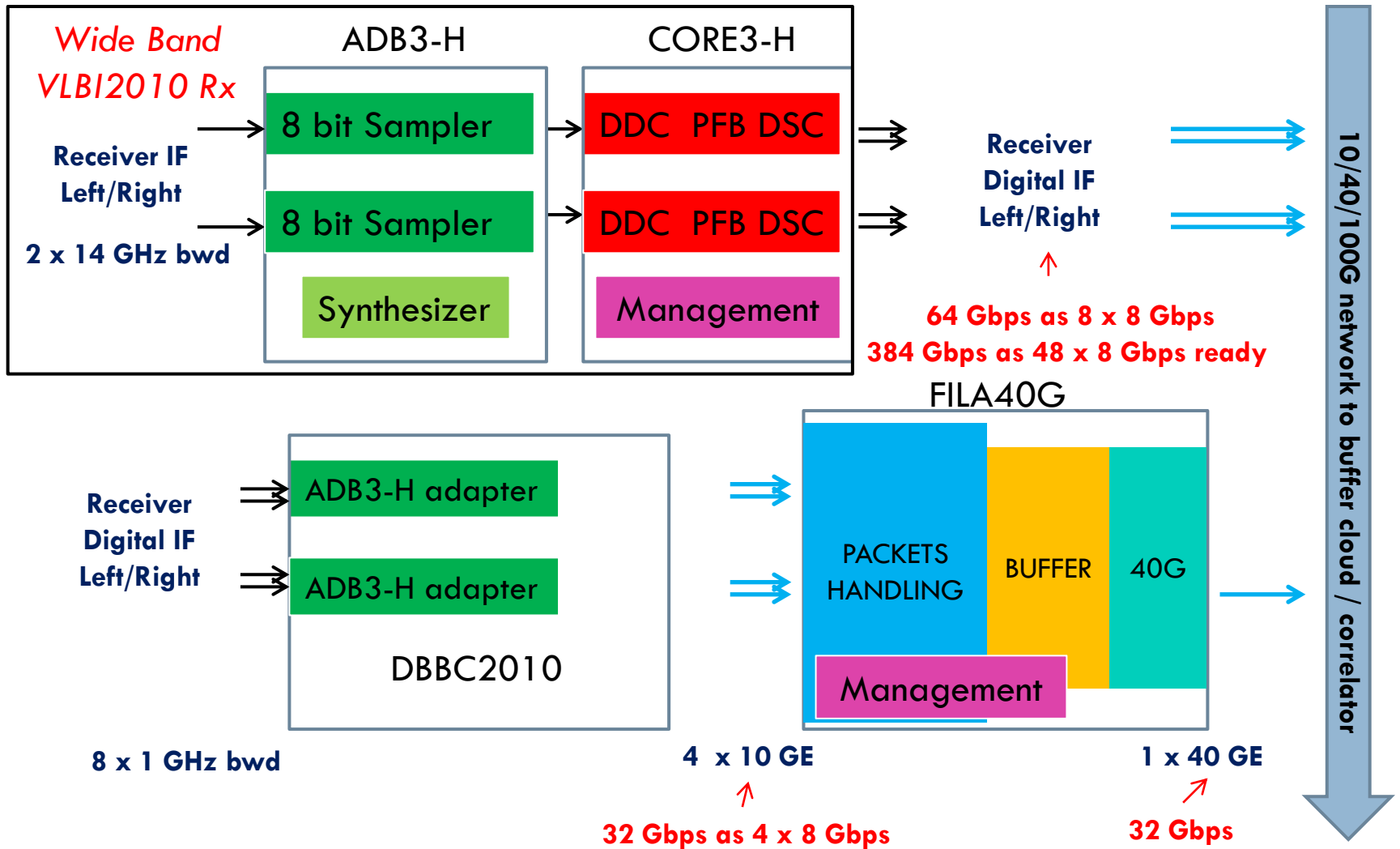
# CORE3-L



# DBBC3 Architecture for VLBI2010



# DBBC3 Architecture for VLBI2010



# ADB3-H General Performance

- **ADB3-H:**

  - Number of IFs: **4**

  - Equivalent Sample Rate ea. IF: **28.672 GSps**

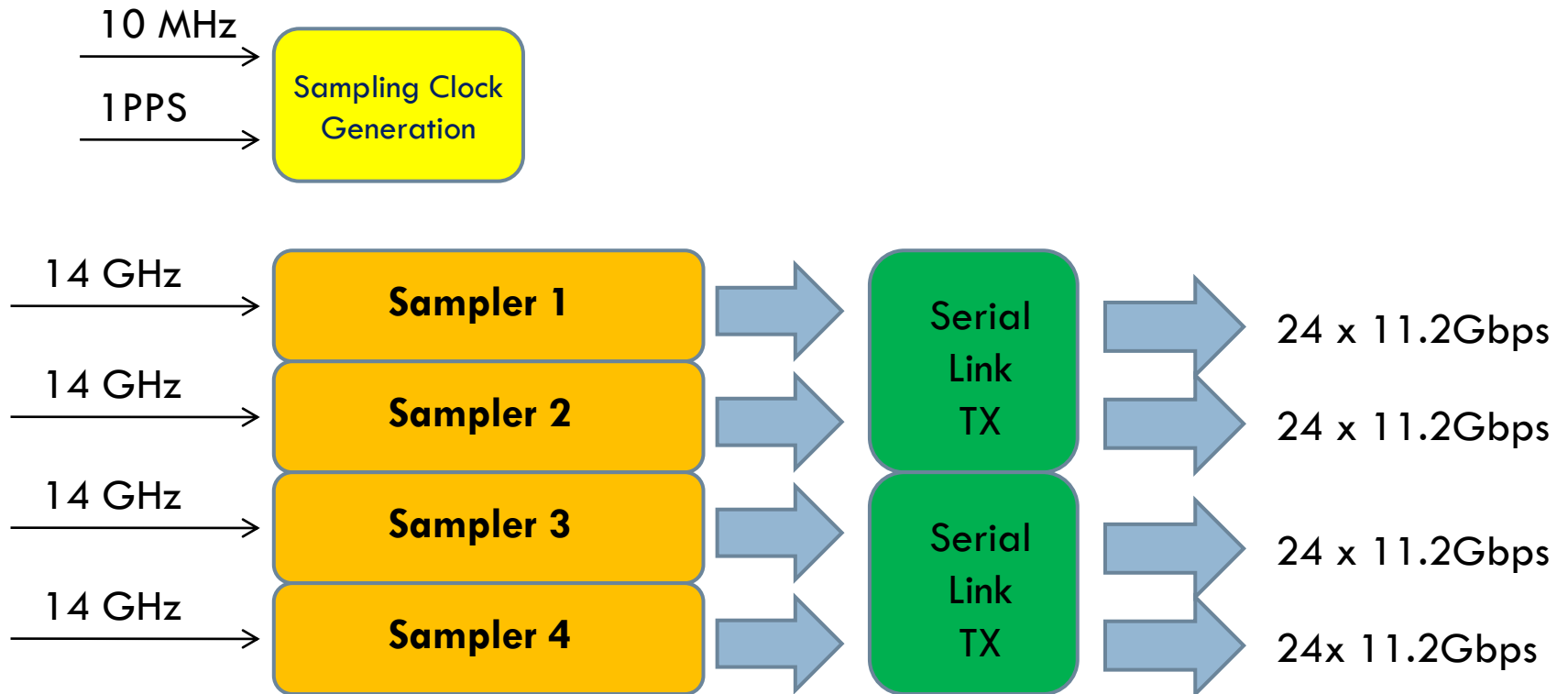
  - Instantaneous bandwidth ea. IF: **14.336 GHz**

  - Sampling representation: **8 bit (ENOB 5.8 - 6.5 bit)**

- Real/Complex Sampling

- Compatibility with existing DBBC environment

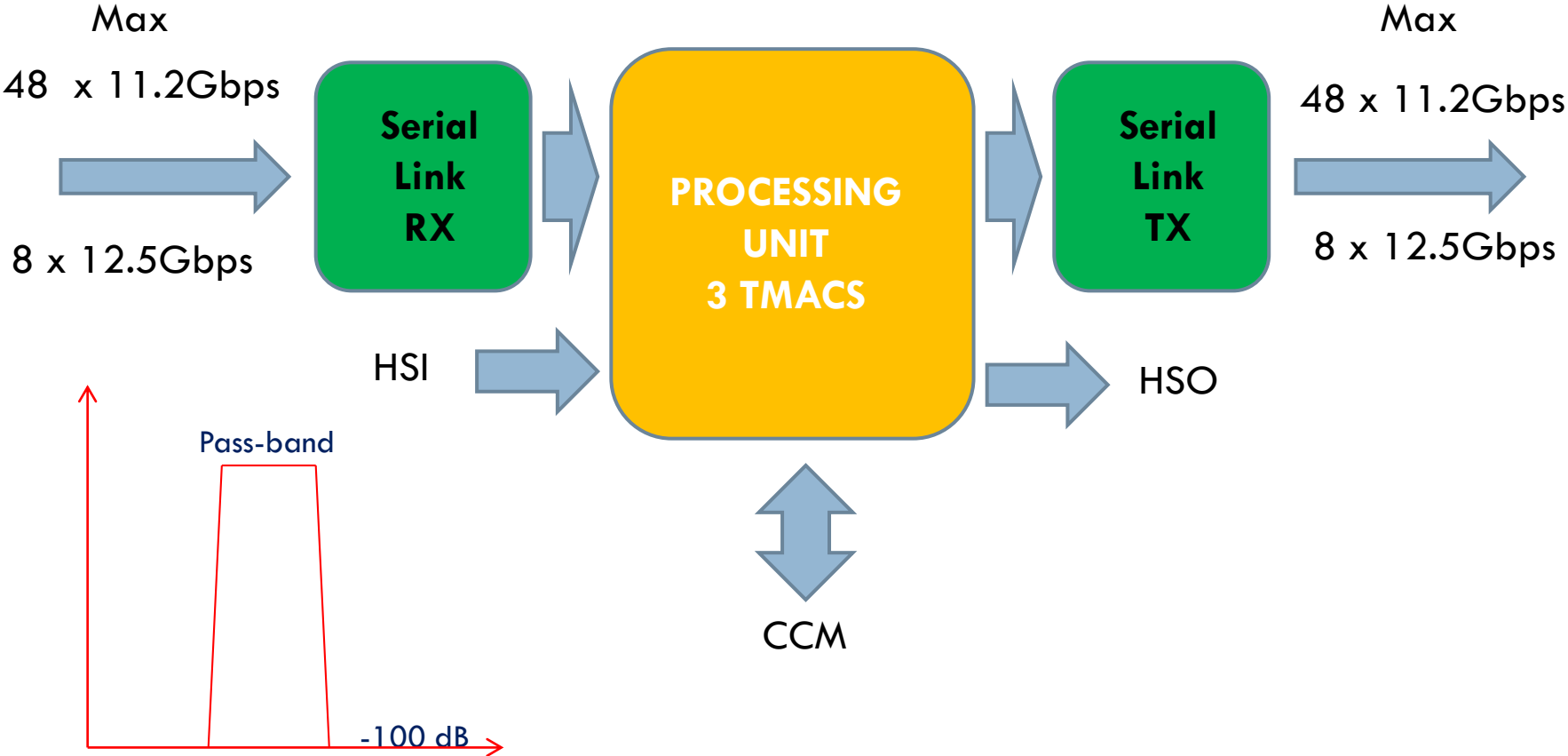
# ADB3-H Sampler



# CORE3-H General Performance

- **Core3-H**
- Number of Input: **max 48 serial links 11.2Gbps**
- Number of Output: **max 48 serial links 11.2Gbps**
- Input Sampling Representation: **8-10 bit**
- Processing capability: **WB\*-DDC, WB\*-PFB, WB\*-DCS**
- Output: **VDIF Ethernet packets,  $\geq 32$ Gbps**
- Compatibility with existing DBBC environment
  
- \* **Wide band**

# CORE3-H



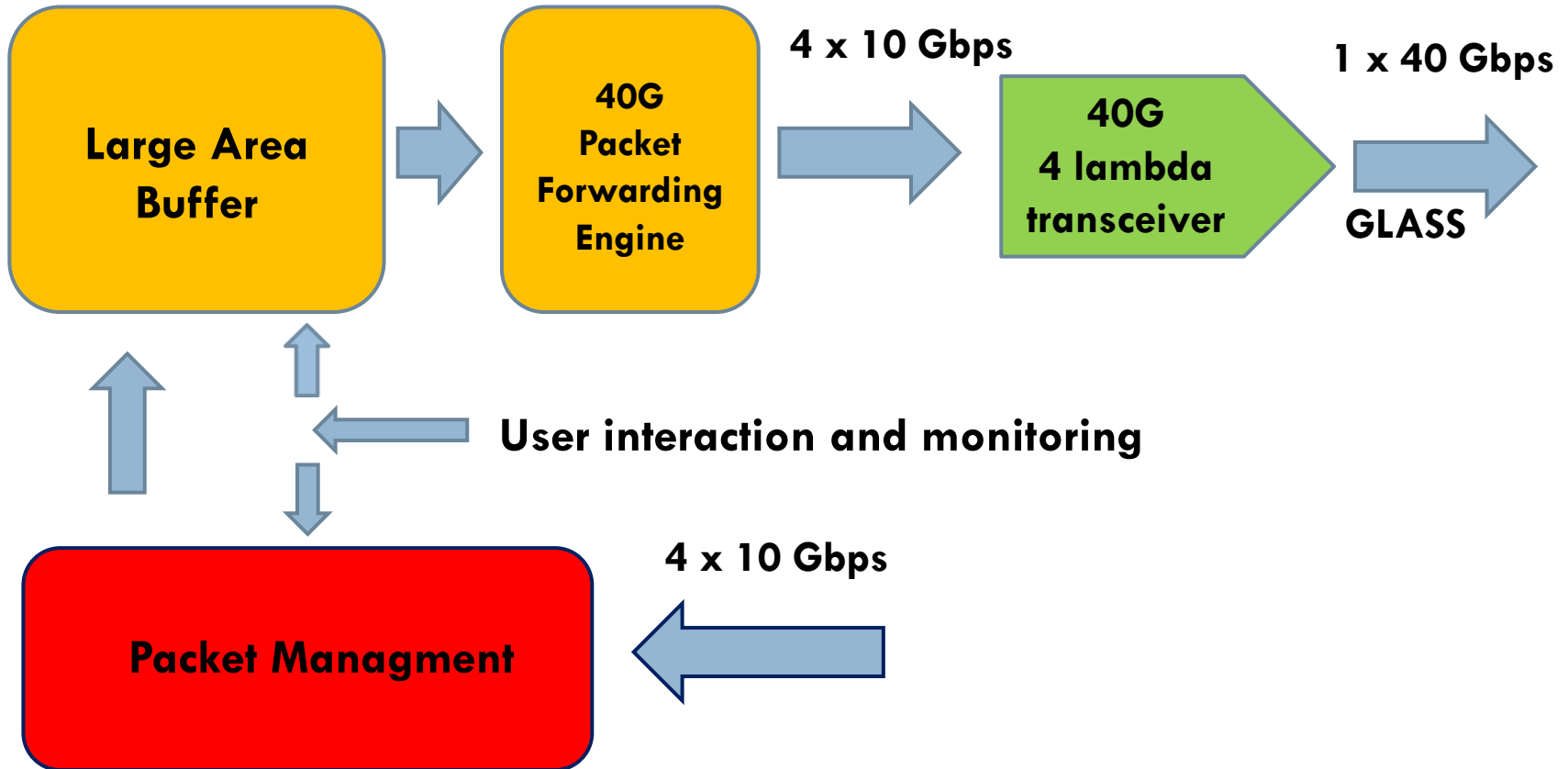


# FILA40G Single Module General Performance

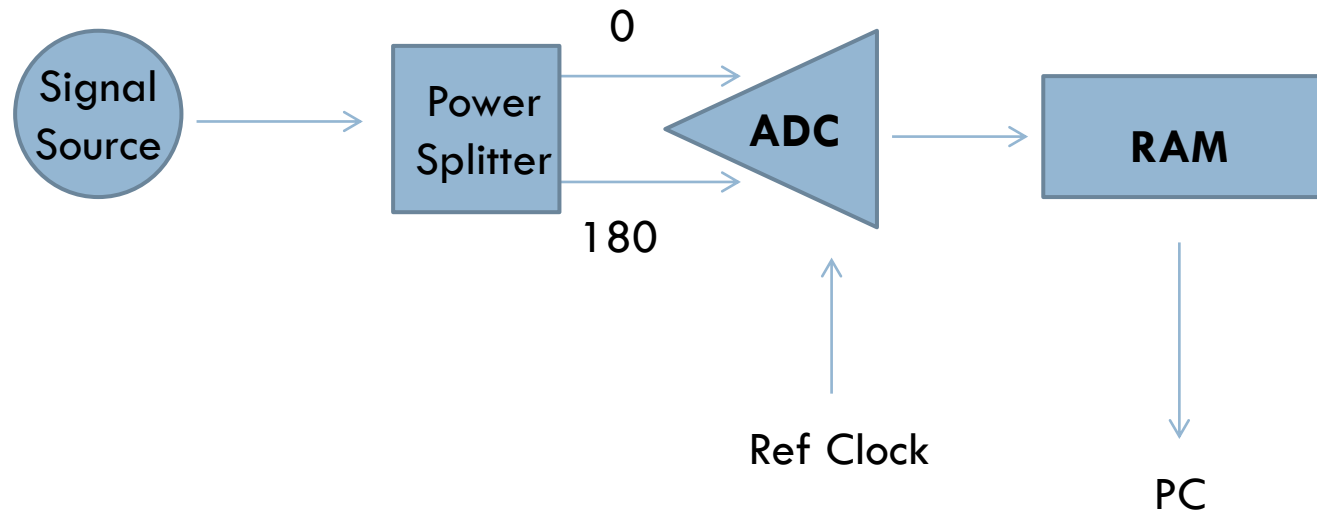
- Serial Link Input: = **4 x 10Gbps**
- Serial Link Processed Output: = **4 x 10Gbps**
- Serial Link Output: = **1 x 40Gbps**
- Packets manipulating capability (filtering, pulsar gating, burst mode, etc.)
- Packets forwarding capability (different correlator nodes, different correlator sites, etc.)
- Packets large buffering (RAM/HD/SSD)
- Packets monitoring capability

# FILA40 Architecture

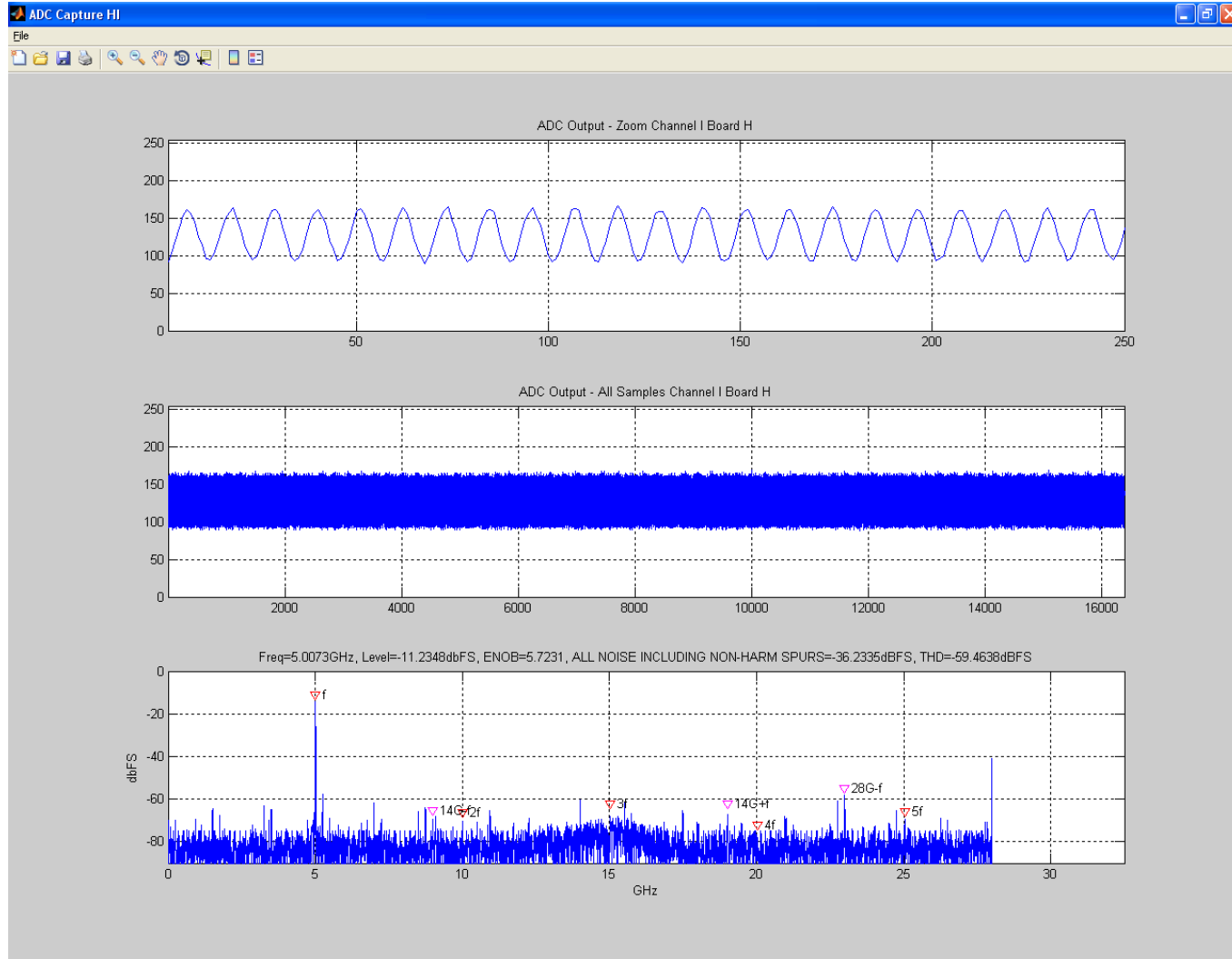
## Single Module



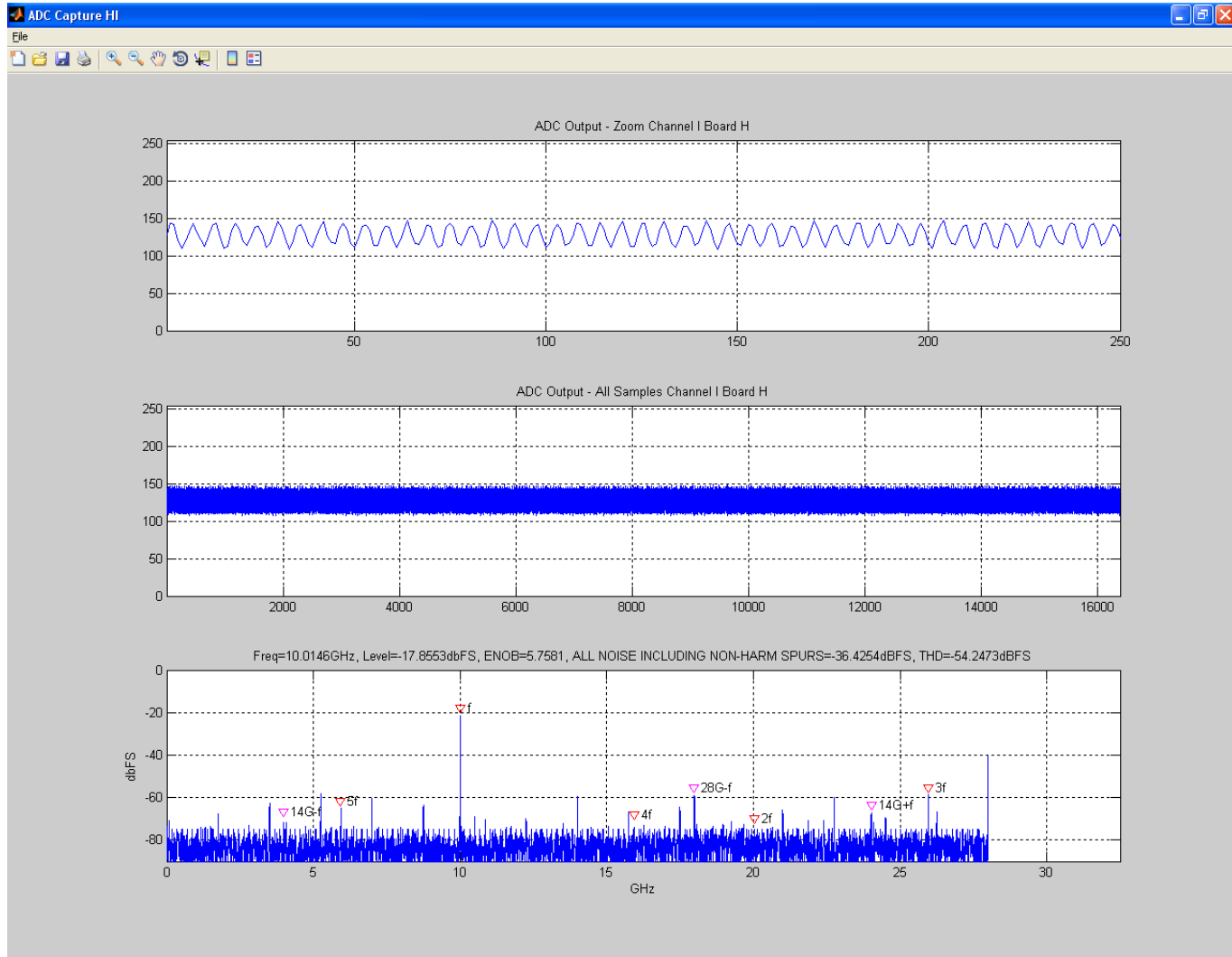
# Some ADB3-H preliminary measurements



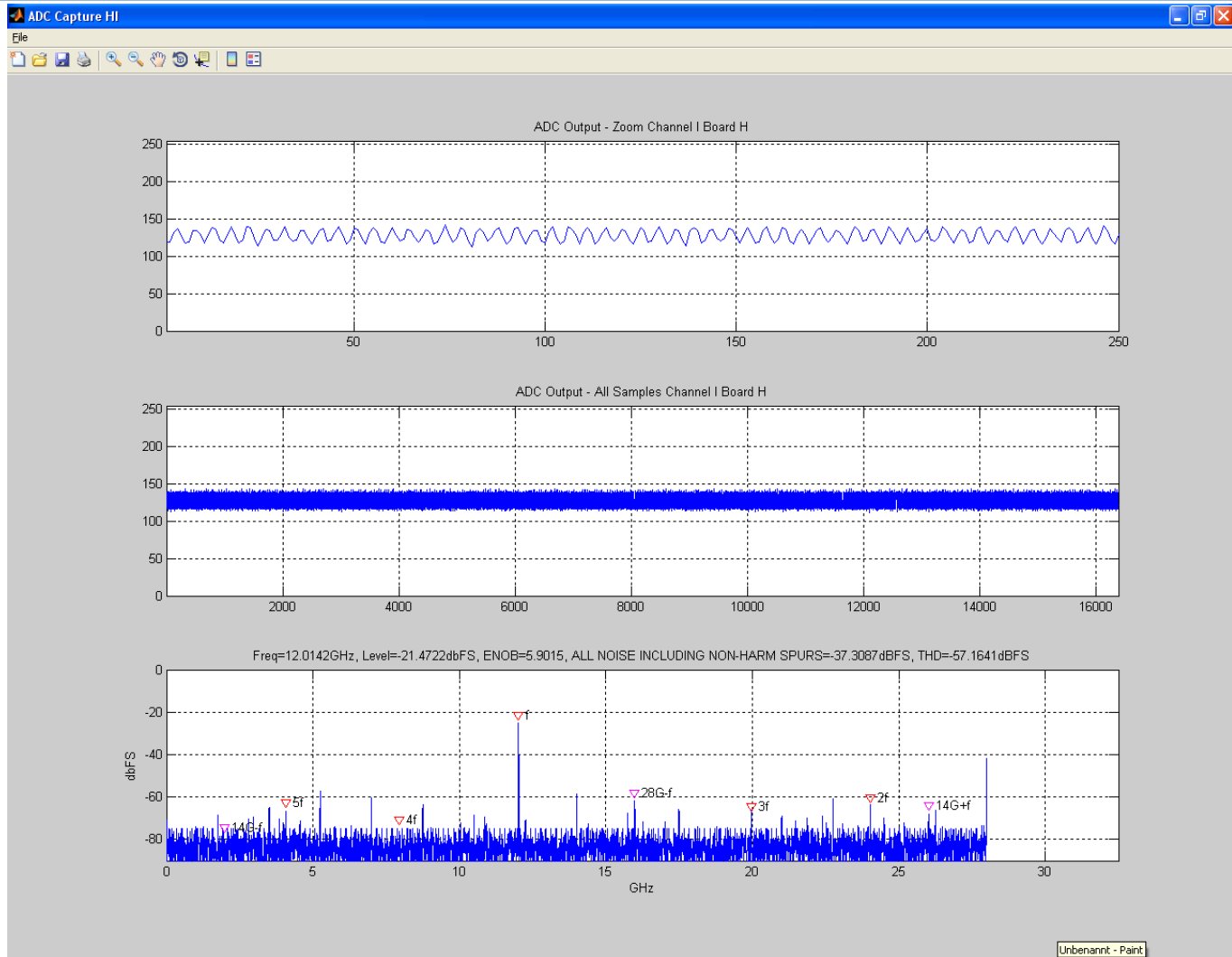
# 5 GHz single tone



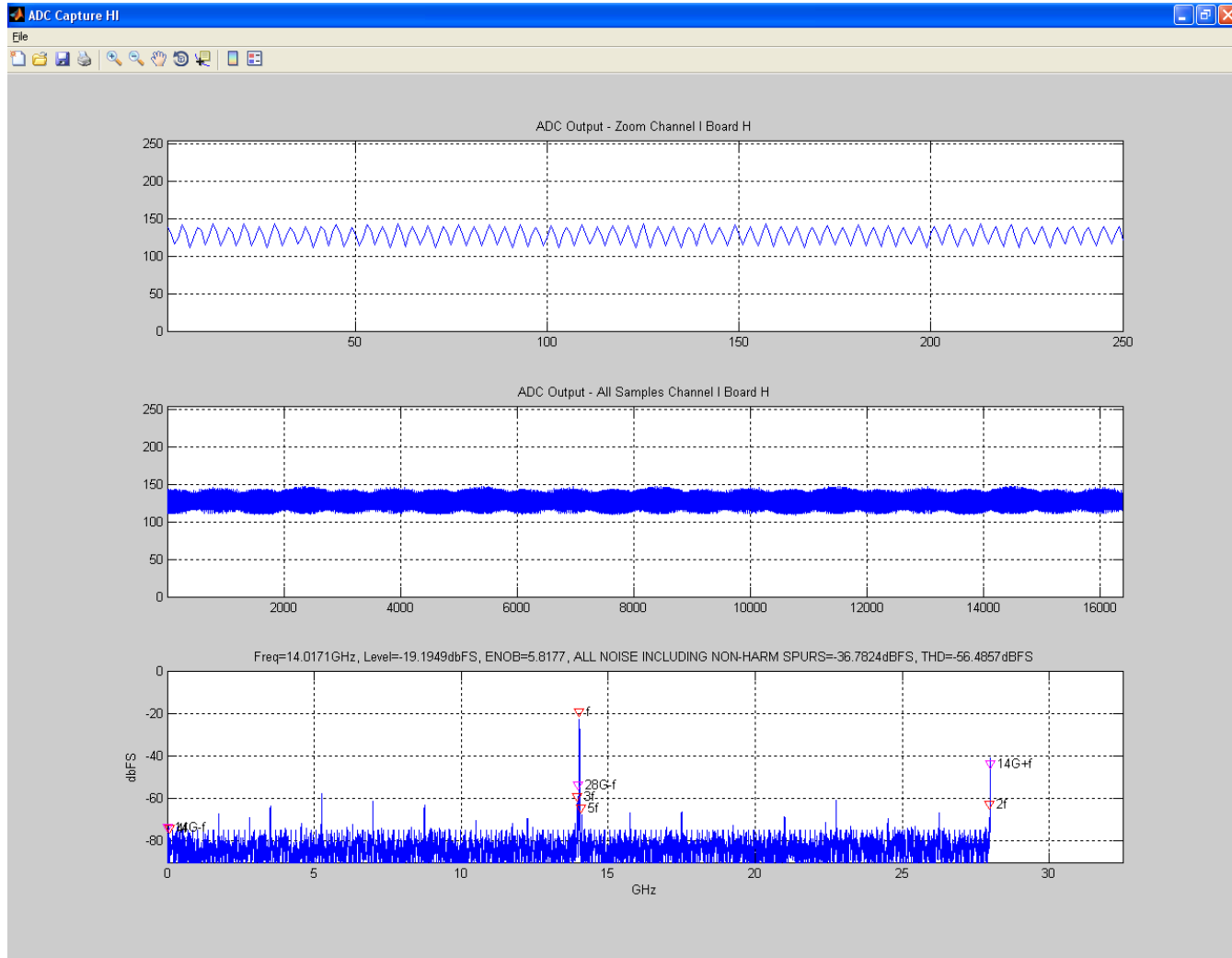
# 10 GHz single tone



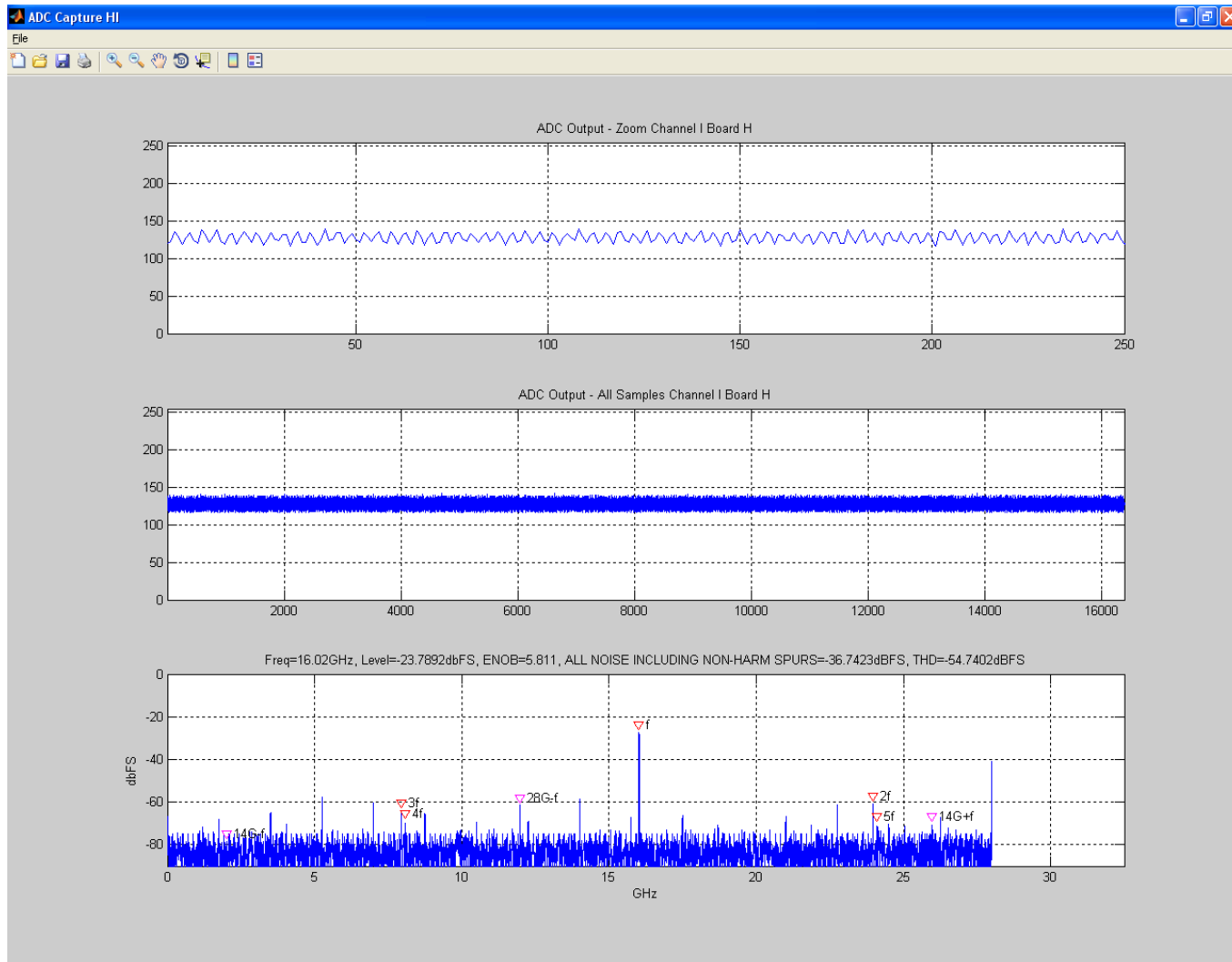
# 12 GHz single tone



# 14 GHz single tone

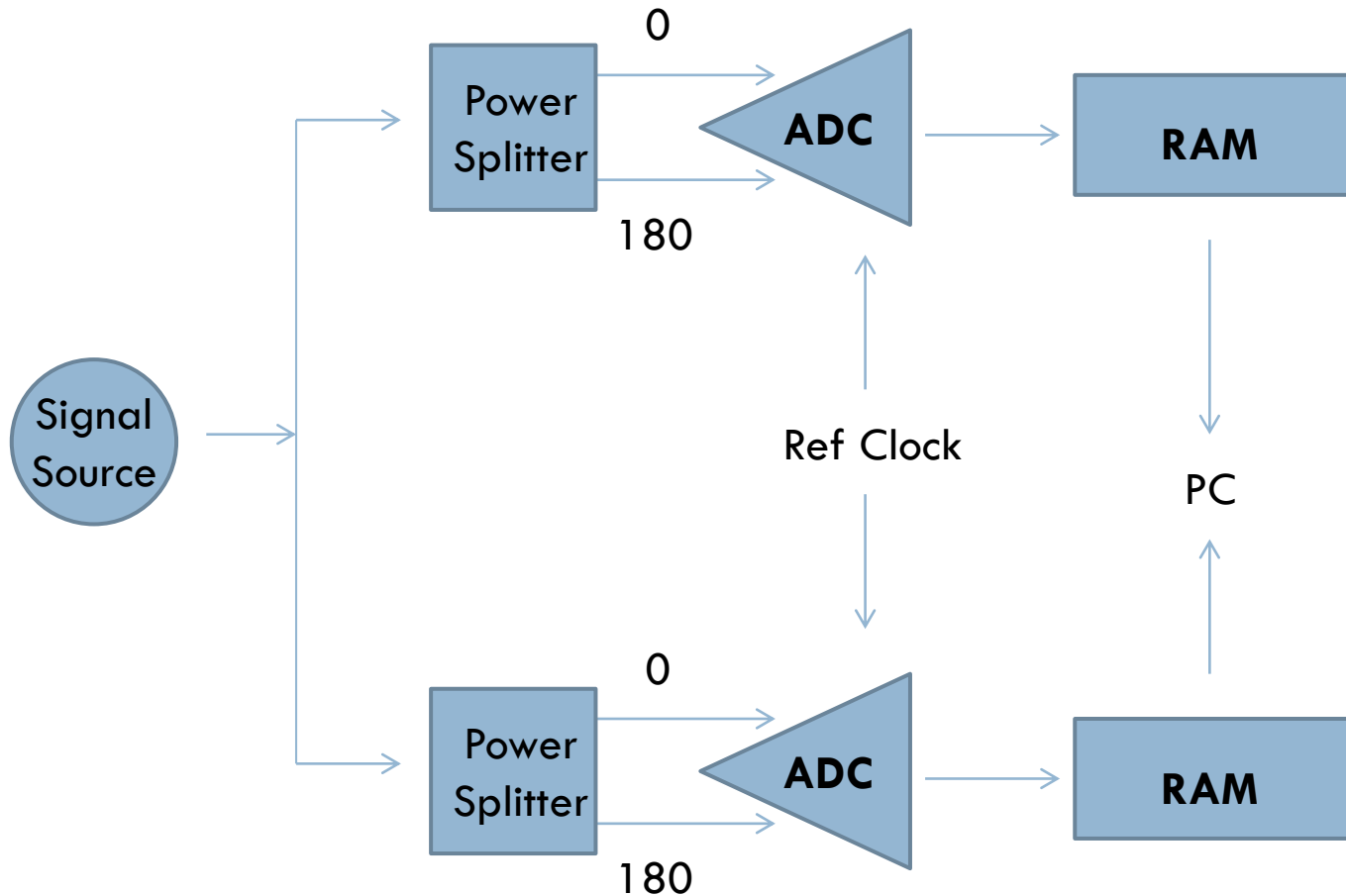


# 16 GHz single tone

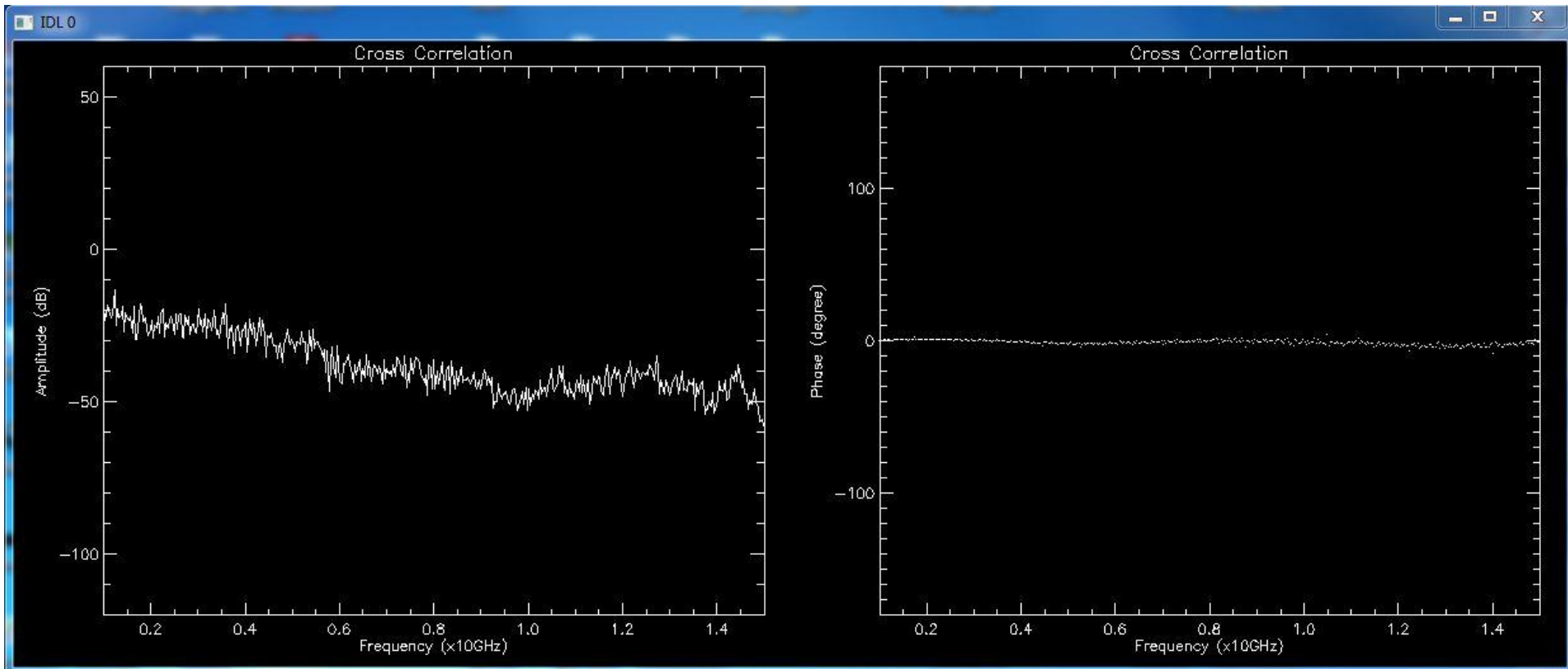




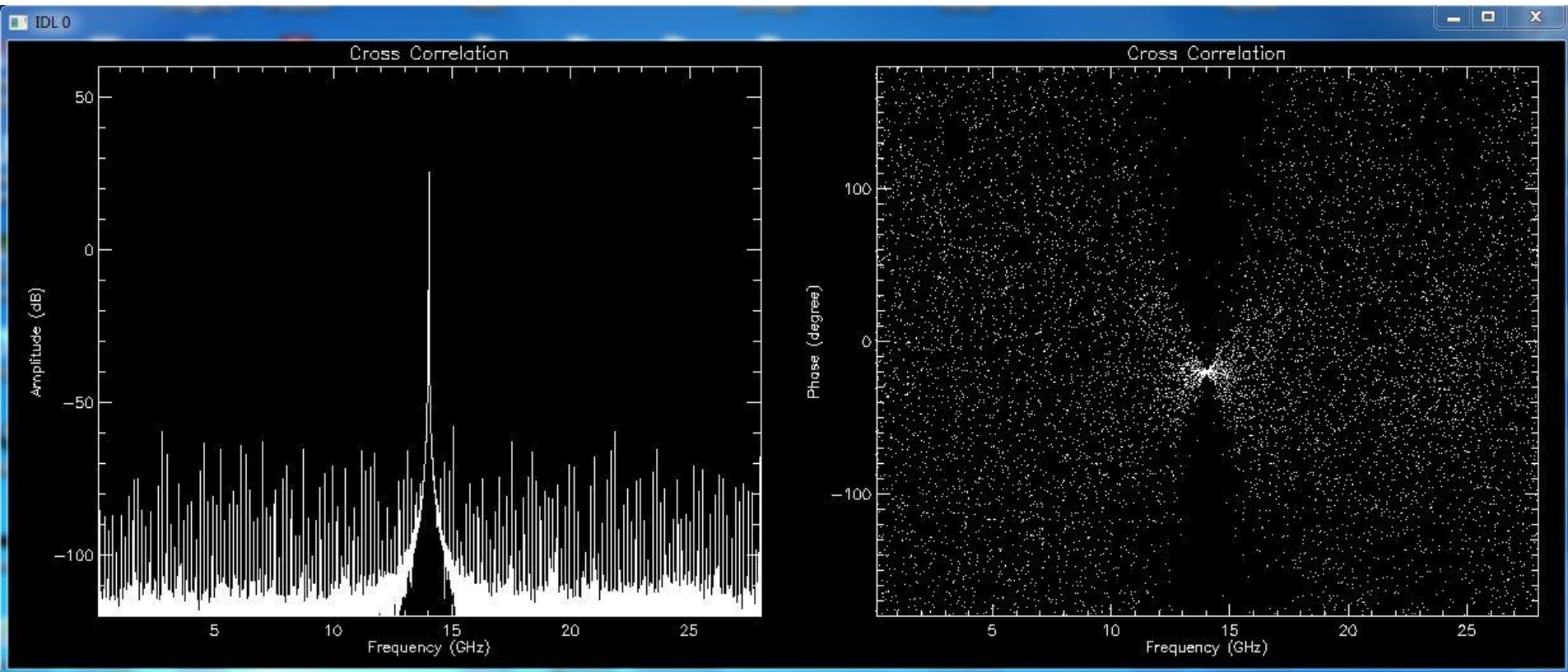
# Some ADB3-H preliminary measurements



# Full 14GHz band cross-correlation



# Single 14GHz tone cross-correlation





**Thank you**