

DBBC3

Multigigabit Backend

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SUMMARY

The DBBC backend is crossing a new phase because an important bandwidth and data rate growth is required

Current state of the art technologies offer the opportunity for a significant improvement in the overall sensitivity and in the delay determination

DBBC3 is the third generation of the DBBC project

DBBC Evolution

DBBC1 2004 - 2008
in: 4 x IF-512MHz
out: **DDC** 16xbbc(1-2-4-8-16MHz)@32MHz
1.024Gbps

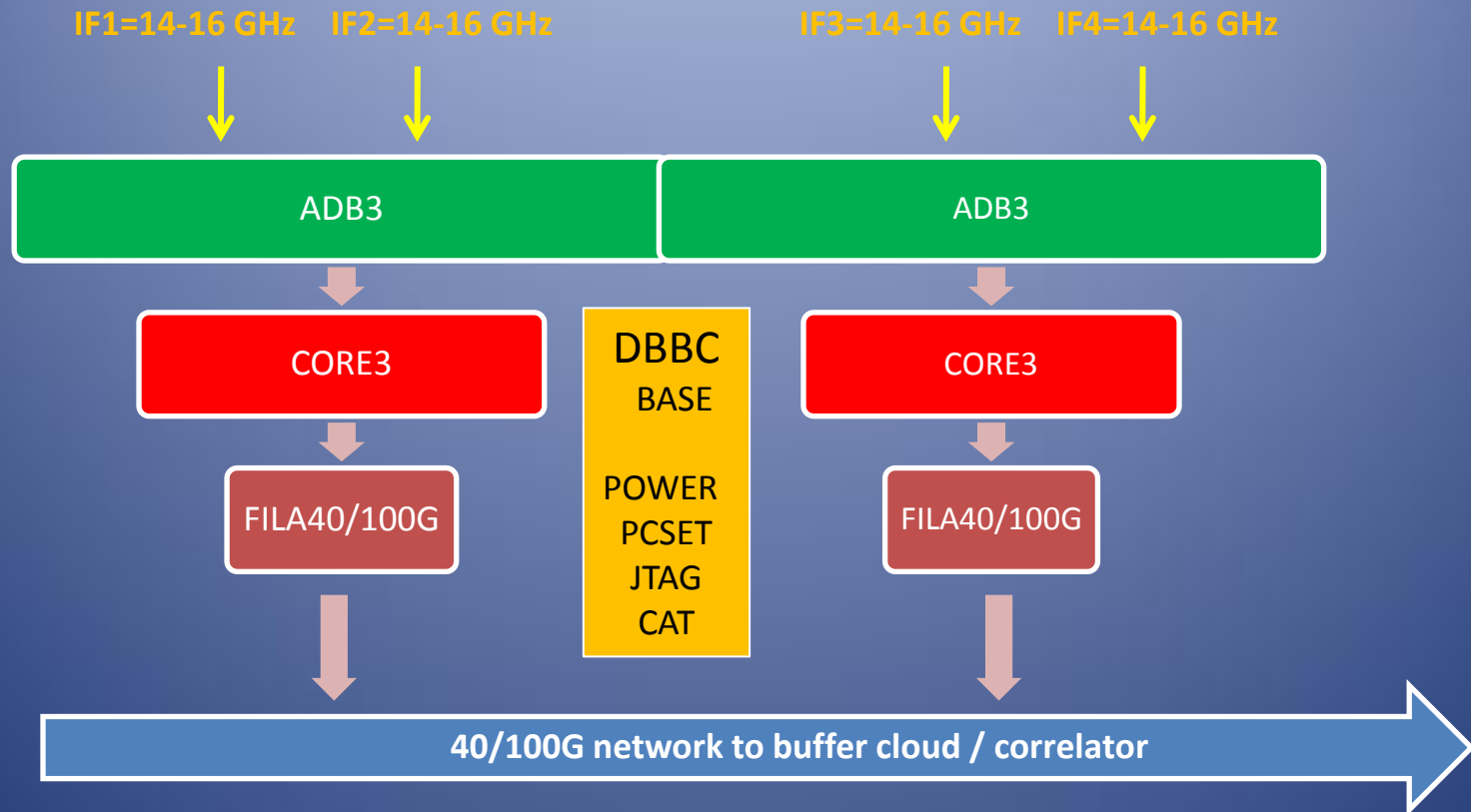
DBBC2 2007 - 2011
in: 4 x IF-1024MHz
out: **DDC** 16xbbc(1-2-4-8-16MHz)@32MHz
PFB 4 x 16 x 32MHz@64MHz
8.192Gbps = 4 x 2048Mbps

DBBC2010 2009 -
in: 8 x IF – 512/1024MHz
out: **PFB** 8 x 16 x 32MHz@64MHz
16.384Gbps = 8 x 2048Mbps

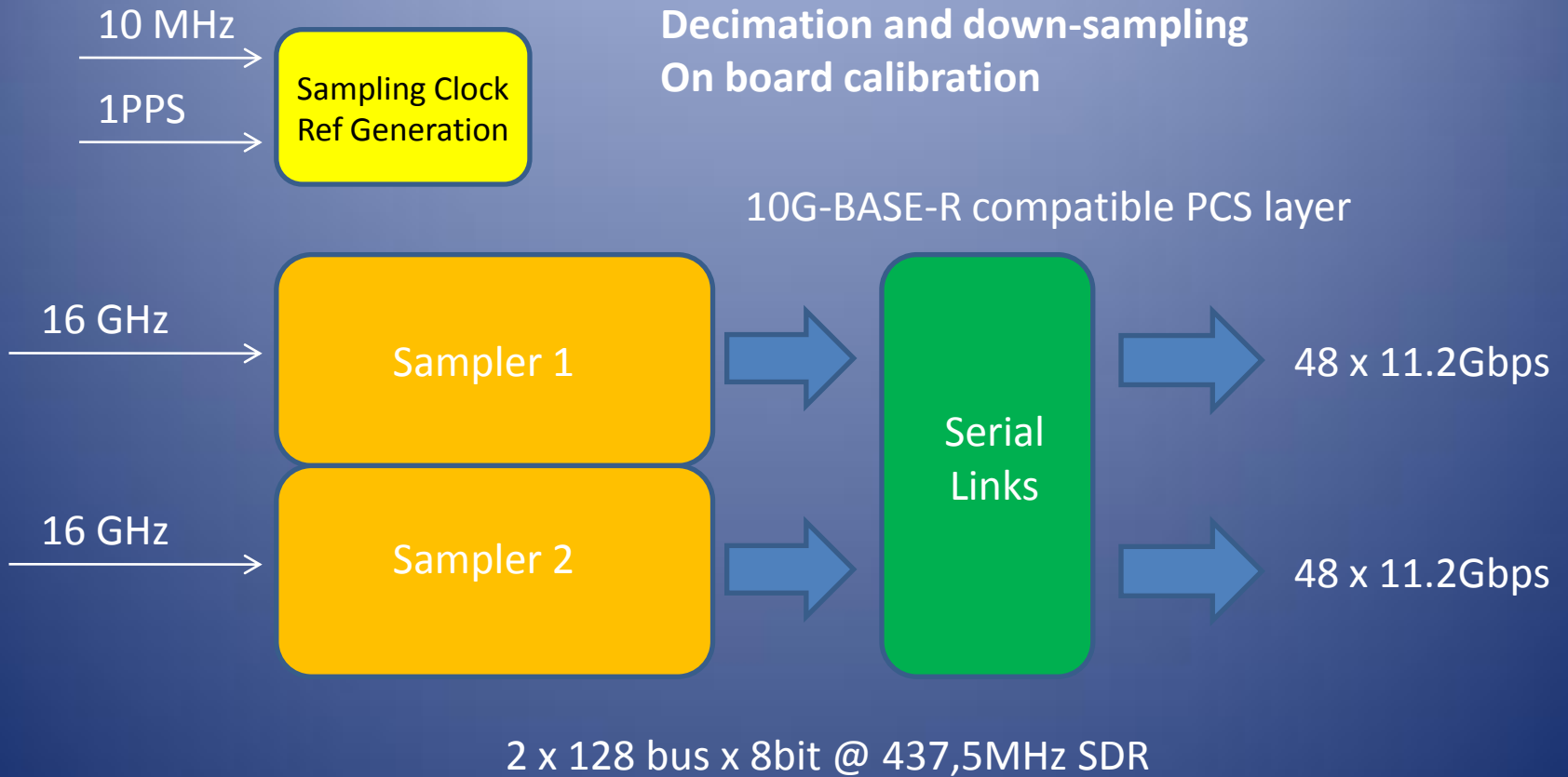
DBBC3 performance

- Number of Input IF: **4**
- Instantaneous bandwidth each IF: **14 - 16 GHz**
- Sampling representation: **8 bit**
- Processing capability **2 x 5 TMACS**
(multiplication-accumulation per second)
- Output: **max 896 Gbps**
- Compatibility with existing DBBC environment

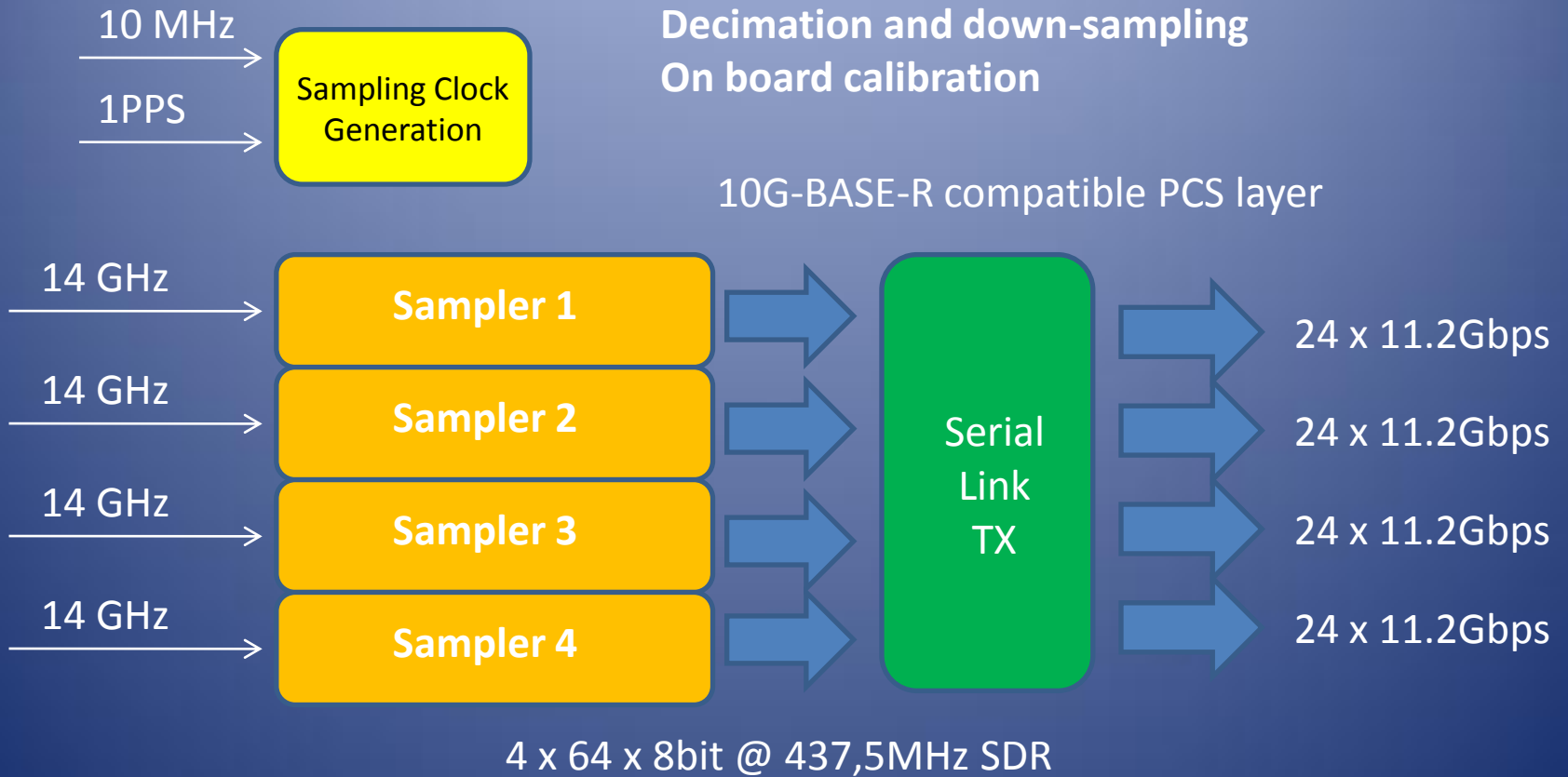
DBBC3 Architecture



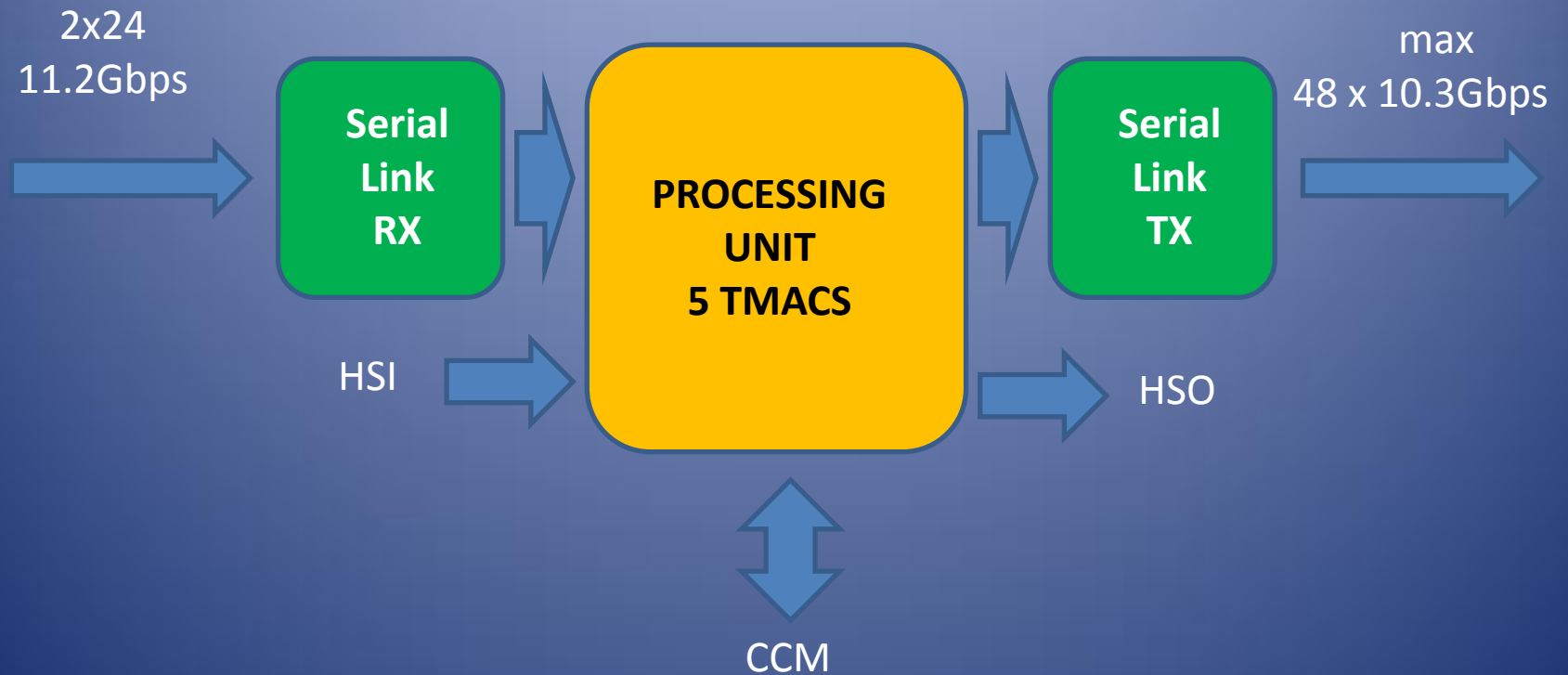
ADB3 mode A



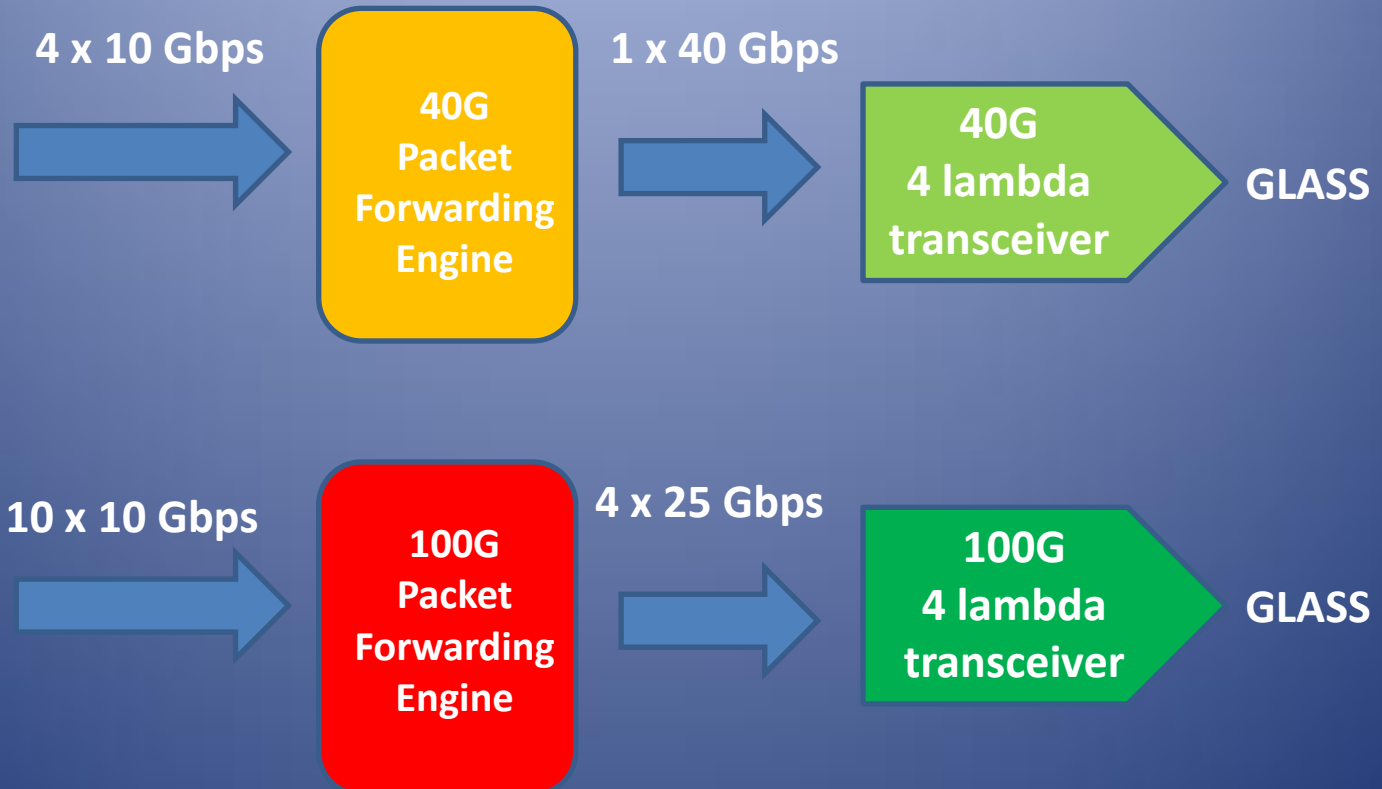
ADB3 mode B



CORE3



FILA40/100G



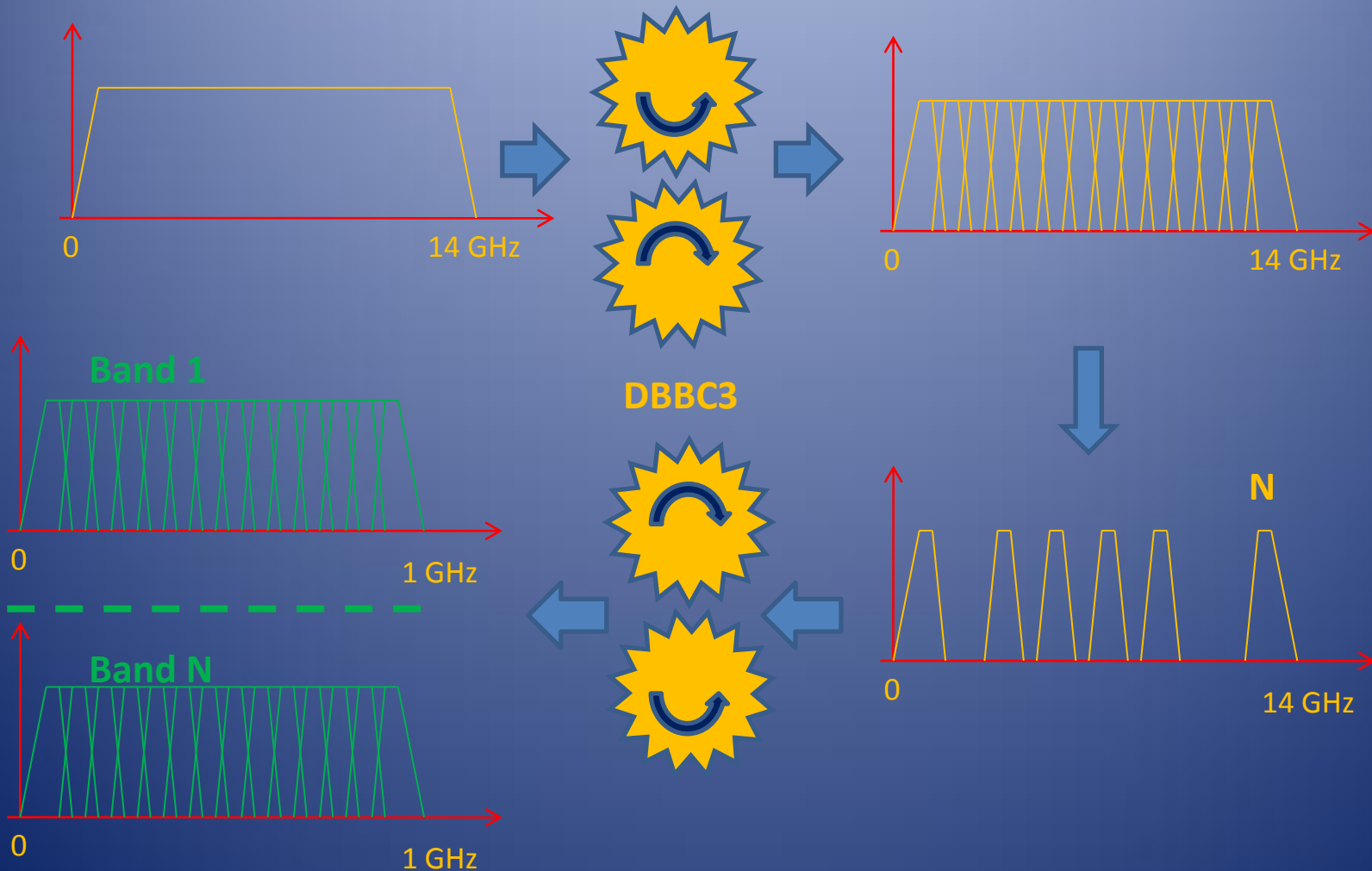
What could we do with it?

VLBI2010 Full Band Digital Direct Conversion

- Direct Input of 4 linear polarization 14 GHz bwd
- Front-end Digital Band Conversion from 14 GHz to 14 x 1 GHz or 28 x 512 MHz
- Intermediate band selection for band synthesis
- Final base-band formation $N \times 15 \times 32\text{MHz}$

VLBI2010 Full Band Digital Direct Conversion

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Status and Development Time

- Funding Proposal to Radionet, developing time depends on its success
- ADB3 project underway: rough prototype for first evaluation expected in May11
- CORE3 : evolution of a previous project, basic firmware for simulation in development
- FILA40/100G: analysis of commercial devices on the market

Development Team

- INAF IRA and Arcetri Obs.
- MPIfR - Bonn
- Onsala Obs.

THANK YOU – Questions?