DBBC2 Backend: Status and Development Plan

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Abstract

The DBBC2 system is in a mature phase now and the deployment is continuing. A review of the backend is shown and the new functionalities in development are reported.

1. Hardware

The DBBC2 hardware system is composed with a class of boards able to support different platforms and so different system configurations. In the VLBI backend implementation two observing types are mainly required: tunable configuration and fixed contiguous bands. The first is adopted to emulate the present MK4 terminal and is required for both geodetic and astronomical observing modes. The second is devoted for astronomical millimeter observations and the new coming VLBI2010 geodetic modes. Both modes are required in the same terminal to be used depending on the observation to be performed, so some efforts have been put to accomplish such modes in a unique hardware architecture.

The interface between the receivers and the backend is included in the DBBC2, and is based on the Conditioning Module, where is possible to select the Nyquist band where to operate and total power measurements are possible. An automatic gain control is able to regulate the signal levels to be transferred to the analog to digital conversion ADB boards. Two types of such sampling elements are available with an instantaneous band for VLBI of 512 or 1024 MHz. Additional possibilities are available up to an instantaneous 2048 MHz, described in this paper at the new hardware development section.

The ADB1 board operates with a sampling 1024 MHz clock, for converting an input signal in the range 10 - 2200 MHz, while the ADB2 is operated at 2048 MHz with an input signal up to 3500 MHz. The ADB2 is able to operate in ADB1 mode and moreover can adopt as piggyback a FILA10G board, to transfer pure sampled data using optical fibers with a 10G Ethernet connection. The ADB2 board was widely tested and is available to be inserted in the standard DBBC2 stack.

The processing unit Core2 board is also full operative and represents the element adopted to generate the down-converted channels in both modes: tunable and fixed tuning. The board is compatible with ADB1 and ADB2 and support a minimal equivalent of four Core1 functionality. The pcb has a number of 40 equivalent layers and all the connections for signal transfer are differential, twisted, matched in delay and impedance between the pads of the dice and the pins of the bus connectors. A piggy-back element can be adopted for additional functionalities.

One Core2 board is able to emulate the complete functionality of four analogue bbcs, or to generate a fixed tuning version of fifteen 32 MHz wide baseband channels, covering an input 512 MHz receiver band.

The CaT2 board (Clock and Timing) is able to generate a highly flexible number of synthesized sampling clock (ex. 2048 MHz, 1024 MHz, etc.) values, phase locked with an external 10 MHz. Low phase-noise and very small sensitivity to temperature are the main performance. The board is also producing 1PPS synchronization signals for all the ADB boards and the entire digital chain. Frequency selection is performed with the use of the DBBC2 internal PC Set.

The FiLa10G can be used as piggy-back board of any ADB2 sampler, giving the possibility to transmit and receive in the same time a high data rate of 20 Gbps + 20 Gbps. The bidirectional functionality could be required for instance when a RFI mitigation is needed to be realized in a remote position with respect to the sampling and processing site. With the typical sampling frequency of 2.048 MHz and the full 10-bit data representation, a double optical fiber set meets the full data handling requirement. Moreover the board is equipped with two additional transceiver able to operate at 1-2-4 Gbps for slower connections.

2. Firmware

The DBBC2 VHDL firmware was completely rewritten in a platform independent fashion. This was accomplished with a great simplification that produced a very compact and efficient code. Performance improvement guarantees a bit by bit identical output from a set of bbcs belonging to the same Core2 board, having of course the same tuning settings and input data. Still some debug is under way to check the entire new code.

The fixed tuned (FT) configuration firmware is also available: it produces a set of 16 (15 usable) contiguous 32 MHz bands from a 512 MHz input range, in any of the Nyquist zones available from the ADB1/2 boards. This configuration is available for the VLBI2010 mode or for the millimetric VLBI network.

Firmware under development is covering the following tasks: a) fully tunable 1 GHz input bandwidth, b) fully tunable 2 GHz input bandwidth, c) 1 GHz FT with 31 channels 32 MHz bwd, d) 2 GHz FT with 63 channels 32 MHz bwd.

Additional firmware configurations are under development, including a multichannel spectrometer, the linear-to-circular (L2C) polarization digital conversion, a polarimeter. In particular the L2C configuration was fully simulated and proved efficient. Now it is expected the adequate processing board (Core3, see in the new hardware development section) for taking care of the necessary processing capability.

3. New Hardware Development

New hardware parts to be integrated in the system are under development. This covers the interfacing, input bandwidth and processing capability.

The FILA10G board is the interface between the system and the MK5C recorder or the network. Main connections are 2 optical fibers operating each at a maximum rate of 10 Gbps. In VLBI standard this is limited by 8.192 Gbps, and for the present recording capability the limitation is 4 Gbps. Data rate is fully bidirectional and compliant with the standard Ethernet networks, under UDP protocol. At present the development status sees the hardware defined and available with some prototypes, and the firmware development at a good stage: VLBI VDIF and MK5B modes are under completion. Some communication experiments have been done with a MK5C recorder.

The 10G network FILA10G board is adopting optical fibers. In order to be connected with one or two MK5C recorders, that adopt copper CX4 standard, needs to be interfaced with a commercial 10G switch having both types of ports. As alternative was developed a bi-directional interface that can be used for such purpose. It's named GLAPPER to recall its functionality to be a transit between GLAss and coPPER.

In order to increase the instantaneous input bandwidth the ADB3 Module has been defined. It is able to support 2048 MHz input bandwidth with a 2.048 GHz sampling clock. Nyquist input bands possible are 10-2048 MHz and 2048-3500 MHz. The main use for such module is with a fixed tuned bands configuration for a significant sensitivity improvement. Prototypes of the ADB3 Module are available and fully debugged.

The Core3 board is an evolution of the present Core2 processing board. It is mainly devoted to very high demanding processing capabilities. It is planned to be used as digital preprocessor for L2C polarization conversion, for VLBI2010 FT configurations with 1 or 2 GHz input bandwidth, and in applications like a very high number of channels spectrometer. The hardware has been fully defined and the boards are expected before the end of 2010. Firmware applications are already simulated and ready to be debugged in the real board.

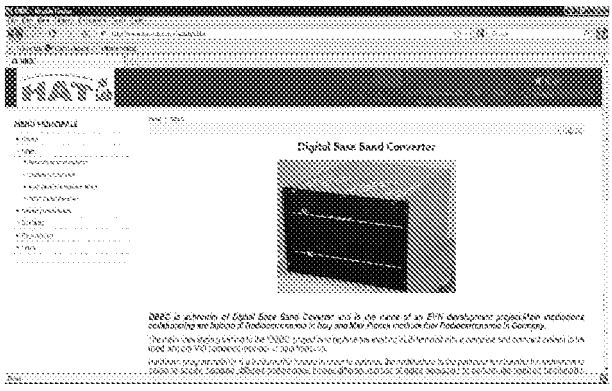

Figure 1. HAT-Lab web site.

4. HAT-Lab

HAT-Lab is a spin-off company supported by INAF for the DBBC production. The company has agreements with IRA-Noto, where laboratories are placed for a part of the production, and MPI in Bonn where other phases of the production are realized. A certain number of operations are realized by external specialized companies to simplify and optimize the production of the complex boards. Assembly and testing is fully realized in HAT-LAb, IRA and MPI.

At present eight systems have been deployed by IRA and now HAT-Lab is going to deliver eight additional systems. In the second part of the year are expected to be produced the same number of units. Production capability of HAT-Lab is around 12 systems per year, and production time is close to 6 months.