# DBBC - A Flexible Platform for VLBI Data Process

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**Abstract**

The development of the first version of DBBC is complete and an extended testing phase is expected in 2006. The instrument is a flexible environment where today a complete analog VLBI pre-recording terminal is realized in digital technology, but having the chance to process data in a different fashion for multiple narrow or fewer very wide band channels without changing any hardware part. A description of this instrument is shown, reporting on the performance with the present implementation, and pointing out the potentiality for a different implementation within the same hardware. Moreover a description of the second version is given with some details on new hardware parts for additional functionalities, such as RFI mitigation, AD sampling in the receiver site.

## 1. Introduction and general description

The main idea staying behind to the 'DBBC' project is to replace the existing VLBI terminal with a complete and compact system to be used with any VSI compliant recorder or data transport. Moreover the cost has to be limited making use of commercially available components. Hardware programmability is a fundamental feature in order to optimize the architecture to the particular functionality the instrument is called to satisfy, because different performance involve different number of gates necessary to perform the required functionality. Under this assumptions, maximum input and output data rates are the limitation and they have to be set so to satisfy the present and reasonable future necessities.

The new development needs to be fully compatible with the existing terminals and correlators in order to require a minimum effort to be introduced in the stations and no modification at the correlator side, still maintaining the possibility to be upgraded for a new class of correlators. The possible upgrades have to be mostly software in order to avoid and modify any hardware part, for cost savings and simplification in the operations, so that programmable hardware is the main component. Anyway hardware upgrade is still possible because a standard in the connection of the different elements is defined.

The entire project is based on a flexible architecture, composed by one or more FPGA boards as computation elements, placed in a mixed cascaded/parallel structure, so to guarantee a parallel usage of data input and a shared parallel output data flow.

In a DBBC a single system unit is composed by four RF/IF Input in the ranges 0.01-512, 512-1024, 1024-1536, 1536-2048 MHz, 2048-2100 MHz with each of them feeding a 1.074 GHz clock sampler. Then four polarizations or bands are available for a single group of output channels selection. A group of 64 channels is able to handle a shared combination of channels coming from the four

bands, supporting two VSI output connectors as output.
Multiple architecture can be used taking the advantage to adopt fully re-configurable FPGA CoreModules, where one of such modules is an autonomous board populated with an appropriate number of gates, fed by any of the four IFs, and sharing the output data bus. Narrow or wide bandwidth channels per module can be assigned, maintaining the maximum number of gates provided by the CoreModule. Modular realization for a stack processing is provided, that implies the use of one or more Core Modules for achieving more gates number and then more processing capability. The input bus is cascaded, with very low skew, between modules. An analog monitor, produced by DA conversion, has been added for testing purposes, in order to be able and evaluate with a common spectrum analyzer the different channels content and performance. This has been proved particularly useful in order to adopt standard equipment normally in use in a radiotelescope. Field System support is required to configure the different modules and allow standard settings, and still getting total power measurements of the converted channel. A limited effort should be assured in the FS side to include the support for the DBBC due to the implicit FS-like structure of the commands the DBBC is able to recognize.
Different configurations can be supported for obtain similar, but not identical, functionalities, as SSB down converter, wide band parallel FIR, poly-phase FIR/FFT, and still more. The possibility to independently tune different channels, and to have them filtered at different bandwidth, while it is an obvious feature in the analog implementation, it is not the unique so obvious solution in the digital implementation, so that different solutions could appear to be more convenient. For this reason the project allows to implement different architectures, and to change them at convenience. A Core Module can handle a maximum input bandwidth of more than 34 Gbit/s, and a maximum output bandwidth of 8.192 Gbit/s. Two high rate bus are present, named HSI and HSO respectively, with the addition of a further Control/Configuration/Monitor bus, named CCM.

## 2. System Components

In the figure 1 the DBBC is shown, while a schematic view of the instrument is visible in figure 2. Signals coming from the receivers trough the ConditioningModule are kept at the proper level before the sampling process.

The ADBoard (figure 3) perform the analog to digital conversion at a rate of $2^{30}$ Hz. Four of these units are able to feed four IFs with 8-bit representation in the processing units, the CoreModule boards (figure 4). The maximum number of such FPGA boards is 16 in a stack configuration. The FiLa board, whose meaning is First/Last, (figure 5) open and close the chain. Such board is indeed used in the initial and final part of the stack to perform more functions: 2 VSI interfaces, DA monitor, Timing synchronization and Clock Synthesizer, Communication, JTAG channel.

The FPGAs Core Configuration represent the firmware to perform the desired functionality, such as the SSB base band conversion. Different architectures can be used because of the full programmability of the module.

The PowerDistributor board is generating the supply voltages for each board of the chain. The software, able to manage the entire functionality of the DBBC is run on a compact PC board with the help of two PCI commercial interfaces. System Management Software is Field System oriented, so that standard commands to set and use the instrument are FieldSystem-like, requiring than a minimum effort to integrate the DBBC in that environment.

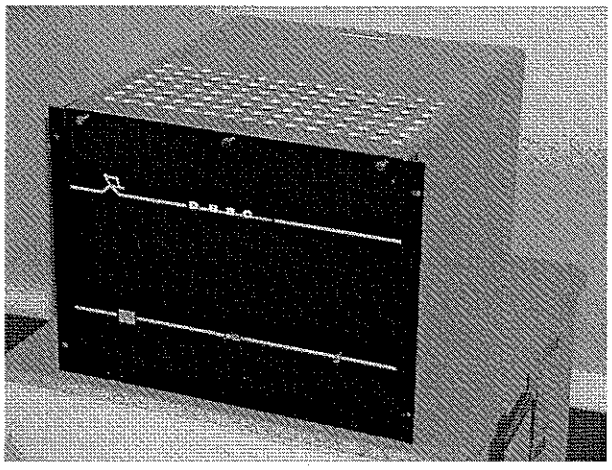

Figure 1. DBBC Back-end System.

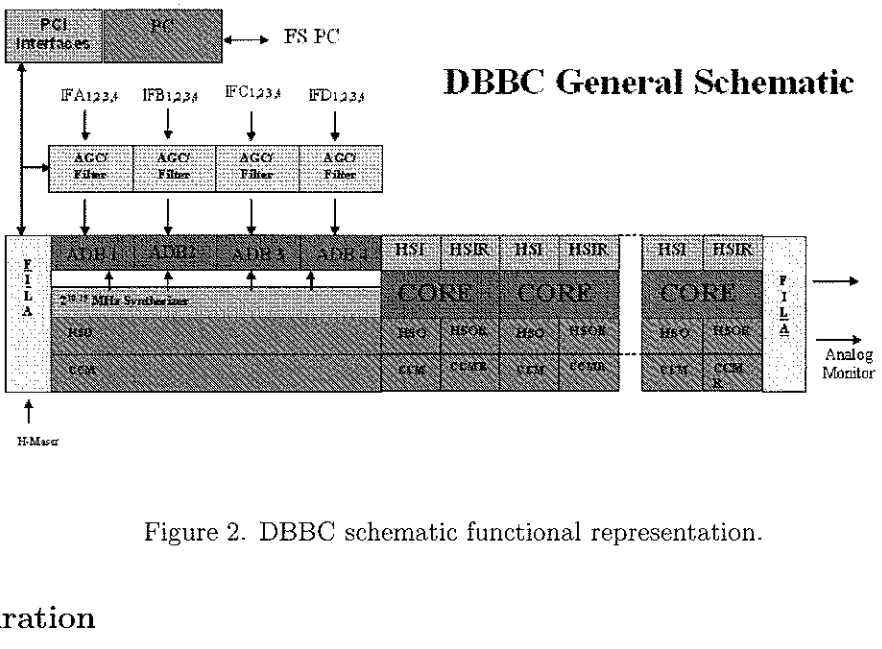


Figure 2. DBBC schematic functional representation.

## 3. Configuration

Different architectures can be used in the Core Modules, having different performance and behaviors. One possible configuration is the DDC digital down converter in the classical implementation meaning. In such a solution a direct SSB conversion is typically performed between high data rate sampled IF band and lower data rate base band. One or two channels are generated for each converter, as in the analog implementation. Important differences, greatly improving the performance are present: local oscillator is a Numerically Controlled Oscillator (NCO), mixer is complex as Look Up Table multiplier, low-pass band filters are Finite Impulse Response (FIR). Decimation circuitry is adopted because of the high ratio between IF and output data rate and is performed with multirate/multistage FIR. Digital Total Power (DTP) measurement at base band level is adopted; Rescaling/Gain Control (RGC) is adopted for dynamic range control and final data representation. The tuning step is 1 Hz, giving the possibility to finely tune the receiver

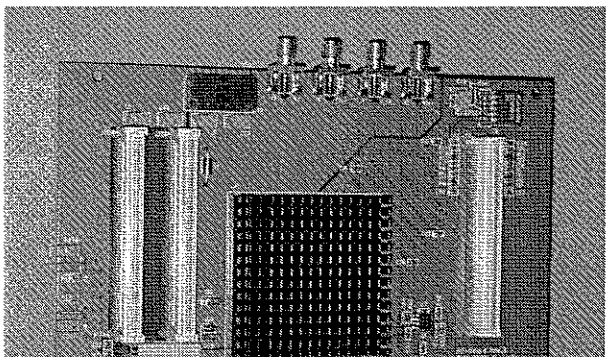

Figure 3. ADBoard - Sampler board 8-bit at $2^{30}$ Hz clock frequency.

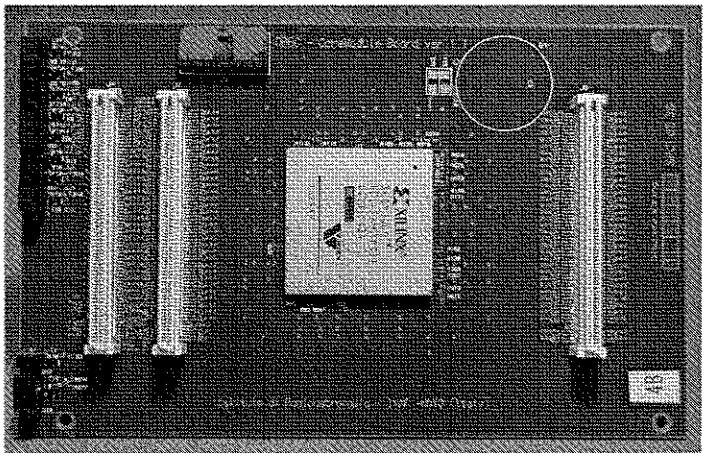

Figure 4. CoreModule Board is the processing element, with three high data rate I/O bus.

for spectroscopy or any other precise frequency settings. Narrow bandwidth typically adopted is defined for this project in the range: 16, 8, 4, 2, 1, 0.5, 0.25 MHz. Output data rate is 32 or 64 MHz at present in order to be able and fit with the standard, now adopted VSI-H data rate. A 128 MHz clock rate is the maximum supported.

## 4. Upgrade

Testing with real observation started with mDBBC (IRA-SHAO agreement): fringes have been detected in both analog-digital and digital-digital baselines. First digital x analog fringes have been detected on Nov 23, 2004 in the Seshan-Urumuqi baseline, while first digital x digital fringes on Feb 2, 2005 in the Noto-Seshan baseline.

The 2006 will be dedicated to an observations/optimization process. Moreover an update program for improving performance is under way. It includes: FPGA Virtex4 device testing for

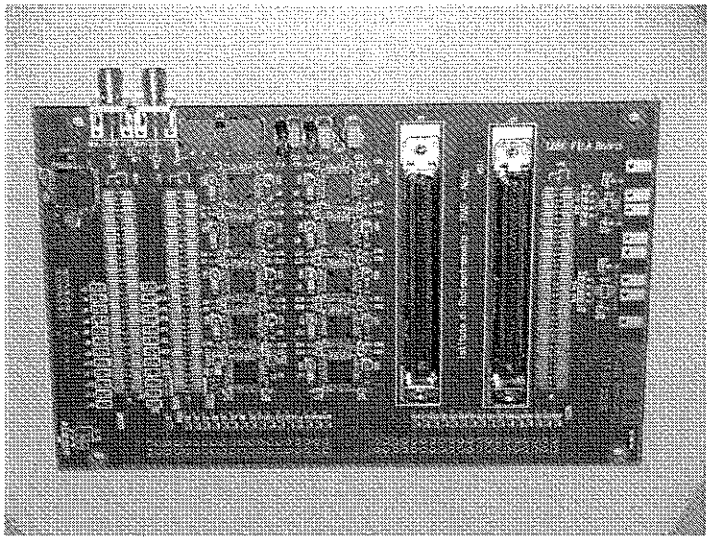

Figure 5. FiLa Board - Support two VSI interfaces, DA converter, PC communication, JTAG programming.

double processing clock and price reduction, Faster AD sampler for input bandwidth increasing, AD sampler placed inside the receiver and sampled data sent through an optical fiber, RFI Mitigation Board: the first CoreModule (same hardware) acts as RFI processor in transfer the pure sampled data with proper configuration.

## 5. Conclusions

The DBBC system is an high flexible instrument because is able to produce independent tunable channels for a full compatibility with the existing acquisition system and correlators. One CoreModule board is replacing a BBC module. Combination of up to 4/16 IFs in a single module is possible. The DBBC system is able to handle also equi-spaced multichannel configuration for producing contiguous not tunable channels. One CoreModule board is able to produce multiple channels. More solutions are possible within the same system with software selection. A minimal architecture is composed by 1 ADBoard, 1 CoreModule (multichannel configuration, or any other), 1 FiLa board (VSI interface, DA converter, etc). A maximal architecture in one system is composed by 4 Conditioning Modules, 1 FiLa board, 4 ADBoard, 16 CoreModule, 1 FiLa board, PC and PCI interfaces. Such wide range of hardware and software conditions allow to assemble a low cost system with the needed performance.

## References

[1] G. Tuccari, Development of a Digital Base Band Converter (DBBC): Basic Elements and Preliminary Results In: New Technologies in VLBI, Astronomical Society of the Pacific Conference Series, Vol. 306, p.177-192, 2004.