DBBC Development: Status and First Results

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Abstract

It is reported a description of the DBBC project, having the aim to realize a fully digital backend system to replace the presently used terminals. The need for such replacement is well known and motivated by the necessity to renew an obsolete system and for achieving better performance making use of the more predictable digital techniques. Field Programmable Gate Array (FPGA) components give the opportunity to take advantages within a concept of a fully programmable system, with the possibility to get a variable architecture and to pursuit an upgrading methodology. The DBBC development is in a well advanced stage and a simplified version, named miniDBBC, coming as collaboration between Italy and China, produced the first experimental results in real observations. Indeed two prototypes have been placed in the Noto (Italy) and Seshan (China) VLBI stations, while two complete systems are in construction.

1. Project Overview

The main idea staying behind to this project is to replace the existing terminal with a complete and compact system to be used with any VSI compliant recorder or data transport. Moreover the cost has to be limited making use of commercially available components.
Hardware programmability is a feature in order to optimize the architecture to the needed performance, because different performance involve different number of gates necessary to perform the required functionality. Under this assumptions, maximum input and output data rates are the limitation and they have to be set so to satisfy the present and reasonable future necessities.
The new development needs to be fully compatible with the existing terminals and correlators in order to require a minimum effort to be introduced in the stations and no modification at the correlator side, still maintaining the possibility to be upgraded for wider bands correlators. The upgrades on the other hand have to be mostly software in order to avoid and modify any hardware part, for cost savings and simplification in the operations, so that programmable hardware is planned as main component.
The entire project is based on a flexible architecture, composed by one or more FPGA boards as computation elements, placed in a mixed cascaded/parallel structure, so to guarantee a parallel usage of data input and a shared parallel output data flow. For such a reason the upgrade could also in principle be possible in hardware replacing or adding compatible modules for different or modified performance, even if this is strongly limited by the software programmability.
In the DBBC project a single unit is composed by four IF Input in the ranges 1-512, 512-1024, 1024-1536, 1536-2048 MHz, with each of them feeding a 1.074 GHz clock sampler. Then four

polarizations or bands are available for a single group of output channels selection. In other words, a group of 64 channels is able to handle a shared combination of channels coming from the four bands.
Multiple architecture can be used taking the advantage to adopt fully re-configurable FPGA Core-Modules, where one of such modules is an autonomous board populated with an appropriate number of gates, fed by any of the four IFs, and sharing the output data bus. More narrow or few wide channels per module can be assigned, maintaining the maximum number of gates provided by the CoreModule. Modular realization for possible cascaded processing is provided, that implies the use of one or more Core Modules for achieving more gates number and then more processing capability. The input bus is cascaded, with very low skew, between modules.
An analog monitor, produced by DA conversion, has been added for testing purposes, in order to be able and evaluate with a common spectrum analyzer the different channels content and performance. This has been proved particularly useful in order to adopt standard equipment normally in use in our radio-telescopes.
Field System support is required to configure the different modules and allow standard settings, and still getting total power measurements of the converted channel. Different configurations can be supported for obtain similar, but not identical, functionalities, as SSB down converter, wide band parallel FIR, poly-phase FIR/FFT. The possibility to independently tune different channels, and to have them filtered at different bandwidth, while it is an obvious feature in the analog implementation, it is not the unique so obvious solution in the digital implementation, so that different solutions appear to be more convenient. For this reason the project allows to implement different architectures, and to change them at convenience.
A Core Module can handle a maximum input bandwidth of 8.192 Gbit/s, apart from the IFs cascade (more than 34 Gbit/s), and a maximum output bandwidth of 4.096 Gbit/s. Two high rate buses are are present, named HSI and HSO respectively, with the addition of a further Control/Configuration/Monitor bus, named CCM.

2. Digital Down Converter Configuration

Different architectures can be used in the Core Modules, having different performance and behaviors. One possible configuration is the DDC digital down converter in the classical implementation meaning. In such a solution a direct SSB conversion is typically performed between high data rate sampled IF band and lower data rate base band. One or two channels are generated for each converter, as in the analog implementation. Important differences, greatly improving the performance are anyway present: local oscillator is a Numerically Controlled Oscillator (NCO), mixer is complex as Look Up Table multiplier, low-pass band filters are Finite Impulse Response (FIR). Decimation circuitry is adopted because of the high ratio between IF and output data rate and is performed with multirate/multistage FIR. Digital Total Power (DTP) measurement at base band level is adopted, Rescaling/Gain Control (RGC) is adopted for dynamic range control and final data representation. The tuning step is 1 Hz, giving the possibility to finely tune the receiver for spectroscopy or any other precise frequency setting. Moreover a full compatibility with the 10 KHz tuning step of the present backend is assured. Narrow bandwidth typically adopted is defined for this project in the range: 16, 8, 4, 2, 1, 0.5, 0.25 MHz. Output data rate is 32 or 64 MHz at present in order to be able and fit with the standard, now adopted VSI-H data rate.

3. Development Status

Most of the bandwidth configurations have been completed or are under completion. The tuning ranges are now ready as 64 and 128 MHz, while 256 and 512 MHz are ready in simulation and are under implementation.
Preliminary testing has been done in laboratory for the developed configurations. Good performance in conversion and tuning have been measured from 0 up to 2.5 GHz. Today with appropriate Nyquist zone pre-selection, L and S band can be directly down-converted and recorded with modified MK4 formatter.
Testing with real observation started with mDBBC (IRA-SHAO agreement): fringes have been detected in both analog-digital and digital-digital baselines. First digital x analog fringes have been detected on Nov 23, 2004 in the Seshan-Urumuqi baseline, while first digital x digital fringes have been detected on Feb 2, 2005 in the Noto-Seshan baseline.
An upgrade in the critical system components is planned, leaving the structure as it is described in this document, including boards layout. In particular, an experience is going to be acquired before introducing the modification, making use of a different AD chip with 10 bit resolution, LVDS differential output, increased max sampling rate, and a Virtex4 FPGA device. Main improvement are expected due to the increment of the internal system clock from 128 MHz to 256 MHz and to the optimized resources and internal routing performance available with the last generation FPGA Xilinx family. Further element will be to make use of the higher Nyquist sampling zone to directly down-convert from sky frequency with bands where this could be applied.
In conclusion the DBBC system is an high flexible instrument because is able to produce independent tunable channels for a full compatibility with the existing acquisition system and correlators. One CoreModule board is replacing a BBC module. The DBBC system is also able to handle polyphase + FFT architectures for producing contiguous not tunable channels. One CoreModule board is able to produce multiple channels. Both solutions are possible within the same system.

References

[1] Tuccari, G. Development of a Digital base Band Converter (DBBC): Basic Elements and Preliminary Results. "New Technologies in VLBI", ASP Conference Series, Vol. 306, 2003, ed. Y. C. Minh (San Francisco: ASP), pp. 177-192

[2] Ferris, D. Digital Filters and Filterbanks for VLBI. Presented at the Symposium of the International VLBI Service for Geodesy and Astrometry "New Technologies in VLBI", held in Gyeong-ju, Korea, 5-8 November 2002

[3] G. Tuccari, "DBBC-A Wide Band Digital Base Band Converter", IVS Third General Meeting Proceedings, Canada, 2004