DBBC - Wideband Digital Base Band Converter System

AD Environment

Ver.1.0

G. Tuccari

EVN Doc n. 116/2004

The AD section represents the transition point where the domain representation of the signals change, and then all the further processes needs to be done with a very different method. As it's well understood to get a fully digital backend means to anticipate in the signal process such transition that now represents the initial step.
Some preprocessing is anyway necessary to adapt the wideband noise coming from a radioastronomical receiver to an analog to digital converter, such as the level control and band-pass limitation.
A commercial available AD converter that has been widely tested is the MAX108, operating at 8-bit. This has been chosen as base for the DBBC project even if during the development whether better solutions will be found, without implications on the rest of the project, a modification could be applied. This device produce a differential output in LVPECL in one or two 8-bit bus, depending on the sampling frequency. Indeed up to a maximum of 750 MHz a single bus can be used, while in excess of this two bus are an appropriate solution.
The DBBC project plan to use a single sampling frequency at 1024 MHz, so to have an output clock of 512 MHz with data demultiplexed on two bus. This output rate is still pretty high for the Xilinx Virtex2 family, where operating at 128 MHz is safe, so that an appropriate further demultiplexing stage is necessary. Such unit is described in a different document.
For a comparison with the VLBA terminal we will consider the signal coming from a receiver with power levels of about - 30dBm/500 MHz and the project of the signal adapting to the AD element will be done accordingly with such levels.

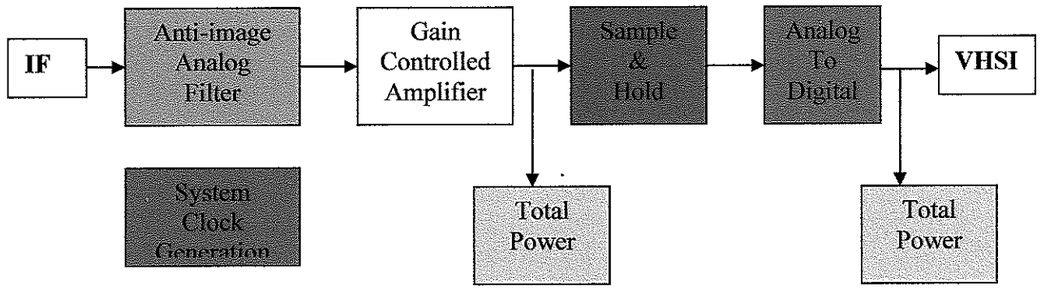


Fig.1

A general schematic view is represented in fig.1 while in the fig.2 a more detailed version is showed.
The schematic drawing reports a view of the unit preceding the sampling stage. Main elements are an initial switch able to insert the received signal or to close the input on a load so to allow the zero levels measurement. An amplifier follows and then the filter selection through a splitter, two filters operating in the range 10 - 512 MHz or 512 - 1024 MHz, a switch. A second amplification stage is then in front of a programmable attenuator operating in the range 0-31.5 dB with 0.5 dB step. Signal is then divided to feed the AD input and the total power measurement stage.
This schematic is a possible implementation of this section and it should represent a starting point. Additional care should be placed in the AD temperature control in order to take under control the timing drift effect and more in general the timing noise. A possible simple solution could just be to adopt the numerous solutions used for the microprocessor temperature control systems where a wide range of controllers are available driving a fan and controlling the chip temperature.

The output bus is named VHSI and is connected to the Multiplexed board trough a set of coaxial cables, in a bus-like structure.

VHSI: 2x8-bit, differential, @512 MHz

Pin definition for VHSI bus

Pin/Connector#	Meaning
1	P bus, pin 0, polarity +
2	P bus, pin 0, polarity -
3	P bus, pin 1, polarity +
4	P bus, pin 1, polarity -
5	P bus, pin 2, polarity +
6	P bus, pin 2, polarity -
7	P bus, pin 3, polarity +
8	P bus, pin 3, polarity -
9	P bus, pin 4, polarity +
10	P bus, pin 4, polarity -
11	P bus, pin 5, polarity +
12	P bus, pin 5, polarity -
13	P bus, pin 6, polarity +
14	P bus, pin 6, polarity -
15	P bus, pin 7, polarity +
16	P bus, pin 7, polarity -
17	A bus, pin 0, polarity +
18	A bus, pin 0, polarity -
19	A bus, pin 1, polarity +
20	A bus, pin 1, polarity -
21	A bus, pin 2, polarity +
22	A bus, pin 2, polarity -
23	A bus, pin 3, polarity +
24	A bus, pin 3, polarity -
25	A bus, pin 4, polarity +
26	A bus, pin 4, polarity -
27	A bus, pin 5, polarity +
28	A bus, pin 5, polarity -
29	A bus, pin 6, polarity +
30	A bus, pin 6, polarity -
31	A bus, pin 7, polarity +
32	A bus, pin 7, polarity -
33	Data Ready, polarity +
34	Data Ready, polarity -

19-1492; Rev 1; 10/01

EVALUATION KIT AVAILABLE

±5V, 1.5Gsps, 8-Bit ADC with On-Chip 2.2GHz Track/Hold Amplifier

MAX108

General Description

The MAX108 PECL-compatible, 1.5Gsps, 8-bit analog-to-digital converter (ADC) allows accurate digitizing of analog signals with bandwidths to 2.2GHz. Fabricated on Maxim's proprietary advanced GST-2 bipolar process, the MAX108 integrates a high-performance track/hold (T/H) amplifier and a quantizer on a single monolithic die.

The innovative design of the internal T/H, which has an exceptionally wide 2.2GHz full-power input bandwidth, results in high performance (typically 7.5 effective bits) at the Nyquist frequency. A fully differential comparator design and decoding circuitry reduce out-of-sequence code errors (thermometer bubbles or sparkle codes) and provide excellent metastable performance. Unlike other ADCs that can have errors resulting in false full- or zero-scale outputs, the MAX108 limits the error magnitude to 1LSB.

The analog input is designed for either differential or single-ended use with a ±250mV input voltage range. Dual, differential, positive-referenced emitter-coupled logic (PECL)-compatible output data paths ensure easy interfacing and include an 8:16 demultiplexer feature that reduces output data rates to one-half the sampling clock rate. The PECL outputs can be operated from any supply between +3V to +5V for compatibility with +3.3V or +5V referenced systems. Control inputs are provided for interleaving additional MAX108 devices to increase the effective system sampling rate.

The MAX108 is packaged in a 25mm x 25mm, 192-contact Enhanced Super Ball-Grid Array (ESBGA™) and is specified over the commercial (0°C to +70°C) temperature range. For pin-compatible, lower speed versions of the MAX108, see the MAX104 (1Gsps) and the MAX106 (600Msps) data sheets.

Applications

Digital RF/IF Signal Processing
Direct RF Downconversion
High-Speed Data Acquisition
Digital Oscilloscopes
High-Energy Physics
Radar/ECM Systems
ATE Systems

Typical Operating Circuit appears at end of data sheet.

ESBGA is a trademark of Amkor/Anam.

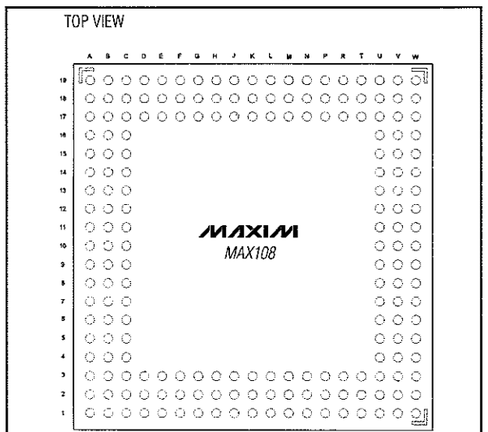
Features

- **1.5Gsps Conversion Rate**
- **2.2GHz Full-Power Analog Input Bandwidth**
- **7.5 Effective Bits at f_{IN} = 750MHz (Nyquist Frequency)**
- **±0.25LSB INL and DNL**
- **50Ω Differential Analog Inputs**
- **±250mV Input Signal Range**
- **On-Chip, +2.5V Precision Bandgap Voltage Reference**
- **Latched, Differential PECL Digital Outputs**
- **Selectable 8:16 Demultiplexer**
- **Internal Demux Reset Input with Reset Output**
- **192-Contact ESBGA Package**
- **Pin Compatible with MAX104 (1Gsps) and MAX106 (600Msps)**

Ordering Information

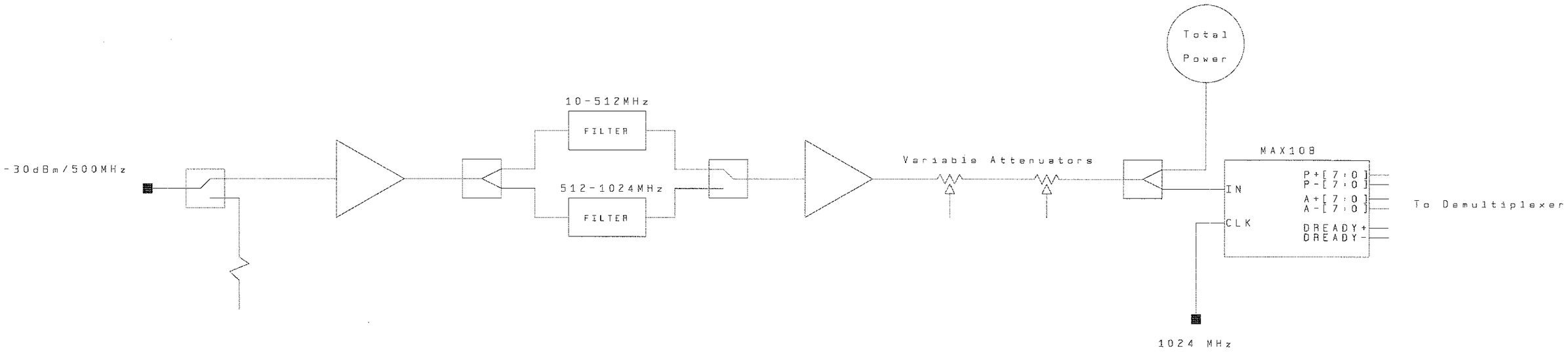
PART	TEMP RANGE	PIN-PACKAGE
MAX108CHC	0°C to +70°C	192 ESBGA

192-Contact ESBGA Ball Assignment Matrix



ESBGA

PCB land pattern appears at end of data sheet.



IRA NOTO

Digital Base Band Converter

IF Control Section

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DRAWN BY: G. Tuccari