DBBC - Wideband Digital Base Band Converter System

CoreModule Board

Ver.1.0

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EVN Doc n. 118/2004

Description

The CoreModule board is the basic element able to produce the digital signal processing in a general fashion. It's composed with a set of FPGA components interconnected in a regular matrix so to be able to handle different architectures. What is stated is mainly the general hardware architecture in terms of I/O and control bus.
The DBBC project requires fast bus for input and output and more in particular requires an input of 8.192 Gbit/s and an output of 4.096 Gbit/s sustained data rate. Such high data rate is supported by two parallel bus, the input one 128 bit wide as 8 demultiplexed by 8-bit LVPECL differential running at 128 MHz, the output one as 128 bit wide LVPECL differential 64 sigle channel at a maximum of 64 MHz clock frequency.
A control bus is able to support the FPGA configuration, so as a dialogue with the internal registers.

Definition for the bus structure and main features:

•HSI Input Bus 8x8bit @128MHz
•HSIR Replicated Input Bus 8x8bit @128MHz
•HSO Shared Output bus 2x32bit @32,64MHz
•HSC Control / Configuration bus 32bit I/O
•HSM Monitor bus 2x12bit @32,64MHz
•HSX Internal data bus 128bit @max128MHz
•Maximum 4 FPGA VirII-1152pin
•'Sandwich' cascade method

A schematic view for the data bus architecture is shown in the figure 1. The HSI bus is connected in parallel to the FPGA chip but only one of them is in charge to replicate, such device is also called as master, or first in the boundary scan configuration chain. A maximum of 4 FPGAs could be allocated in the CoreModule board with the possibility for them to share signals through an interconnected bus, named HSX. The output bus is open-drain-like shared bus with the responsibility to collect from different FPGA processing units, even belonging to different CoreModule boards, signals to be sent to a VSI interface.

A schematic view of a CoreModule assembly structure is shown in figure 2, where it can be seen as the boards are interconnected in a way they can share the same input bus coming from one of the four possible IFs, while different CoreModules operating with different IFs share the same output bus, so to be able to create any combination of channels from more bands or polarizations.

An indicative board layout is shown in fig.3. The central connectors are the HSI, while HSO and HSC and HSM are divided in the edge connectors.

Each of the four FPGA receptacles is able to support a 1152 pin chip, so with the possibility to place XC2V3000-4000-6000-8000 getting a full number of gates per board of 12-16-24-32 Mgates.
A carefull estimation of the needed resources has to be taken into account for optimize the number of CoreModules with respect to the number of gates per board, depending on the cost in the final stage of the project.

Interfacing is realized internally to the single FPGA, with the only exception for the address decoding of each chip that is generating a CS strobe for configuring. RW and data meaning are consistent for configuration. Configuration downloading could be selected between JTAG and parallel mode.

Pin definition for HSI and HSIR bus connector 1

Pin#	Meaning
1	A bus, pin 0, polarity +
2	A bus, pin 0, polarity -
3	A bus, pin 1, polarity +
4	A bus, pin 1, polarity -
5	A bus, pin 2, polarity +
6	A bus, pin 2, polarity -
7	A bus, pin 3, polarity +
8	A bus, pin 3, polarity -
9	A bus, pin 4, polarity +
10	A bus, pin 4, polarity -
11	A bus, pin 5, polarity +
12	A bus, pin 5, polarity -
13	A bus, pin 6, polarity +
14	A bus, pin 6, polarity -
15	A bus, pin 7, polarity +
16	A bus, pin 7, polarity -
17	B bus, pin 0, polarity +
18	B bus, pin 0, polarity -
19	B bus, pin 1, polarity +
20	B bus, pin 1, polarity -
21	B bus, pin 2, polarity +
22	B bus, pin 2, polarity -
23	B bus, pin 3, polarity +
24	B bus, pin 3, polarity -
25	B bus, pin 4, polarity +
26	B bus, pin 4, polarity -
27	B bus, pin 5, polarity +
28	B bus, pin 5, polarity -
29	B bus, pin 6, polarity +
30	B bus, pin 6, polarity -
31	B bus, pin 7, polarity +
32	B bus, pin 7, polarity -

Pin#	Meaning
33	C bus, pin 0, polarity +
34	C bus, pin 0, polarity -
35	C bus, pin 1, polarity +
36	C bus, pin 1, polarity -
37	C bus, pin 2, polarity +
38	C bus, pin 2, polarity -
39	C bus, pin 3, polarity +
40	C bus, pin 3, polarity -
41	C bus, pin 4, polarity +
42	C bus, pin 4, polarity -
43	C bus, pin 5, polarity +
44	C bus, pin 5, polarity -
45	C bus, pin 6, polarity +
46	C bus, pin 6, polarity -
47	C bus, pin 7, polarity +
48	C bus, pin 7, polarity -
49	D bus, pin 0, polarity +
50	D bus, pin 0, polarity -
51	D bus, pin 1, polarity +
52	D bus, pin 1, polarity -
53	D bus, pin 2, polarity +
54	D bus, pin 2, polarity -
55	D bus, pin 3, polarity +
56	D bus, pin 3, polarity -
57	D bus, pin 4, polarity +
58	D bus, pin 4, polarity -
59	D bus, pin 5, polarity +
60	D bus, pin 5, polarity -
61	D bus, pin 6, polarity +
62	D bus, pin 6, polarity -
63	D bus, pin 7, polarity +
64	D bus, pin 7, polarity -
65	GND
66	GND
67	CLK128, polarity +
68	CLK128, polarity -

Pin definition for HSI and HSIR bus connector 2

Pin#	Meaning
1	E bus, pin 0, polarity +
2	E bus, pin 0, polarity -
3	E bus, pin 1, polarity +
4	E bus, pin 1, polarity -
5	E bus, pin 2, polarity +
6	E bus, pin 2, polarity -
7	E bus, pin 3, polarity +
8	E bus, pin 3, polarity -
9	E bus, pin 4, polarity +
10	E bus, pin 4, polarity -
11	E bus, pin 5, polarity +
12	E bus, pin 5, polarity -
13	E bus, pin 6, polarity +
14	E bus, pin 6, polarity -
15	E bus, pin 7, polarity +
16	E bus, pin 7, polarity -
17	F bus, pin 0, polarity +
18	F bus, pin 0, polarity -
19	F bus, pin 1, polarity +
20	F bus, pin 1, polarity -
21	F bus, pin 2, polarity +
22	F bus, pin 2, polarity -
23	F bus, pin 3, polarity +
24	F bus, pin 3, polarity -
25	F bus, pin 4, polarity +
26	F bus, pin 4, polarity -
27	F bus, pin 5, polarity +
28	F bus, pin 5, polarity -
29	F bus, pin 6, polarity +
30	F bus, pin 6, polarity -
31	F bus, pin 7, polarity +
32	F bus, pin 7, polarity -

Pin#	Meaning
33	G bus, pin 0, polarity +
34	G bus, pin 0, polarity -
35	G bus, pin 1, polarity +
36	G bus, pin 1, polarity -
37	G bus, pin 2, polarity +
38	G bus, pin 2, polarity -
39	G bus, pin 3, polarity +
40	G bus, pin 3, polarity -
41	G bus, pin 4, polarity +
42	G bus, pin 4, polarity -
43	G bus, pin 5, polarity +
44	G bus, pin 5, polarity -
45	G bus, pin 6, polarity +
46	G bus, pin 6, polarity -
47	G bus, pin 7, polarity +
48	G bus, pin 7, polarity -
49	H bus, pin 0, polarity +
50	H bus, pin 0, polarity -
51	H bus, pin 1, polarity +
52	H bus, pin 1, polarity -
53	H bus, pin 2, polarity +
54	H bus, pin 2, polarity -
55	H bus, pin 3, polarity +
56	H bus, pin 3, polarity -
57	H bus, pin 4, polarity +
58	H bus, pin 4, polarity -
59	H bus, pin 5, polarity +
60	H bus, pin 5, polarity -
61	H bus, pin 6, polarity +
62	H bus, pin 6, polarity -
63	H bus, pin 7, polarity +
64	H bus, pin 7, polarity -
65	GND
66	GND
67	CLK128, polarity +
68	CLK128, polarity -

Pin definition for HSO bus connector 1

Pin#	Meaning
1	O1 bus, bit 0, polarity +
2	O1 bus, bit 0, polarity -
3	O1 bus, bit 1, polarity +
4	O1 bus, bit 1, polarity -
5	O1 bus, bit 2, polarity +
6	O1 bus, bit 2, polarity -
7	O1 bus, bit 3, polarity +
8	O1 bus, bit 3, polarity -
9	O1 bus, bit 4, polarity +
10	O1 bus, bit 4, polarity -
11	O1 bus, bit 5, polarity +
12	O1 bus, bit 5, polarity -
13	O1 bus, bit 6, polarity +
14	O1 bus, bit 6, polarity -
15	O1 bus, bit 7, polarity +
16	O1 bus, bit 7, polarity -
17	O1 bus, bit 8, polarity +
18	O1 bus, bit 8, polarity -
19	O1 bus, bit 9, polarity +
20	O1 bus, bit 9, polarity -
21	O1 bus, bit 10, polarity +
22	O1 bus, bit 10, polarity -
23	O1 bus, bit 11, polarity +
24	O1 bus, bit 11, polarity -
25	O1 bus, bit 12, polarity +
26	O1 bus, bit 12, polarity -
27	O1 bus, bit 13, polarity +
28	O1 bus, bit 13, polarity -
29	O1 bus, bit 14, polarity +
30	O1 bus, bit 14, polarity -
31	O1 bus, bit 15, polarity +
32	O1 bus, bit 15, polarity -
33	O1 bus, bit 16, polarity +
34	O1 bus, bit 16, polarity -

Pin#	Meaning
35	O1 bus, bit 17, polarity +
36	O1 bus, bit 17, polarity -
37	O1 bus, bit 18, polarity +
38	O1 bus, bit 18, polarity -
39	O1 bus, bit 19, polarity +
40	O1 bus, bit 19, polarity -
41	O1 bus, bit 20, polarity +
42	O1 bus, bit 20, polarity -
43	O1 bus, bit 21, polarity +
44	O1 bus, bit 21, polarity -
45	O1 bus, pin 22, polarity +
46	O1 bus, pin 22, polarity -
47	O1 bus, pin 23, polarity +
48	O1 bus, pin 23, polarity -
49	O1 bus, pin 24, polarity +
50	O1 bus, pin 24, polarity -
51	O1 bus, pin 25, polarity +
52	O1 bus, pin 25, polarity -
53	O1 bus, pin 26, polarity +
54	O1 bus, pin 26, polarity -
55	O1 bus, pin 27, polarity +
56	O1 bus, pin 27, polarity -
57	O1 bus, pin 28, polarity +
58	O1 bus, pin 28, polarity -
59	O1 bus, pin 29, polarity +
60	O1 bus, pin 29, polarity -
61	O1 bus, pin 30, polarity +
62	O1 bus, pin 30, polarity -
63	O1 bus, pin 31, polarity +
64	O1 bus, pin 31, polarity -
65	GND
66	GND
67	O1 bus, clko,polarity +
68	O1 bus, clko,polarity -

Pin definition for HSO bus connector 2

Pin#	Meaning
1	O2 bus, bit 0, polarity +
2	O2 bus, bit 0, polarity -
3	O2 bus, bit 1, polarity +
4	O2 bus, bit 1, polarity -
5	O2 bus, bit 2, polarity +
6	O2 bus, bit 2, polarity -
7	O2 bus, bit 3, polarity +
8	O2 bus, bit 3, polarity -
9	O2 bus, bit 4, polarity +
10	O2 bus, bit 4, polarity -
11	O2 bus, bit 5, polarity +
12	O2 bus, bit 5, polarity -
13	O2 bus, bit 6, polarity +
14	O2 bus, bit 6, polarity -
15	O2 bus, bit 7, polarity +
16	O2 bus, bit 7, polarity -
17	O2 bus, bit 8, polarity +
18	O2 bus, bit 8, polarity -
19	O2 bus, bit 9, polarity +
20	O2 bus, bit 9, polarity -
21	O2 bus, bit 10, polarity +
22	O2 bus, bit 10, polarity -
23	O2 bus, bit 11, polarity +
24	O2 bus, bit 11, polarity -
25	O2 bus, bit 12, polarity +
26	O2 bus, bit 12, polarity -
27	O2 bus, bit 13, polarity +
28	O2 bus, bit 13, polarity -
29	O2 bus, bit 14, polarity +
30	O2 bus, bit 14, polarity -
31	O2 bus, bit 15, polarity +
32	O2 bus, bit 15, polarity -
33	O2 bus, bit 16, polarity +
34	O2 bus, bit 16, polarity -

Pin#	Meaning
35	O2 bus, bit 17, polarity +
36	O2 bus, bit 17, polarity -
37	O2 bus, bit 18, polarity +
38	O2 bus, bit 18, polarity -
39	O2 bus, bit 19, polarity +
40	O2 bus, bit 19, polarity -
41	O2 bus, bit 20, polarity +
42	O2 bus, bit 20, polarity -
43	O2 bus, bit 21, polarity +
44	O2 bus, bit 21, polarity -
45	O2 bus, pin 22, polarity +
46	O2 bus, pin 22, polarity -
47	O2 bus, pin 23, polarity +
48	O2 bus, pin 23, polarity -
49	O2 bus, pin 24, polarity +
50	O2 bus, pin 24, polarity -
51	O2 bus, pin 25, polarity +
52	O2 bus, pin 25, polarity -
53	O2 bus, pin 26, polarity +
54	O2 bus, pin 26, polarity -
55	O2 bus, pin 27, polarity +
56	O2 bus, pin 27, polarity -
57	O2 bus, pin 28, polarity +
58	O2 bus, pin 28, polarity -
59	O2 bus, pin 29, polarity +
60	O2 bus, pin 29, polarity -
61	O2 bus, pin 30, polarity +
62	O2 bus, pin 30, polarity -
63	O2 bus, pin 31, polarity +
64	O2 bus, pin 31, polarity -
65	GND
66	GND
67	O2 bus, clko,polarity +
68	O2 bus, clko,polarity -

Pin definition for HSC bus connector 1

Pin#	Meaning
1	D bus, bit 0
2	D bus, bit 1
3	D bus, bit 2
4	D bus, bit 3
5	D bus, bit 4
6	D bus, bit 5
7	D bus, bit 6
8	D bus, bit 7
9	D bus, bit 8
10	D bus, bit 9
11	D bus, bit 10
12	D bus, bit 11
13	D bus, bit 12
14	D bus, bit 13
15	D bus, bit 14
16	D bus, bit 15
17	D bus, bit 16
18	D bus, bit 17
19	D bus, bit 18
20	D bus, bit 19
21	D bus, bit 20
22	D bus, bit 21
23	D bus, bit 22
24	D bus, bit 23
25	D bus, bit 24
26	D bus, bit 25
27	D bus, bit 26
28	D bus, bit 27
29	D bus, bit 28
30	D bus, bit 29
31	D bus, bit 30
32	D bus, bit 31
33	GND
34	GND

Pin#	Meaning
35	A bus, bit 0
36	A bus, bit 1
37	A bus, bit 2
38	A bus, bit 3
39	A bus, bit 4
40	A bus, bit 5
41	A bus, bit 6
42	A bus, pin 7
43	A bus, pin 8
44	A bus, pin 9
45	A bus, pin 10
46	A bus, pin 11
47	A bus, pin 12
48	A bus, pin 13
49	A bus, pin 14
50	A bus, pin 15
51	C bus, R/W
52	C bus, CS strobe
53	GND
54	GND
55	TCK
56	TDI
57	TDO
58	TMS
59	
60	
61	
62	
63	
64	
65	
66	
67	
68	

Pin definition for HSC/HSM bus connector 2

Pin#	Meaning
1	D bus, bit 0
2	D bus, bit 1
3	D bus, bit 2
4	D bus, bit 3
5	D bus, bit 4
6	D bus, bit 5
7	D bus, bit 6
8	D bus, bit 7
9	D bus, bit 8
10	D bus, bit 9
11	D bus, bit 10
12	D bus, bit 11
13	D bus, bit 12
14	D bus, bit 13
15	D bus, bit 14
16	D bus, bit 15
17	D bus, bit 16
18	D bus, bit 17
19	D bus, bit 18
20	D bus, bit 19
21	D bus, bit 20
22	D bus, bit 21
23	D bus, bit 22
24	D bus, bit 23
25	D bus, bit 24
26	D bus, bit 25
27	D bus, bit 26
28	D bus, bit 27
29	D bus, bit 28
30	D bus, bit 29
31	D bus, bit 30
32	D bus, bit 31
33	GND
34	GND

Pin#	Meaning
35	A bus, bit 0
36	A bus, bit 1
37	A bus, bit 2
38	A bus, bit 3
39	A bus, bit 4
40	A bus, bit 5
41	A bus, bit 6
42	A bus, pin 7
43	M bus, pin 0, polarity -
44	M bus, pin 0, polarity -
45	M bus, pin 1, polarity -
46	M bus, pin 1, polarity -
47	M bus, pin 2, polarity -
48	M bus, pin 2, polarity -
49	M bus, pin 3, polarity -
50	M bus, pin 3, polarity -
51	M bus, pin 4, polarity -
52	M bus, pin 4, polarity -
53	M bus, pin 5, polarity -
54	M bus, pin 5, polarity -
55	M bus, pin 6, polarity -
56	M bus, pin 6, polarity -
57	M bus, pin 7, polarity -
58	M bus, pin 7, polarity -
59	M bus, pin 8, polarity -
60	M bus, pin 8, polarity -
61	M bus, pin 9, polarity -
62	M bus, pin 9, polarity -
63	M bus, pin 10, polarity -
64	M bus, pin 10, polarity -
65	M bus, pin 11, polarity +
66	M bus, pin 11, polarity -
67	M bus, clk,polarity +
68	M bus, clk,polarity -

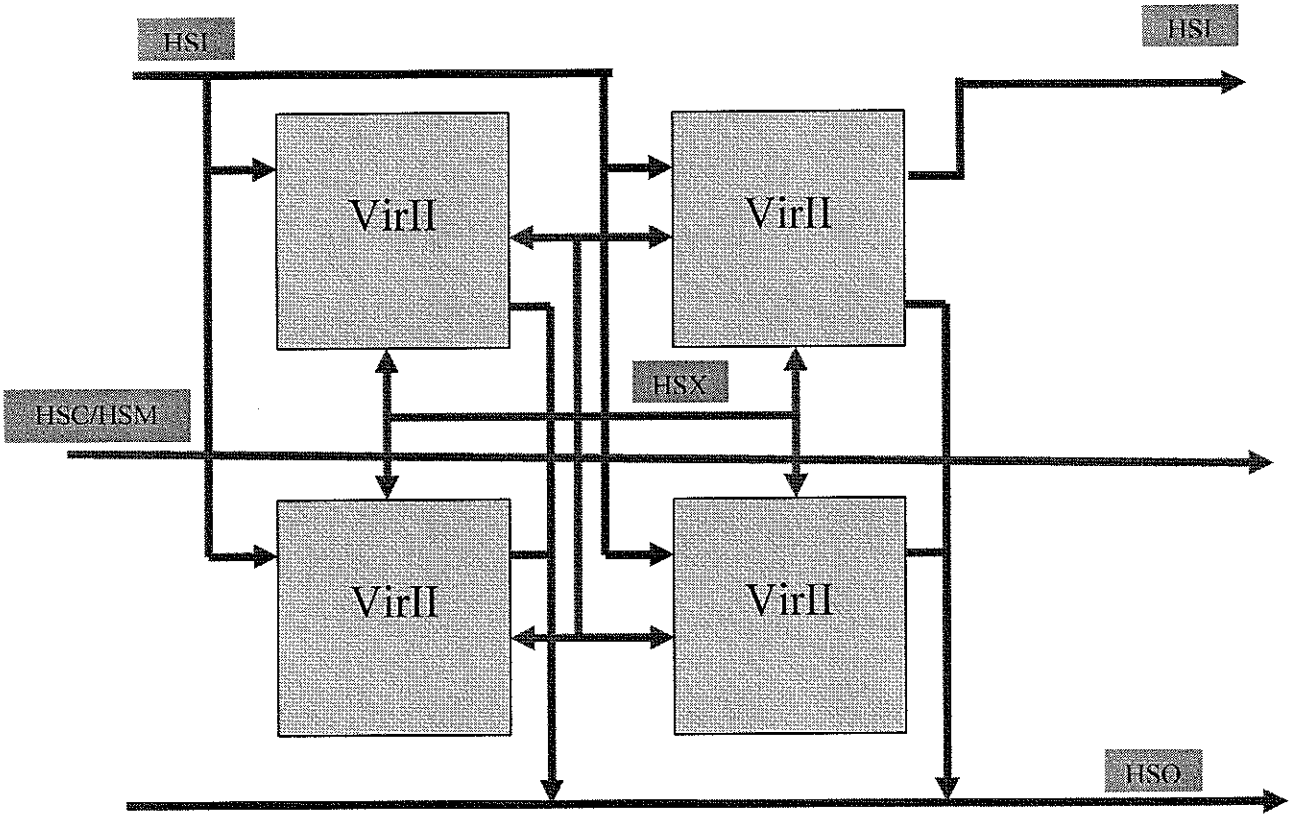

Fig. 1

DBBC Core Modules Cascade Architecture

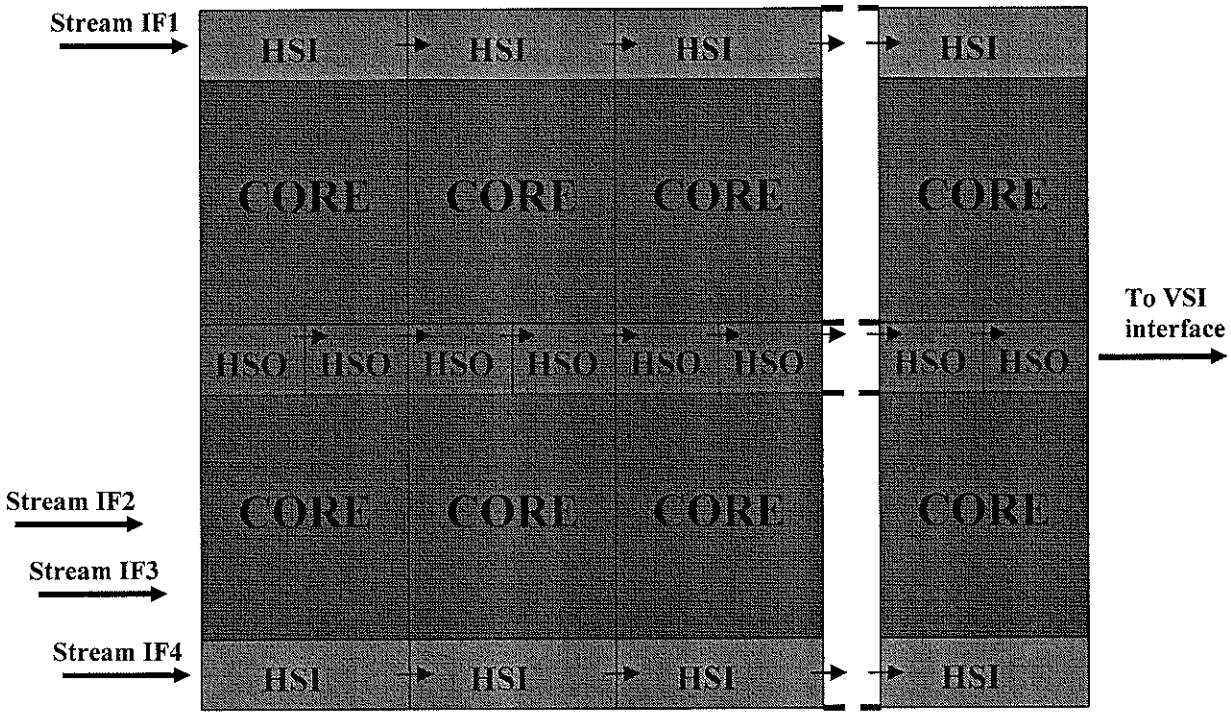

Fig. 2

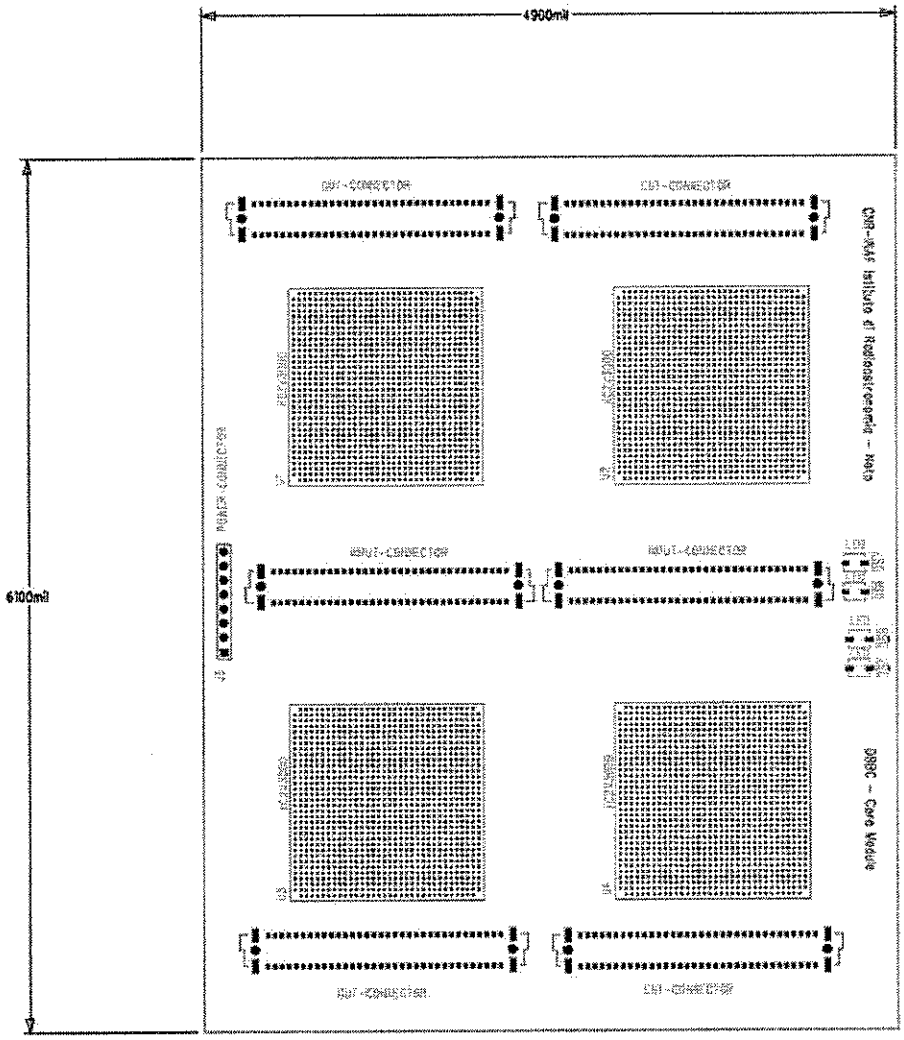

Fig. 3

Virtex-II Platform FPGAs: Complete Data Sheet

DS031 (v3.3) June 24, 2004

Product Specification

Module 1: Introduction and Overview

DS031-1 (v3.3) June 24, 2004
7 pages

- Summary of Features
- General Description
- Device/Package Combinations and Maximum I/O
- Ordering Information

Module 2: Functional Description

DS031-2 (v3.3) June 24, 2004
39 pages

- Detailed Description
- Digitally Controlled Impedance (DCI)
- Configurable Logic Blocks (CLBs)
- Sum of Products
- 3-State Buffers
- 18-Kb Block SelectRAM™ Resources
- 18-Bit x 18-Bit Multipliers
- Global Clock Multiplexer Buffers
- Digital Clock Manager (DCM)
- Active Interconnect Technology
- Creating a Design
- Configuration

Module 3: DC and Switching Characteristics

DS031-3 (v3.3) June 24, 2004
42 pages

- Electrical Characteristics
- Performance Characteristics
- Switching Characteristics
- Pin-to-Pin Output Parameter Guidelines
- Pin-to-Pin Input Parameter Guidelines
- DCM Timing Parameters

Module 4: Pinout Information

DS031-4 (v3.3) June 24, 2004
226 pages

- Pin Definitions
- Pinout Tables
  - CS144/CSG144 Chip-Scale BGA Package
  - FG256/FGG256 Fine-Pitch BGA Package
  - FG456/FGG456 Fine-Pitch BGA Package
  - FG676/FGG676 Fine-Pitch BGA Package
  - BG575/BGG575 Standard BGA Package
  - BG728/BGG728 Standard BGA Package
  - FF896 Flip-Chip Fine-Pitch BGA Package
  - FF1152 Flip-Chip Fine-Pitch BGA Package
  - FF1517 Flip-Chip Fine-Pitch BGA Package
  - BF957Flip-Chip BGA Package

IMPORTANT NOTE: *Page, figure, and table numbers begin at 1 for each module, and each module has its own Revision History at the end. Use the PDF "Bookmarks" pane for easy navigation in this volume.*

Virtex-II Platform FPGAs: Introduction and Overview

DS031-1 (v3.3) June 24, 2004

Product Specification

Summary of Virtex-II™ Features

- Industry First Platform FPGA Solution
- IP-Immersion Architecture
  - Densities from 40K to 8M system gates
  - 420 MHz internal clock speed (Advance Data)
  - 840+ Mb/s I/O (Advance Data)
- SelectRAM™ Memory Hierarchy
  - 3 Mb of dual-port RAM in 18 Kbit block SelectRAM resources
  - Up to 1.5 Mb of distributed SelectRAM resources
- High-Performance Interfaces to External Memory
  - DRAM interfaces
    - SDR / DDR SDRAM
    - Network FCRAM
    - Reduced Latency DRAM
  - SRAM interfaces
    - SDR / DDR SRAM
    - QDR™ SRAM
  - CAM interfaces
- Arithmetic Functions
  - Dedicated 18-bit x 18-bit multiplier blocks
  - Fast look-ahead carry logic chains
- Flexible Logic Resources
  - Up to 93,184 internal registers / latches with Clock Enable
  - Up to 93,184 look-up tables (LUTs) or cascadable 16-bit shift registers
  - Wide multiplexers and wide-input function support
  - Horizontal cascade chain and sum-of-products support
  - Internal 3-state bussing
- High-Performance Clock Management Circuitry
  - Up to 12 DCM (Digital Clock Manager) modules
    - Precise clock de-skew
    - Flexible frequency synthesis
    - High-resolution phase shifting
  - 16 global clock multiplexer buffers
- Active Interconnect Technology
  - Fourth generation segmented routing structure
  - Predictable, fast routing delay, independent of fanout
- SelectIO™-Ultra Technology
  - Up to 1,108 user I/Os
  - 19 single-ended and six differential standards
  - Programmable sink current (2 mA to 24 mA) per I/O
  - Digitally Controlled Impedance (DCI) I/O: on-chip termination resistors for single-ended I/O standards
  - PCI-X compatible (133 MHz and 66 MHz) at 3.3V
  - PCI compliant (66 MHz and 33 MHz) at 3.3V
  - CardBus compliant (33 MHz) at 3.3V
  - Differential Signaling
    - 840 Mb/s Low-Voltage Differential Signaling I/O (LVDS) with current mode drivers
    - Bus LVDS I/O
    - Lightning Data Transport (LDT) I/O with current driver buffers
    - Low-Voltage Positive Emitter-Coupled Logic (LVPECL) I/O
    - Built-in DDR input and output registers
  - Proprietary high-performance SelectLink Technology
    - High-bandwidth data path
    - Double Data Rate (DDR) link
    - Web-based HDL generation methodology
- Supported by Xilinx Foundation™ and Alliance Series™ Development Systems
  - Integrated VHDL and Verilog design flows
  - Compilation of 10M system gates designs
  - Internet Team Design (ITD) tool
- SRAM-Based In-System Configuration
  - Fast SelectMAP configuration
  - Triple Data Encryption Standard (DES) security option (Bitstream Encryption)
  - IEEE 1532 support
  - Partial reconfiguration
  - Unlimited reprogrammability
  - Readback capability
- 0.15 µm 8-Layer Metal Process with 0.12 µm High-Speed Transistors
- 1.5V (V_{CCINT}) Core Power Supply, Dedicated 3.3V V_{CCAUX} Auxiliary and V_{CCO} I/O Power Supplies
- IEEE 1149.1 Compatible Boundary-Scan Logic Support
- Flip-Chip and Wire-Bond Ball Grid Array (BGA) Packages in Three Standard Fine Pitches (0.80 mm, 1.00 mm, and 1.27 mm)
- Wire-Bond BGA Devices Available in Pb-Free Packaging (**www.xilinx.com/pbfree**)
- 100% Factory Tested

Table 1: **Virtex-II Field-Programmable Gate Array Family Members**

Device	System Gates	CLB (1 CLB = 4 slices = Max 128 bits)			Multiplier Blocks	SelectRAM Blocks		DCMs	Max I/O Pads(1)
		Array Row x Col.	Slices	Maximum Distributed RAM Kbits		18 Kbit Blocks	Max RAM (Kbits)		
XC2V40	40K	8 x 8	256	8	4	4	72	4	88
XC2V80	80K	16 x 8	512	16	8	8	144	4	120
XC2V250	250K	24 x 16	1,536	48	24	24	432	8	200
XC2V500	500K	32 x 24	3,072	96	32	32	576	8	264
XC2V1000	1M	40 x 32	5,120	160	40	40	720	8	432
XC2V1500	1.5M	48 x 40	7,680	240	48	48	864	8	528
XC2V2000	2M	56 x 48	10,752	336	56	56	1,008	8	624
XC2V3000	3M	64 x 56	14,336	448	96	96	1,728	12	720
XC2V4000	4M	80 x 72	23,040	720	120	120	2,160	12	912
XC2V6000	6M	96 x 88	33,792	1,056	144	144	2,592	12	1,104
XC2V8000	8M	112 x 104	46,592	1,456	168	168	3,024	12	1,108

Notes:
1. See details in Table 2, "Maximum Number of User I/O Pads".

General Description

The Virtex-II family is a platform FPGA developed for high performance from low-density to high-density designs that are based on IP cores and customized modules. The family delivers complete solutions for telecommunication, wireless, networking, video, and DSP applications, including PCI, LVDS, and DDR interfaces.

The leading-edge 0.15 µm / 0.12 µm CMOS 8-layer metal process and the Virtex-II architecture are optimized for high speed with low power consumption. Combining a wide variety of flexible features and a large range of densities up to 10 million system gates, the Virtex-II family enhances programmable logic design capabilities and is a powerful alternative to mask-programmed gates arrays. As shown in Table 1, the Virtex-II family comprises 11 members, ranging from 40K to 8M system gates.

Packaging

Offerings include ball grid array (BGA) packages with 0.80 mm, 1.00 mm, and 1.27 mm pitches. In addition to traditional wire-bond interconnects, flip-chip interconnect is used in some of the BGA offerings. The use of flip-chip interconnect offers more I/Os than is possible in wire-bond versions of the similar packages. Flip-chip construction offers the combination of high pin count with high thermal capacity.

Wire-bond packages CS, FG, and BG are optionally availabe in Pb-free versions CSG, FGG, and BGG. See **Virtex-II Ordering Examples, page 6.**

Table 2 shows the maximum number of user I/Os available. The Virtex-II device/package combination table (Table 6 at the end of this section) details the maximum number of I/Os for each device and package using wire-bond or flip-chip technology.

Table 2: **Maximum Number of User I/O Pads**

Device	Wire-Bond	Flip-Chip
XC2V40	88	-
XC2V80	120	-
XC2V250	200	-
XC2V500	264	-
XC2V1000	328	432
XC2V1500	392	528
XC2V2000	-	624
XC2V3000	516	720
XC2V4000	-	912
XC2V6000	-	1,104
XC2V8000	-	1,108