DBBC - Wideband Digital Base Band Converter System

Demultiplexer

Ver.1.0

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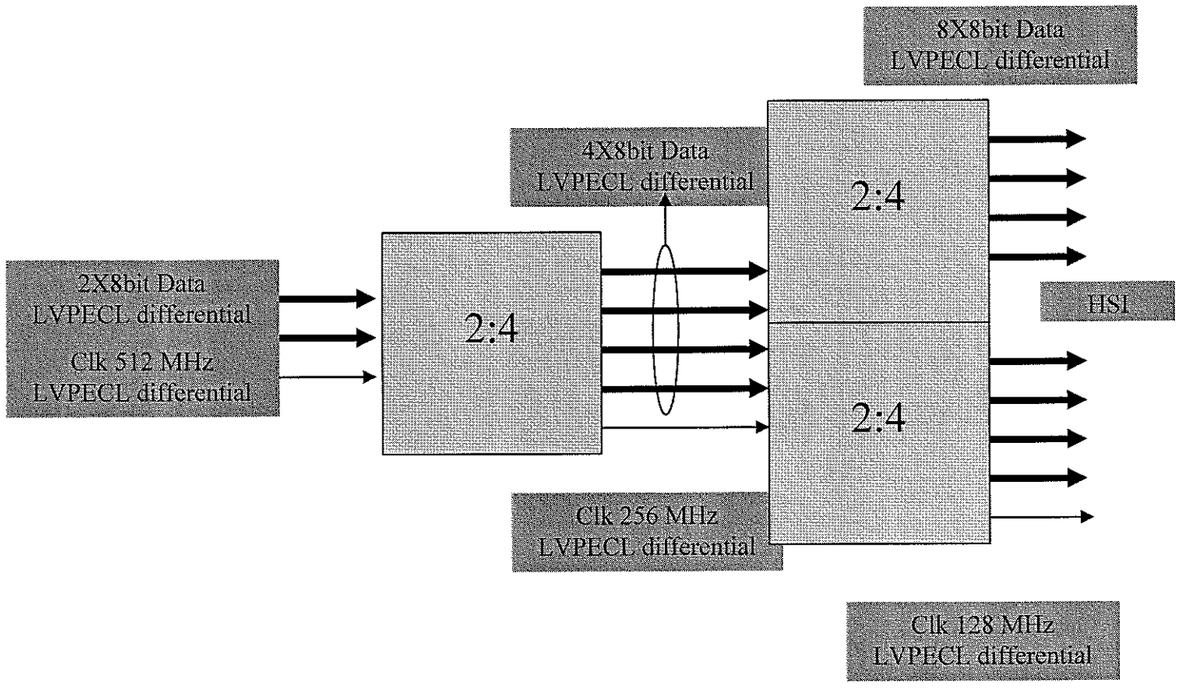
EVN Doc n. 117/2004

1. Description

Data sampled in the AD module are to be transferred to the CoreModule using a parallel bus. The AD module is indded sampling at 1024 MHz clock rate and for simplifing the data distribution is using a demultipler to reduce the clock rate at one half the sample rate. So the 8 bit wide bus, is output as two differential LVPECL bus with 512 MHz clock. This clock rate is still too high as processing rate with the FPGA VirtexII family device, so that a further data rate reduction is necessary.
Accordingly with a compromise between cost, number of gates, resources complexity, max data rate, the Virtex II family has been chosen, able to work at a sustained clock rate in eccess of 128 MHz. Using such devices as main processing element is then necessary to perform a 2:8 data demultiplexing to achieve the 128MHz of processing rate, starting from 512 MHz. Such demultipler section is then operating between the AD section and the Core Module.



The Demultiplexer Module can be composed by two sections in cascade, one operating at the input clock frequency, 512 MHz, and producing a 2:4 version of data with four buses @256MHz, the second section operating with such data as input and two further stages 2:4 having 8 buses @128 MHz.
How to implement such functionality should be carefully evaluated, but the easiest solution seems to be adopting discrete components of appropriate working frequency. A class of fast digital devices is available as standard logic at this time from ON Semiconductor, from which is possible to get design elements operating in the gigahertz domain. A possible implementation can then be realized with an appropriate board layout particular care.
Other solutions could come from the new device family V4 from Xilinx, but still at the time of this document preparation not experience is available, but only information on specification that would meet the needed performance.

In this description we add a practical schematic drawing as starting point for development. This circuit anyway should be considered preliminary and subject to evaluation.

Device MC100EP451 is a 6-bit differential register operating with common clock up to 3.0 GHz, so well over the 512 MHz that is required as maximum clock in this project. Operating with opposite phase in the clock distribution data are registered with a 256MHz clock version in two passes, so to present two consecutive samples introduced at 512 MHz in two bus at 256 MHz.
This is realized for both P and A bus as coming from the AD MAX 108 converter and then producing 4 bus. Each one of these is then subject to the same process again with a clock version at 128 MHz, producing the final effect of 2:8 demultiplexing.

Reduction of clock frequency is realized dividing the input clock with device MC100EP52 in configuration such to toggle data input at a rate of the input clock. Overall effect is to divide by two, that is then again realized for the final output clock.

Clock distribution, that looks to be critical is realized with the help of the differential low skew 1:5 dedicated chip, still operating at LVPECL level.

The output bus is the HSI bus for the CoreModule boards, while the input bus is named VHSI for signals coming from the AD section.

VHSI: 2x8-bit, differential, 512 MHz clock

HSI: 8x8-bit, differential, 128 MHz clock

The VHSI bus due to the very fast clock frequency is a collection of coaxial connectors grouped in a bus-like meaning.

Pin definition for VHSI bus

Pin/Connector#	Meaning
1	P bus, pin 0, polarity +
2	P bus, pin 0, polarity -
3	P bus, pin 1, polarity +
4	P bus, pin 1, polarity -
5	P bus, pin 2, polarity +
6	P bus, pin 2, polarity -
7	P bus, pin 3, polarity +
8	P bus, pin 3, polarity -
9	P bus, pin 4, polarity +
10	P bus, pin 4, polarity -
11	P bus, pin 5, polarity +
12	P bus, pin 5, polarity -
13	P bus, pin 6, polarity +
14	P bus, pin 6, polarity -
15	P bus, pin 7, polarity +
16	P bus, pin 7, polarity -
17	A bus, pin 0, polarity +
18	A bus, pin 0, polarity -
19	A bus, pin 1, polarity +
20	A bus, pin 1, polarity -
21	A bus, pin 2, polarity +
22	A bus, pin 2, polarity -
23	A bus, pin 3, polarity +
24	A bus, pin 3, polarity -
25	A bus, pin 4, polarity +
26	A bus, pin 4, polarity -
27	A bus, pin 5, polarity +
28	A bus, pin 5, polarity -
29	A bus, pin 6, polarity +
30	A bus, pin 6, polarity -
31	A bus, pin 7, polarity +
32	A bus, pin 7, polarity -
33	Data Ready, polarity +
34	Data Ready, polarity -

Pin definition for HSI bus connector 1

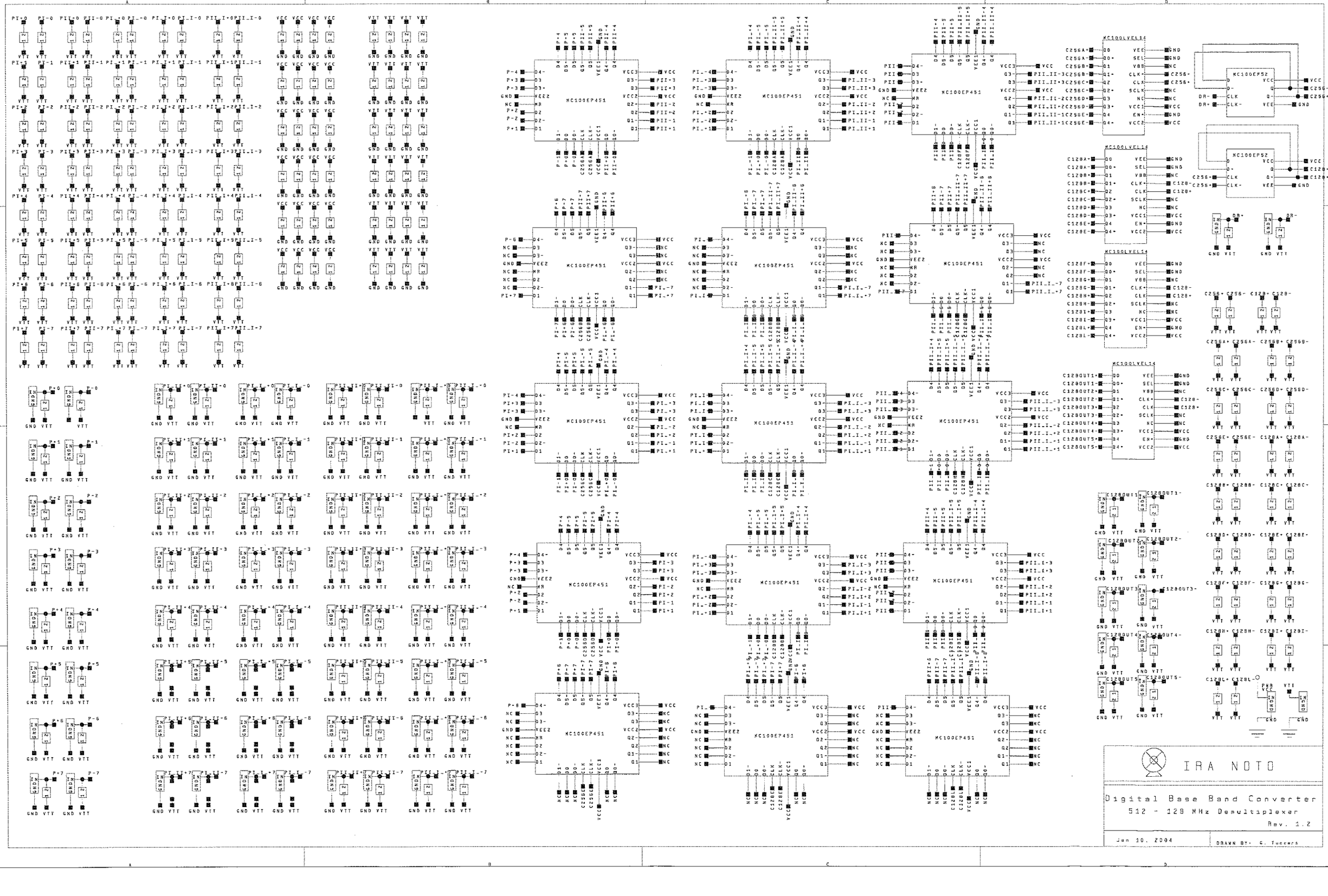
Pin#	Meaning
1	A bus, pin 0, polarity +
2	A bus, pin 0, polarity -
3	A bus, pin 1, polarity +
4	A bus, pin 1, polarity -
5	A bus, pin 2, polarity +
6	A bus, pin 2, polarity -
7	A bus, pin 3, polarity +
8	A bus, pin 3, polarity -
9	A bus, pin 4, polarity +
10	A bus, pin 4, polarity -
11	A bus, pin 5, polarity +
12	A bus, pin 5, polarity -
13	A bus, pin 6, polarity +
14	A bus, pin 6, polarity -
15	A bus, pin 7, polarity +
16	A bus, pin 7, polarity -
17	B bus, pin 0, polarity +
18	B bus, pin 0, polarity -
19	B bus, pin 1, polarity +
20	B bus, pin 1, polarity -
21	B bus, pin 2, polarity +
22	B bus, pin 2, polarity -
23	B bus, pin 3, polarity +
24	B bus, pin 3, polarity -
25	B bus, pin 4, polarity +
26	B bus, pin 4, polarity -
27	B bus, pin 5, polarity +
28	B bus, pin 5, polarity -
29	B bus, pin 6, polarity +
30	B bus, pin 6, polarity -
31	B bus, pin 7, polarity +
32	B bus, pin 7, polarity -

Pin#	Meaning
33	C bus, pin 0, polarity +
34	C bus, pin 0, polarity -
35	C bus, pin 1, polarity +
36	C bus, pin 1, polarity -
37	C bus, pin 2, polarity +
38	C bus, pin 2, polarity -
39	C bus, pin 3, polarity +
40	C bus, pin 3, polarity -
41	C bus, pin 4, polarity +
42	C bus, pin 4, polarity -
43	C bus, pin 5, polarity +
44	C bus, pin 5, polarity -
45	C bus, pin 6, polarity +
46	C bus, pin 6, polarity -
47	C bus, pin 7, polarity +
48	C bus, pin 7, polarity -
49	D bus, pin 0, polarity +
50	D bus, pin 0, polarity -
51	D bus, pin 1, polarity +
52	D bus, pin 1, polarity -
53	D bus, pin 2, polarity +
54	D bus, pin 2, polarity -
55	D bus, pin 3, polarity +
56	D bus, pin 3, polarity -
57	D bus, pin 4, polarity +
58	D bus, pin 4, polarity -
59	D bus, pin 5, polarity +
60	D bus, pin 5, polarity -
61	D bus, pin 6, polarity +
62	D bus, pin 6, polarity -
63	D bus, pin 7, polarity +
64	D bus, pin 7, polarity -
65	GND
66	GND
67	CLK128, polarity +
68	CLK128, polarity -

Pin definition for HSI and HSIR bus connector 2

Pin#	Meaning
1	E bus, pin 0, polarity +
2	E bus, pin 0, polarity -
3	E bus, pin 1, polarity +
4	E bus, pin 1, polarity -
5	E bus, pin 2, polarity +
6	E bus, pin 2, polarity -
7	E bus, pin 3, polarity +
8	E bus, pin 3, polarity -
9	E bus, pin 4, polarity +
10	E bus, pin 4, polarity -
11	E bus, pin 5, polarity +
12	E bus, pin 5, polarity -
13	E bus, pin 6, polarity +
14	E bus, pin 6, polarity -
15	E bus, pin 7, polarity +
16	E bus, pin 7, polarity -
17	F bus, pin 0, polarity +
18	F bus, pin 0, polarity -
19	F bus, pin 1, polarity +
20	F bus, pin 1, polarity -
21	F bus, pin 2, polarity +
22	F bus, pin 2, polarity -
23	F bus, pin 3, polarity +
24	F bus, pin 3, polarity -
25	F bus, pin 4, polarity +
26	F bus, pin 4, polarity -
27	F bus, pin 5, polarity +
28	F bus, pin 5, polarity -
29	F bus, pin 6, polarity +
30	F bus, pin 6, polarity -
31	F bus, pin 7, polarity +
32	F bus, pin 7, polarity -

Pin#	Meaning
33	G bus, pin 0, polarity +
34	G bus, pin 0, polarity -
35	G bus, pin 1, polarity +
36	G bus, pin 1, polarity -
37	G bus, pin 2, polarity +
38	G bus, pin 2, polarity -
39	G bus, pin 3, polarity +
40	G bus, pin 3, polarity -
41	G bus, pin 4, polarity +
42	G bus, pin 4, polarity -
43	G bus, pin 5, polarity +
44	G bus, pin 5, polarity -
45	G bus, pin 6, polarity +
46	G bus, pin 6, polarity -
47	G bus, pin 7, polarity +
48	G bus, pin 7, polarity -
49	H bus, pin 0, polarity +
50	H bus, pin 0, polarity -
51	H bus, pin 1, polarity +
52	H bus, pin 1, polarity -
53	H bus, pin 2, polarity +
54	H bus, pin 2, polarity -
55	H bus, pin 3, polarity +
56	H bus, pin 3, polarity -
57	H bus, pin 4, polarity +
58	H bus, pin 4, polarity -
59	H bus, pin 5, polarity +
60	H bus, pin 5, polarity -
61	H bus, pin 6, polarity +
62	H bus, pin 6, polarity -
63	H bus, pin 7, polarity +
64	H bus, pin 7, polarity -
65	GND
66	GND
67	CLK128, polarity +
68	CLK128, polarity -


MC100EP451
MC100LVEL14
MC100EP52
IRA NOTO
Digital Base Band Converter
512 - 128 MHz Demultiplexer
Rev. 1.2
Jan 10, 2004
DRAWN BY: G. Tuccari

MC10EP451, MC100EP451

3.3V / 5V ECL 6-Bit Differential Register with Master Reset

The MC10/100EP451 is a 6–bit fully differential register with common clock and Single–Ended Master Reset (MR). It is ideal for very high frequency applications where a registered data path is necessary.

All inputs have a 75 kΩ pulldown resistor internally. Differential inputs have an override clamp. Unused differential register inputs can be left open and will default LOW. When the differential inputs are forced to $<V_{EE}$ + 1.2 V, the clamp will override and force the output to a default state. When in the default state, and since the flip–flop is edge triggered, the output reaches a determined, but not predicted, valid state.

The positive transition of CLK (pin 4) will latch the registers. Master Reset (MR) HIGH will asynchronously reset all registers forcing Q outputs to go LOW.

The 100 Series contains temperature compensation.

- 450 ps Typical Propagation Delay
- Maximum Frequency > 3.0 GHz Typical
- Asynchronous Master Reset
- 20 ps Skew Within Device, 35 ps Skew Device–To–Device
- PECL Mode Operating Range: V_{CC} = 3.0 V to 5.5 V
  With V_{EE} = 0 V
- NECL Mode Operating Range: V_{CC} = 0 V
  With V_{EE} = –3.0 V to –5.5 V
- Open Input Default State
- Safety Clamp on Inputs

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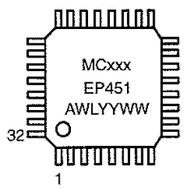
LQFP–32
FA SUFFIX
CASE 873A

MARKING DIAGRAM*



xxx = 10 or 100
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

*For additional information, see Application Note AND8002/D

ORDERING INFORMATION

Device	Package	Shipping
MC10EP451FA	LQFP–32	250 Units/Tray
MC10EP451FAR2	LQFP–32	2000 Tape & Reel
MC100EP451FA	LQFP–32	250 Units/Tray
MC100EP451FAR2	LQFP–32	2000 Tape & Reel

MC10EP52, MC100EP52

3.3V / 5V ECL Differential Data and Clock D Flip-Flop

The MC10EP/100EP52 is a differential data, differential clock D flip–flop. The device is pin and functionally equivalent to the EL52 device.

Data enters the master portion of the flip–flop when the clock is LOW and is transferred to the slave, and thus the outputs, upon a positive transition of the clock. The differential clock inputs of the EP52 allow the device to also be used as a negative edge triggered device.

The EP52 employs input clamping circuitry so that under open input conditions (pulled down to V_{EE}) the outputs of the device will remain stable.

The 100 Series contains temperature compensation.

- 330 ps Typical Propagation Delay
- Maximum Frequency > 4 GHz Typical
- PECL Mode: V_{CC} = 3.0 V to 5.5 V with V_{EE} = 0 V
- NECL Mode: V_{CC} = 0 V with V_{EE} = –3.0 V to –5.5 V
- Open Input Default State
- Safety Clamp on Inputs
- Q Output Will Default LOW with Inputs Open or at V_{EE}

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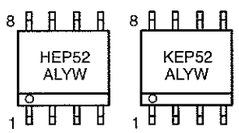
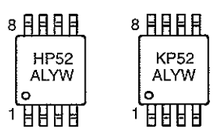
MARKING DIAGRAMS*

SO–8
D SUFFIX
CASE 751



TSSOP–8
DT SUFFIX
CASE 948R



H = MC10
K = MC100
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

*For additional information, see Application Note AND8002/D

ORDERING INFORMATION

Device	Package	Shipping
MC10EP52D	SO–8	98 Units/Rail
MC10EP52DR2	SO–8	2500 Tape & Reel
MC100EP52D	SO–8	98 Units/Rail
MC100EP52DR2	SO–8	2500 Tape & Reel
MC10EP52DT	TSSOP–8	100 Units/Rail
MC10EP52DTR2	TSSOP–8	2500 Tape & Reel
MC100EP52DT	TSSOP–8	100 Units/Rail
MC100EP52DTR2	TSSOP–8	2500 Tape & Reel

MC100LVEL14

3.3V ECL 1:5 Clock Distribution Chip

The MC100LVEL14 is a low skew 1:5 clock distribution chip designed explicitly for low skew clock distribution applications. The device can be driven by either a differential or single-ended ECL or, if positive power supplies are used, PECL input signal. The LVEL14 is functionally and pin compatible with the EL14 but is designed to operate in ECL or PECL mode for a voltage supply range of –3.0 V to –3.8 V (or 3.0 V to 3.8 V).

The LVEL14 features a multiplexed clock input to allow for the distribution of a lower speed scan or test clock along with the high speed system clock. When LOW (or left open and pulled LOW by the input pulldown resistor) the SEL pin will select the differential clock input.

The common enable ($\overline{EN}$) is synchronous so that the outputs will only be enabled/disabled when they are already in the LOW state. This avoids any chance of generating a runt clock pulse when the device is enabled/disabled as can happen with an asynchronous control. The internal flip flop is clocked on the falling edge of the input clock, therefore all associated specification limits are referenced to the negative edge of the clock input.

The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

- 50 ps Output-to-Output Skew
- Synchronous Enable/Disable
- Multiplexed Clock Input
- ESD Protection: >2 KV HBM
- The 100 Series Contains Temperature Compensation
- PECL Mode Operating Range: V_{CC}= 3.0 V to 3.8 V with V_{EE} = 0 V
- NECL Mode Operating Range: V_{CC}= 0 V with V_{EE} = –3.0 V to –3.8 V
- Internal Input Pulldown Resistors on CLK
- Q Output will Default LOW with Inputs Open or at V_{EE}
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL 94 V–0 @ 0.125 in,
  Oxygen Index: 28 to 34
- Transistor Count = 303 devices

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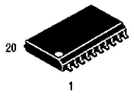
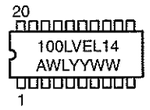


SOIC–20
DW SUFFIX
CASE 751D

MARKING DIAGRAM



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC100LVEL14DW	SOIC–20	38 Units/Rail
MC100LVEL14DWR2	SOIC–20	1000 Units/Reel