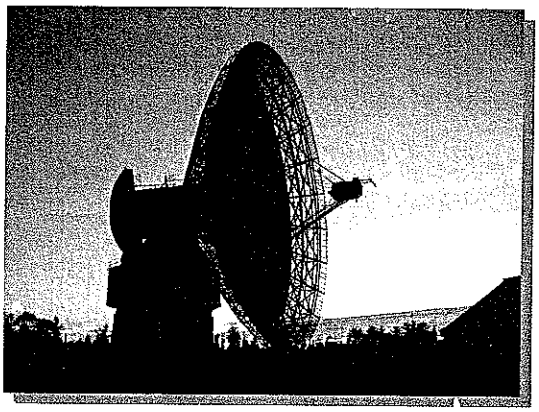
International VLBI Service for Geodesy and Astrometry

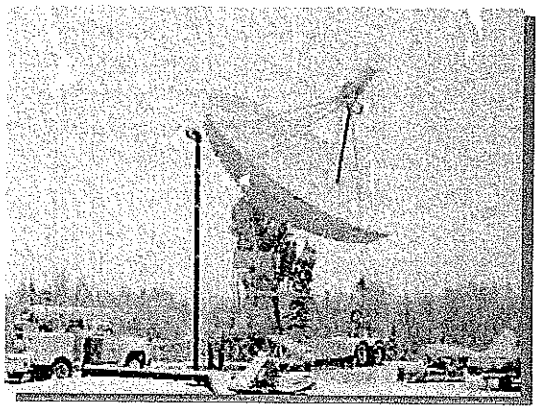
2004

GENERAL MEETING PROCEEDINGS

Ottawa, Canada

February 9-11





NASA/CP-2004-212255

DBBC - A Wide Band Digital Base Band Converter

Gino Tuccari

INAF-IRA, Italian National Astrophysical Institute-RadioAstronomy Institute
e-mail: g.tuccari@ira.cnr.it

Abstract

It is presented a description of a project to develop a fully digital backend system to replace the presently used terminals. The need for such replacement is well known and motivated by the necessity to both: renew an obsolete system whose the components replacement is every day more difficult, and for achieving better performance making use of the more predictable digital techniques. Field Programmable Gate Array (FPGA) components show continuous increasing performance in terms of gate density and working frequency, giving a real opportunity to take advantages within a concept of fully upgrading methodology. Then, if what could now be developed to accomplish the transition between recording systems and the application of the VSI interfacing standard, is realized in the present, still the same hardware environment can be container of different needs in a near future, with the data transport and correlator evolution. This development is producing some prototypes for testing the performance of different architectures taking into account theoretical achievable performance and the actual features. Two samples with preliminary configurations are placed in Noto and Effelsberg; development and testing are indeed performed on the field.

1. Introduction

The introduction of a new backend system in the VLBI system has been widely discussed during the last years, due to different reasons, some looking at the past, others to the future. Indeed the technologies used in the VLBI terminal now adopted, have been developed in the decades 70s and 80s of the past century, and so, now maintenance and performance are strongly affected by their obsolescence. More, data acquisition has been recently deeply upgraded with new disk based recording systems, greatly improving reliability and performance, while e-VLBI is becoming reality, as it can be seen in numerous experiments, proving and preparing the VLBI world to this huge leap.

In the while 'Digital Radio' technologies are becoming familiar within new telecommunication developments, where frequency conversion is required, so that implies as an effort is to be done for understanding if commercial technology is now ready for the VLBI needed performance, at a cost for which also a new generation of radio telescopes, now with a lack of VLBI terminals, could greatly get benefits.

All these considerations, so as others related, imposed the need for such a development. A new backend hardware to be economically convenient, flexible, able to improve the performance, needs to be completely reviewed, trying to keep apart choices or solutions adopted in the past, mostly imposed by the limitations and necessities coming with the tape recording. Such critical reconsideration can greatly furnish benefits in terms of costs and performance.

A new class of commercially available devices is present on the market, fully programmable, giving the possibility to structure a system flexible to be adapted for different needs with different

solutions. This aspect seems to be very promising for supporting also in a future evolutions in the correlators and in the data transfer methods.

2. Project Overview

The main idea staying behind to this project is to replace the existing terminal with a complete and compact system to be used with any VSI compliant recorder or data transport. Moreover the cost has to be limited making use of commercially available components.
Hardware programmability is a feature in order to optimize the architecture to the needed performance, because different performance involve different number of gates necessary to perform the required functionality. Under this assumptions, maximum input and output data rates are the limitation and they have to be set so to satisfy the present and for reasonable future necessities.
The new development needs to be fully compatible with the existing terminals and correlators in order to require a minimum effort to be introduced in the stations and no modification at the correlator side, still maintaining the possibility to be upgraded for wider bands correlators. The upgrades, on the other hand have to be mostly software in order to avoid and modify any hardware part, for cost savings and simplification in the operations, so that programmable hardware is planned as main component.
The entire project is based on a flexible architecture, composed by one or more FPGA boards as computation elements, placed in a mixed cascaded/parallel structure, so to guarantee a parallel usage of data input and a shared parallel output data flow. For such a reason the upgrade could also in principle be possible in hardware replacing or adding compatible modules for different or modified performance, even if this is strongly limited by the software programmability.

In the DBBC project a single unit is composed by four IF Input in the range 50-500 or 500-950 MHz, with each of them feeding a 1.024 GHz sampler. Then four polarizations or bands are available for a single group of output channels selection. In other words, a group of 32 or 64 channels is able to handle a shared combination of channels coming from the four bands.
Multiple architecture can be used taking the advantage to adopt fully re-configurable FPGA Core Modules, where one of such modules is an autonomous board populated with an appropriate number of gates, fed by one of the input IF, and sharing the output data bus. More narrow or few wide channels per module can be assigned, maintaining the maximum number of gates provided by the Core Module. Modular realization for possible cascaded processing is provided, that implies the use of one or more Core Modules for achieving more gates number and then more processing capability. The input bus is cascaded, with very low skew, between modules for the same band.
An analog monitor, produced by DA conversion, has been added for testing purposes, in order to be able and evaluate with a common spectrum analyzer the different channels content and performance. This has been proved particularly useful in order to adopt standard equipment normally in use in our radio-telescopes.

Field System support is required to configure the different modules and allow standard settings, and still getting total power measurements and any other information the converter is able to produce. A partial FPGA configuration approach is used so to optimize the configuration time. Different configurations can be supported for obtain similar, but not identical, functionalities,

such SSB down converter, wide band parallel FIR, poly-phase FIR/FFT. The more flexibilities, the more number of gates and cost. The possibility to independently tune different channels, and to have them filtered at different bandwidth, while it is an obvious feature in the analog implementation, it is not the same in the digital implementation, so that different solutions can be more convenient. The project anyway allows to implement different architectures, and to change them at convenience.

A Core Module can handle a maximum input bandwidth of 10 Gbit/s and a maximum output bandwidth of 4.096 Gbit/s. The two high rate buses are named HIS and HSO respectively, and a further Control/Configuration bus, HSCC, adopts PCI-X (or 3GIO(1x) if available during the development time).
Different modules with different number of gates are supported for different functionalities and costs, making use of a standard board populated with a flexible number of chips. A module with 24 Mgates can handle up to 4 independent narrow band LSB&USB channels (preliminary), or 4 wide band channels (ex. 1X512, 2x256, 4x128 MHz) (preliminary).

3. Digital Down Converter Configuration

Different architectures can be used in the Core Modules, having different performance and behaviors. One possible configuration is the DDC digital down converter in the classical implementation meaning. In such a solution a direct conversion is typically performed between high data rate sampled IF band and lower data rate base band. One or two channels are generated for each converter, as in the analog implementation. Important differences, greatly improving the performance are anyway present: local oscillator is a Numerically Controlled Oscillator (NCO), mixer is complex as Look Up Table multiplier, low-pass band filters are Finite Impulse Response (FIR). Decimation circuitry is adopted because of the high ratio between IF and output data rate and is performed with multirate/multistage FIR.
Digital Total Power (DTP) measurement at IF and at base band level is adopted, Rescaling/Gain Control (RGC) is adopted for dynamic range control and final data representation.

Narrow bandwidth typically adopted is defined for this project in the range: 16, 8, 4, 2, 1 MHz, having still possibility to filter with narrower bandwidth. Such solution directly affect the tuning step size. Still, the finer tuning capability, the more resource needed, with consequent number of gates involved and cost increasing.
Wide bandwidths are defined as 512, 256, 128, 64, 32 MHz and are generated at fixed tuning bases. So for example the 512 MHz band is in the range 0 - 512, or 512 - 1024 MHz IF band; 256 MHz band is defined as 0-256/256-512, or 512-768/768-1024 MHz, and so on.

Output data rate is 32 MHz at present in order to be able and fit with the standard, now adopted VSI-H data rate, but 64 and 128 MHz are available. Data output configuration for wide bands is conceived in a multiplexing fashion.

4. Development Issues

The development will pass through two prototype levels, each of them characterized by testing with real observations. The first level includes two systems with an environment including A/D, FPGAs, D/A, etc., that have been assembled and named 'DbbcProt A', placed in IRA (Noto) and 'DbbcProt B' placed in MPI (Bonn, Effelsberg). Development and on field testing between units are linked together, including correlation phases, in order to keep under control effects on the real data.
A modified version of the EVN MKIV formatter with digital input is used in the first phase of development, while afterwards a VSI interface will be used. At the end of the development period four functionally complete prototypes of second generation will be delivered to stations for a more complete testing. Such final prototypes will be able to include VSI-E interfacing capabilities, through an optional high speed network connection.

References

[1] Ferris, D. Digital Filters and Filterbanks for VLBI.
Presented at the Symposium of the International VLBI Service for Geodesy and Astrometry "New Technologies in VLBI", held in Gyeong-ju, Korea, 5-8 November 2002

[2] Tuccari, G. Development of a Digital base Band Converter (DBBC): Basic Elements and Preliminary Results. "New Technologies in VLBI", ASP Conference Series, Vol. 306, 2003, ed. Y. C. Minh (San Francisco: ASP), pp. 177-192