Max-Planck-Institut
für Radioastronomie

Effelsberg Direct Digitization

Packetizer – Backend

Interface Control Document

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Document Revisions

Revision	Date	Comments	Author
1.0	11/Sep/2017	Initial Revision	A. Bansod
1.1,1.2	12/Dec/2017	Minor corections, Item Pointers Change for 12 bit mode	A. Bansod
1.3	03/May/2018	Added Filter Bank SPEAD Interface Definition, Heap Id Changes	A. Bansod
1.4	09/May/2018	Corrections on data rates and heap id structure for 12 bit mode	A. Bansod
1.5	23/Jan/2019	Information on Feng Firmware SPEAD format	A. Bansod
1.6	08/Feb/2019	Modified SPEAD Heap Id and Offset, Section 1.1.6	A. Bansod

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LIST OF ABBREVIATIONS

ABBREVIATION	
Eff/Effelsberg	Effelsberg 100m Telescope
GbE	Gigabit Ethernet
ICD	Interface Control Document
IP	Internet Protocol
FFT	Fast Fourier Transform
LSB	Least Significant Bit
MSB	Most Significant Bit
PFB	Polyphase Filter Bank
PPS	Pulse Per Second
SPEAD	Streaming Protocol for Exchanging Astronomical Data
TBC	To Be Confirmed
TBD	To Be Determined
UBB	Ultra-Broad Band Receiver
UDP	User Datagram Protocol

1. INTERFACE DEFINITION

This interface defines the interface between the planned Packetizers for the Effelsberg Receivers with direct digitization and the Backends.

An overview of the planned interface is given in Figure 1.

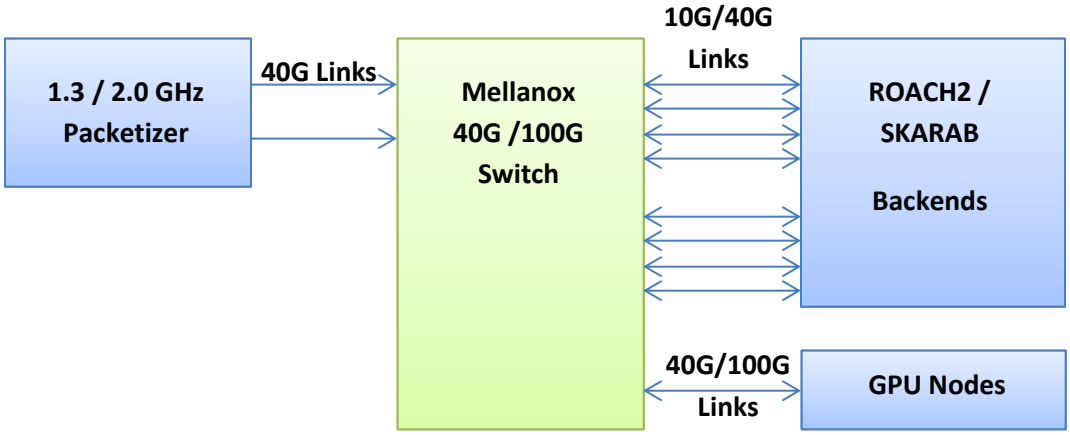

Figure 1: Packetizer – Backend Interface Overview

1.1 Interface Description

The interface facilitates the data transfer from the Packetizer to the Backends via SPEAD [1, 2] protocol over Ethernet (Multicast UDP stream). The Packetizer sends data over 2 40GbE Links to a Mellanox 40GbE/100GbE switch which is then either received by the ROACH2 based Backends over 8 10GbE (80 Gbps) links, SKARAB over 4 40GbE links (160 Gbps) or GPU nodes over 2 40GbE links.

1.1.1 Packetizer Timestamp

The SPEAD metadata will include a 48-bit timestamp synchronized with the first ADC sample in the data payload. The first sample needs to be aligned with the 1PPS signal available at Effelsberg and an synchronization command to sync the data with a given 1PPS signal should be available from the Packetizer interface. The timestamp then should be incremented by the number of samples per FPGA clock available from the ADC. The timestamp should represent the number of ADC samples from the synchronization with the 1PPS signal. The timestamp is referred as SPEADTIME for rest of this document. In current setup, the SPEADTIME increments by 4096 for a given UDP packet and the actual value is written in SPEAD header.

1.1.2 EDD Packetizer Data Packetization

The direct digitization scheme will be first used for UBB receiver at Effelsberg. The UBB Packetizer shall support following mode of operation viz.

- 1.3 GHz Bandwidth @ 12 bits Samples per Polarization

For the initial test with the EDD Backend, following mode will be used with C+ receiver signal available at Faraday room at Effelsberg

- 2 GHz Bandwidth @ 8 bits Samples per Polarization

2.0 GHz Bandwidth @ 8 bits

In this mode, the Packetizer should transmit 4096 bytes, 8 bit signed data from the same polarization over 40GbE link. The layout of the data as well as link budget using 2x 40GbE links is given in Table 1 & 2 respectively.

ADC Data Frame	***Number of Bytes***
Preamble	7
Start of the Frame	1
MAC	12
Protocol	2
IP Header	20
UDP Header	8
SPEAD Header	8 + 64
Padding	6
CRC32	4
Dead Time	2
Data Payload	4096 (4096 * 8 bits)

Table 1: 8 bit Packetizer Data Frame Structure

Packetizer Data Link Rates	***8-bit Mode***
BW (MHz)	2000
Start of the Frame	1
Sample Rate (Gsps)	4000
Bits	8
Polarizations	2
Payload Throughput (Gbps)	4000*2*8 = 64000
Link Efficiency	TBD
Effective Data Rate (Gbps)	TBD
ADC Snap Block Dump Rate	TBD
40GbE Utilization	TBD

Table 2: 8 bit Packetizer Data Link Rates

1.3 GHz Bandwidth @ 12 bits Samples Mode

In this mode, the Packetizer should transmit 6144 bytes, 12 bit signed data from the same polarization over 40GbE link. The layout of the data as well as link budget using 2x 40GbE links is given in Table 3 & 4 respectively.

ADC Data Frame	***Number of Bytes***
Preamble	7
Start of the Frame	1
MAC	12
Protocol	2
IP Header	20
UDP Header	8
SPEAD Header	8 + 64
Padding	6
CRC32	4
Dead Time	2
Data Payload	6144 (4096 * 12 bits)

Table 3: 12 bit Packetizer Data Frame Structure

Packetizer Data Link Rates	***12-bit Mode***
BW (MHz)	1300
Start of the Frame	1
Sample Rate (Gsps)	2600
Bits	12
Polarizations	2
Payload Throughput (Gbps)	2600*2*12 = 62400
Link Efficiency	TBD
Effective Data Rate (Gbps)	TBD
ADC Snap Block Dump Rate	TBD
40GbE Utilization	TBD

Table 4: 12 bit Packetizer Data Link Rates

1.1.3 EDD Filter Bank Data Packetization

The directly digitized data from Packetizer will be captured and converted to filter bank with a Polyphase filter bank and needs to be sent over high speed Ethernet using multicast streams. The specifications and requirements for the UBB mode are below.

Mode	***12 bit @ 1.3 GHz (UBB Receiver with direct digitization)***
Data rate (Incoming)	62.4 Gbps
Data format	SPEAD [*Refer 1.1.5*]
Timestamp	SPEADTIME [*Refer 1.1.1*]
Polyphase Filter Bank (PFB)	16-65536
PFB Width, Taps	<1 or >1 , Taps=8
FFT Channels	**64**
Data rate (outgoing)	41.6 Gbps
Data Format	SPEAD [*Refer 1.1.6*]
Platforms	ROACH2, SKARAB, GPU

1.1.4 SPEAD Parameters

1.1.4.1 Noise Diode Status

The SPEAD meta data header shall include a 1 bit field to indicate the status of the Noise Diode switch at the time stamp of the first ADC sample in the data payload.

Parameter Value	***Description***
0	Noise Diode Off
1	Noise Diode On

1.1.4.2 Digitizer/Packetizer Serial Number

TBC.

1.1.4.3 Digitizer/ Packetizer Receptor ID

TBC.

1.1.4.4 Digitizer / Packetizer Type

Parameter Value	***Description***
0	2.0 GHz Mode
1	1.3 GHz Mode
2-255	Reserved

1.1.4.5 Polarization ID

Parameter Value	***Description***
0	Vertical Polarization
1	Horizontal Polarization
2-3	Reserved

1.1.4.4 ADC Saturation Flag

The saturation flag should be set for a given packet if the ADC counts are saturated.

1.1.5 Packetizer SPEAD Specifications

The SPEAD specifications will differ for the planned two modes of operation. Details of SPEAD Flavor for the two modes are summarized below.

1.1.5.1 SPEAD Header

The SPEAD header has 64 bits size and contains information to identify the SPEAD flavor and its attributes and item pointers after the header. It is same for the two modes.

Magic Number(8 b)	*0x53*
SPEAD Version(8 b)	4
item id width (bytes) (8 b)	(64-48/8) = 2
heap address width in bytes (8 b)	48/8=6
<reserved> (16 b)	0
number of item pointers after header (16 b)	8

	2 GHz @ 8 bits	**1.3 GHz @ 12 bits**
SPEAD Flavor	*SPEAD-64-48*	*SPEAD-64-48*
SPEAD direct address IDs	0x1600,0x3101,0x3102	0x1600,0x3101,0x3102
SPEAD indirect address IDs	0x3310	0x3311
SPEAD Version	4	4
SPEAD Heap id (48b)	SPEADTIME	SPEADTIME (47b) + Pol Id (1b)
SPEAD Heap Size (48b)	4096 bytes	6144 bytes
SPEAD Payload Length (48b)	4096 bytes	6144 bytes
SPEAD Heap Offset (48b)	0	0
0x1600	SPEADTIME	SPEADTIME
0x3101	[digitiser_serial(24b) digitiser_type(8b) receptor_id(14b) pol_id(2b)]	[digitiser_serial(24b) digitiser_type(8b) receptor_id(14b) pol_id(2b)]
0x3102	[adc_count(16b) zeros (30b) adc_saturation_flag(1b) ndiode_flag(1b)]	[adc_count(16b) zeros (30b) adc_saturation_flag(1b) ndiode_flag(1b)]
0x3310 (8 bit) / 0x3311 (12 bit)	0	0

Table 5: SPEAD-64-48 Structure

1.1.5.2 Item Pointers

The current version has 8 item pointers which are followed after the header. The format of item pointer in SPEAD-64-48 and the item pointers in the given format are given in Table 7.

Item Pointer #	Item Pointer	MSB(1b)	(15b)	LSB (48b)
-	-	ItemAddressMode	ItemIdentifier	ItemAddress
1	heap_id	1	000 0000 0000 0001	SPEADTIME (47b) + Pol Id (1b)
2	heap_size	1	000 0000 0000 0010	4096 (8 bit) / 6144 (12 bit)
3	heap_offset	1	000 0000 0000 0011	0
4	payload _length	1	000 0000 0000 0100	4096 (8 bit) / 6144 (12 bit)
5	0x1600	1	001 0110 0000 0000	SPEADTIME
6	0x3101	1	011 0001 0000 0001	[digitiser_serial(24b) digitiser_type(8b) receptor_id(14b) pol_id(2b)]
7	0x3102	1	011 0001 0000 0010	[adc_count(16b) zeros (30b) adc_saturation_flag(1b) ndiode_flag(1b)]
8	0x3310/0x3311	0	011 0011 0000 0000	0

Table 6: SPEAD-64-48 Item Pointers

1.1.5.3 Payload Data

The SPEAD Payload should contain 8bit/12bit Signed ADC Samples with Oldest ADC Sample at the MSB position of the 64 bit word, packed contiguously over 64bit boundaries. An example of the SPEAD Payload word is given in Table 8.

SPEAD PACKET	**2 GHz @ 8 bits**	**1.3 GHz @ 12 bits**
9-521/777	Payload Word 1, [63:56] – ADC Sample 1 [7:0], [55:48] – ADC Sample 2 [7:0], [47:40] – ADC Sample 3 [7:0], [39:32] – ADC Sample 4 [7:0], [31:24] – ADC Sample 5 [7:0], [23:16] – ADC Sample 6 [7:0], [15:8] – ADC Sample 7 [7:0], [7:0] – ADC Sample 8 [7:0], …	Payload Word 1, [63:52] – ADC Sample 1 [11:0], [51:40] – ADC Sample 2 [11:0], [39:28] – ADC Sample 3 [11:0], [27:16] – ADC Sample 4 [11:0], [15:4] – ADC Sample 5 [11:0], [3:0] – ADC Sample 6 [11:8], Payload word 2, [63:56] – ADC Sample 8 [7:0], …

Table 7: SPEAD-64-48 Payload Structure

1.1.6 Backends SPEAD Specifications

The EDD Backends will receive data from the Packetizer and convert them to filter bank modes and send it over Ethernet using SPEAD protocol. Details of the SPEAD format to be used are given in Table 8.

SPEAD Flavor	*SPEAD-64-48*
SPEAD direct address IDs	0x1600,0x4101,0x4103,0x0000,0x0000,0x0000
SPEAD indirect address IDs	0x4300
SPEAD Version	4
SPEAD Heap id (48b)	SPEADTIME(28b) + Base Frequency(6b) + Board_id (14b)
SPEAD Heap Size (48b)	262,144 Bytes
SPEAD Payload Length (48b)	8192 bytes
SPEAD Heap Offset (48b)	Payload offset in heap
0x1600 (48b)	SPEADTIME
0x4101 (48b)	board_id (16b)
0x4103 (48b)	Base Frequency (12b)
0x4300 (48b)	0
0x0000 (48b)	0
0x0000 (48b)	0
0x0000 (48b)	0

Table 8: Backend SPEAD-64-48 Structure

1.1.6.1 SPEAD Header

The SPEAD header has 64 bits size and contains information to identify the SPEAD flavor and its attributes and item pointers after the header.

Magic Number(8 b)	*0x53*
SPEAD Version(8 b)	4
item id width (bytes) (8 b)	(64-48/8) = 2
heap address width in bytes (8 b)	48/8=6
<reserved> (16 b)	0
number of item pointers after header (16 b)	11

1.1.6.2 Item Pointers

The current version has 11 item pointers which are followed after the header. The format of item pointer in SPEAD-64-48 and **some** of the item pointers in the given format are given below:

Item Pointer #	Item Pointer	MSB(1b)	(15b)	LSB (48b)
-	-	ItemAddressMode	ItemIdentifier	ItemAddress
1	heap_id	1	000 0000 0000 0001	SPEADTIME(28b) + Base Frequency(6b) + Board_id(14b)
2	heap_size	1	000 0000 0000 0010	262,144 Bytes
3	heap_offset	1	000 0000 0000 0011	Payload offset in heap
4	payload_length	1	000 0000 0000 0100	8192
5	0x1600	1	001 0110 0000 0000	SPEADTIME
6	0x4101	1	100 0001 0000 0001	board_id
7	0x4103	1	100 0001 0000 0011	Frequency Channel
11	0x4300	0	100 0011 0000 0000	0

Table 9: Backend SPEAD-64-48 Item Pointers

2 Backend Setup

The Backends for EDD consist of ROACH2, SKARAB boards and GPU nodes which will convert digitized data into set of filter banks and tag them with the frequency bins information using SPEAD protocol. The filter bank data will be send out over Ethernet using Multicast streams. Information on the SPEAD protocol and data format is given in sections 1.1.3, 1.1.6.

2.1 System Setup

The Current EDD Packetizer sends data over 2x 40GbE links via the 40GbE/100GbE Ethernet switch to the ROACH2 board using 8x 10GbE SFP+ split cables. The ROACH2 board based backend either will down convert the data or convert it to filter bank data before sending it the GPU node for further processing. The Packetizer data can as well be directly captured from a GPU node for direct processing.

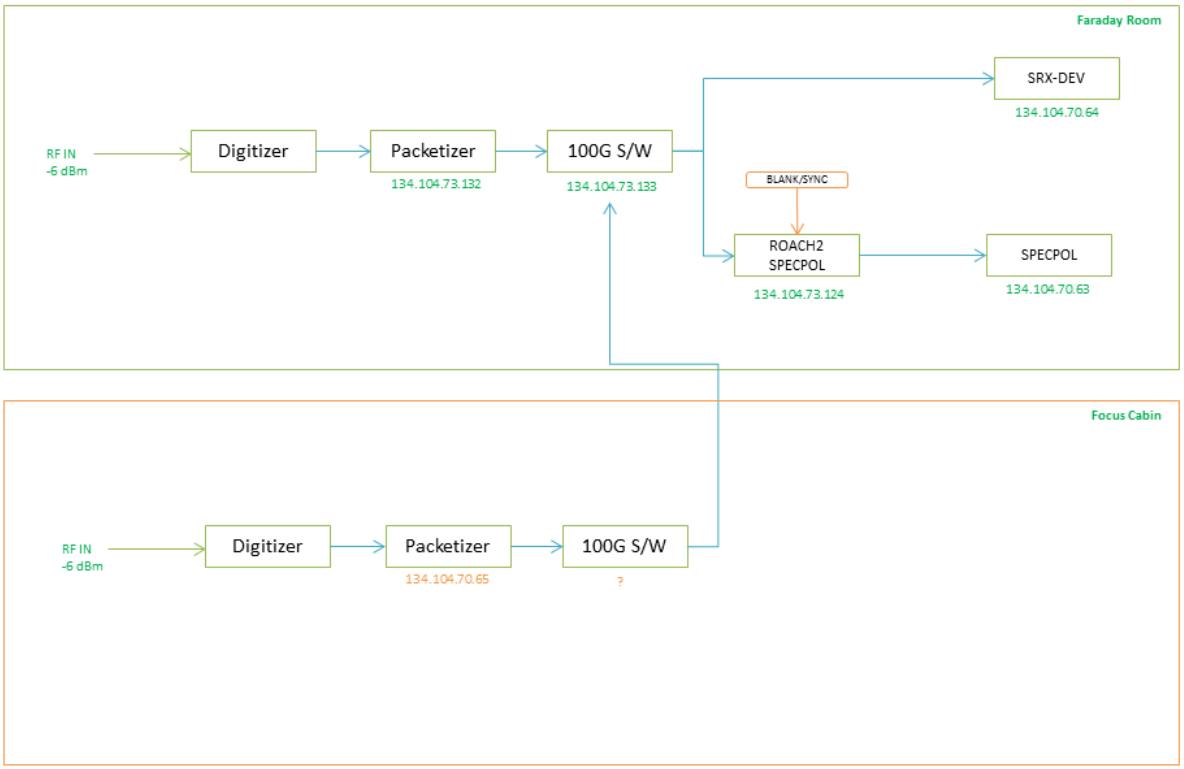

Figure 2: System Setup for Effelsberg Direct Digitization Test

The Setup consists of following components:

1. ROACH2 board with Multicast Support
2. Digitizer + Packetizer units with 2x 40GbE Links
3. Mellanox SN2100 40GbE/100GbE Switches (VLAN 100)
4. HPC GPU Node (ROACH2/Switch Control & Data Capture, Reduction)

2.2 Firmwares

A set of firmwares based on ROACH2 are developed to implement the test the EDD in Faraday room at Effelsberg radio telescope followed by using the UBB receiver with direct digitization.

The initial test will consist of the following firmwares:

- Full Resolution Firmware for Pulsar Timing
  - Compatible with existing Pulsar Timing Data Processing Backend
  - Currently downconverts to 500 MHz BW but can support 2 GHz subject to performance of GPU nodes w/ realtime dspsr.
  - Can be easily extended to support SPEAD format for SPEAD receiver

- Spectro-Polarimeter firmware with 2048 PFB/FFT and Blank/Sync Support
  - Compiled at 265 MHz to support 2 GHz Bandwidth
  - Supports 32bit Accumulations to be compatible with FITS writer
  - Current only support Stokes I but can be extended to full Stokes
  - Can be extended to support SPEAD format

After the first stage of testing, the direct digitization scheme will be tested with UBB receiver. A ROACH2 firmware is developed to stream filter bank data over SPEAD format.

- Coherent DeDispersion PFB/FFT Firmware with SPEAD Support
  - Processes 64 Gbps data from Packetizer and converts to filter banks
  - 8 tap PFB/FFT with required number of Frequency channels
  - Supports SPEAD format to tag filter bank data out over multicast streams
  - Output data rate at 42.6 Gbps

The above firmware can be easily extended to support packetizers with different link rates and will be extended to SKARAB platform to support higher bandwidths.

3 References

1. http://casper.berkeley.edu/astrobaki/images/9/93/SPEADsignedRelease.pdf

2. https://casper.berkeley.edu/wiki/SPEAD

3. L-Band Digitizer CBF Interface Control Document (M1000-0001-053, Version: 3)